PL611s-27

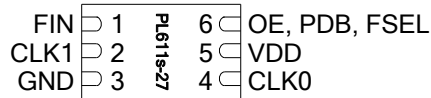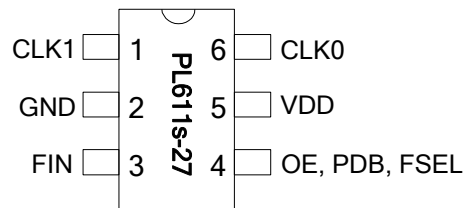## 1.8V to 3.3V PicoPLL^{TM} Programmable Clock

FEATURES

- Advanced One Time Programmable (OTP) PLL design
- Very low Jitter and Phase Noise
    - 30-70ps Pk-Pk typical
- Output Frequency up to
    - 65MHz @ 1.8V operation
    - 90MHz @ 2.5V operation
    - 125MHz @ 3.3V operation
- Reference Input Frequency: 1MHz to 200MHz
- Accepts >0.1V square or sine wave input
- Low current consumption, <10µA when PDB is activated
- One programmable I/O pin can be configured as Output Enable (OE), Frequency Switching (FSEL), or Power Down (PDB) input.
- Outputs disable to Active Low state.
- Single 1.8V ~ 3.3V, ± 10% power supply
- Operating temperature range from -40°C to 85°C
- Available in 6-pin DFN and SOT23 GREEN/RoHS compliant packages.

DESCRIPTION

The PL611s-27 is a general purpose frequency synthesizer and a member of PicoPLL product family. Designed to fit in a small 6-pin DFN, or 6-pin SOT package for high performance applications, the PL611s-27 offers very low phase noise, jitter, and power consumption, while offering 2 clock outputs. The Frequency Switching (FSEL) capability of PL611s-27 allows for programming two sets of frequencies, while the power down feature of PL611s-27, when activated, allows the IC to consume less than 10µA of power. PL611s-27's programming flexibility allows generating any output using a reference input signal.
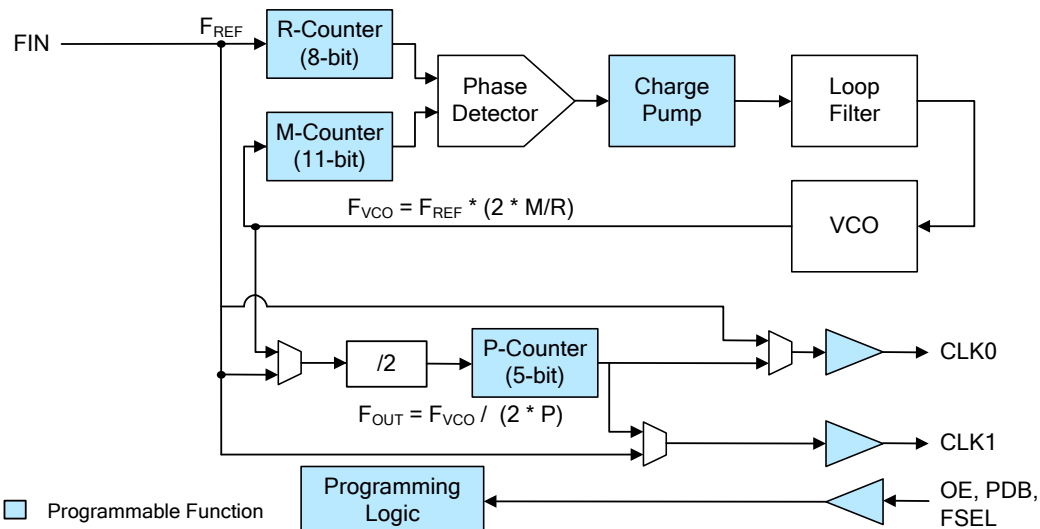
PACKAGE PIN CONFIGURATION

FIN	1		6	OE, PDB, FSEL
CLK1	2	PL611s-27	5	VDD
GND	3		4	CLK0

DFN-6L
(2.0 x 1.3 x 0.6mm)

CLK1	1		6	CLK0
GND	2	PL611s-27	5	VDD
FIN	3		4	OE, PDB, FSEL

SOT23-6L
(3.0 x 3.0 x 1.35mm)

BLOCK DIAGRAM

$$F_{VCO} = F_{REF} * (2 * M/R)$$

$$F_{OUT} = F_{VCO} / (2 * P)$$

1.8V to 3.3V PicoPLL™ Programmable Clock

KEY PROGRAMMING PARAMETERS

CLK[0:1] Output Frequency	Output Drive Strength	Programmable Input/Output

$F_{OUT} = F_{REF} * M / (R * P)$
Where   M = 11 bit
           R = 8 bit
           P = 5 bit
$CLK0 = F_{OUT}$, F_{REF} or F_{REF} / (2*P)
$CLK1 = F_{REF}$ or CLK0
	Three optional drive strengths to choose from:
	
	• Low: 4mA
	• Std: 8mA (default)
	• High: 16mA
		One pin can be configured as:
		
		• OE - input
		• PDB - input
		• FSEL – input

PACKAGE PIN ASSIGNMENT

Name	Pin Assignment DFN Pin#	Pin Assignment SOT Pin #	Type	Description
CLK1	2	1	O	Programmable Clock Output. CLK1 = CLK0 or CLK1=F_{REF}
GND	3	2	P	GND connection
FIN	1	3	I	Reference input pin
OE, PDB, FSEL	6	4	I	This programmable I/O pin can be configured as an Output Enable (OE) input, Power Down (PDB) input or Frequency Switching (FSEL) input. <table><tr><th>State</th><th>OE</th><th>PDB</th><th>FSEL</th></tr><tr><td>0</td><td>Disable CLK</td><td>Power Down Mode</td><td>Bank '0'</td></tr><tr><td>1 (default)</td><td>Normal mode</td><td>Normal mode</td><td>Bank '1'</td></tr></table>
VDD	5	5	P	VDD connection
CLK0	4	6	O	Programmable Clock Output

The embedded table within the OE, PDB, FSEL description:

State	OE	PDB	FSEL
0	Disable CLK	Power Down Mode	Bank '0'
1 (default)	Normal mode	Normal mode	Bank '1'

OE AND PDB FUNCTION DESCRIPTION

OE	PDB	Osc.	PLL	CLK0	CLK1 When CLK1=F_{REF}	CLK1 When CLK1=CLK0
1(Default)	N/A	On	On	On	On	On
0	N/A	On	Off	Active Low	On	Active Low
N/A	1(Default)	On	On	On	On	On
N/A	0	Off	Off	Active Low	Active Low	Active Low

FUNCTIONAL DESCRIPTION

PL611s-27 is a highly featured, very flexible, advanced programmable PLL design for high performance, low-power, small form-factor applications. The PL611s-27 accepts a reference clock input of 1MHz to 200MHz and is capable of producing two outputs up to 125MHz. This flexible design allows the PL611s-27 to deliver any PLL generated frequency, F_{REF} (Ref Clk) frequency or $F_{REF}/(2*P)$ to CLK0 and/or CLK1. Some of the design features of the PL611s-27 are mentioned below:

PLL Programming

The PLL in the PL611s-27 is fully programmable. The PLL is equipped with an 8-bit input frequency divider (R-Counter), and an 11-bit VCO frequency feedback loop divider (M-Counter). The output of the PLL is transferred to a 5-bit post VCO divider (P-Counter). The output frequency is determined by the following formula [$F_{OUT} = F_{REF} * M / (R * P)$].

Clock Output (CLK0)

CLK0 is the main clock output. The output of CLK0 can be configured as the PLL output ($F_{VCO}/(2*P)$), F_{REF} (Ref Clk Frequency) output, or $F_{REF}/(2*P)$ output. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is 125MHz (3.3V).

Clock Output (CLK1)

The CLK1 feature allows the PL611s-27 to have an additional clock output. This output can be programmed to one of the following:

> F_{REF} - Reference (Ref Clk) Frequency
> CLK0

When using the OE function CLK1 will remain "Always On" if programmed as F_{REF} output and *will not* be disabled when OE is pulled low. If CLK1 is programmed to equal CLK0 then the output *will* disable when OE is pulled low. When using the PDB function CLK1 will always be disabled along with CLK0. The output drive level can be programmed to Low Drive (4mA), Standard Drive (8mA) or High Drive (16mA). The maximum output frequency is 125MHz (3.3V).

Output Enable (OE)

The Output Enable feature allows the user to enable and disable the CLK0 and/or CLK1 outputs by toggling the OE pin.

Power-Down Control (PDB)

The Power Down (PDB) feature allows the user to put the PL611s-27 into "Sleep Mode". When activated (logic '0'), PDB 'Disables the PLL, the oscillator circuitry, counters, and all other active circuitry. In Power Down mode the IC consumes <10μA of power.

Frequency Select (FSEL)

The Frequency Select (FSEL) feature allows the PL611s-27 to switch between two pre-programmed banks allowing the device "On the Fly" frequency switching.

1.8V to 3.3V PicoPLL™ Programmable Clock

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{DD}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{DD}+0.5	V
Output Voltage Range	V_O	-0.5	V_{DD}+0.5	V
Soldering Temperature (Green package)			260	°C
Data Retention @ 85°C		10		Year
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*		-40	85	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied. *Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

AC SPECIFICATIONS

| PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input (FIN) Frequency	All operating voltages (see Input Signal Amplitude restrictions below)	1		200	MHz
Input (FIN) Signal Amplitude	DC Coupled, LVCMOS input, High	0.7*V_{DD}			Vpp
	DC Coupled, LVCMOS input, Low			0.3*V_{DD}	
Input (FIN) Signal Amplitude	Internally AC coupled (High Frequency)	0.9		V_{DD}	Vpp
Input (FIN) Signal Amplitude	Internally AC coupled (Low Frequency) 3.3V ≤50MHz, 2.5V ≤40MHz, 1.8V ≤15MHz	0.1		V_{DD}	Vpp
Output Frequency	@ V_{DD} =3.3V			125	MHz
	@ V_{DD} =2.5V			90	MHz
	@ V_{DD} =1.8V			65	MHz
Settling Time	At power-up (after V_{DD} increases over 1.62V)			2	ms
Output Enable Time	OE Function; Ta=25º C, 15pF Load. Add one clock period to this measurement for a usable clock output.			10	ns
	PDB Function; Ta=25º C, 15pF Load			2	ms
Output Rise Time	15pF Load, 10/90% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Output Fall Time	15pF Load, 90/10% V_{DD}, High Drive, 3.3V		1.2	1.7	ns
Duty Cycle	V_{DD} / 2	45	50	55	%
Period Jitter,Pk-to-Pk* (10,000 samples measured)	Capacitive decoupling between V_{DD} and GND.		70		ps

* Note: Jitter performance depends on the programming parameters.

1.8V to 3.3V PicoPLL™ Programmable Clock

DC SPECIFICATIONS

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with Loaded LVCMOS Outputs	I_{DD}	@ V_{DD} =3.3V, 27MHz, load=15pF		5.5		mA
Supply Current, Dynamic, with Loaded LVCMOS Outputs	I_{DD}	@ V_{DD} =2.5V, 27MHz, load=15pF		3.8		mA
Supply Current, Dynamic with Loaded LVCMOS Outputs	I_{DD}	@ V_{DD} =1.8V, 27MHz, load=15pF		1.8		mA
Stand By Current, with Loaded Outputs	I_{DD}	When PDB=0			<10	µA
Operating Voltage	V_{DD}		1.62		3.63	V
Power Supply Ramp	t_{PU}	Time for V_{DD} to reach 90% V_{DD}. Power ramp must be monotonic.			100	ms
Output Low Voltage	V_{OL}	I_{OL} = +4mA Std Drive			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA Std Drive	$V_{DD} - 0.4$			V
Output Current, Low Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	4			mA
Output Current, Standard Drive	I_{OSD}	V_{OL} = 0.4V, V_{OH} = 2.4V	8			mA
Output Current, High Drive	I_{OHD}	V_{OL} = 0.4V, V_{OH} = 2.4V	16			mA

1.8V to 3.3V PicoPLL™ Programmable Clock

LAYOUT RECOMMENDATIONS
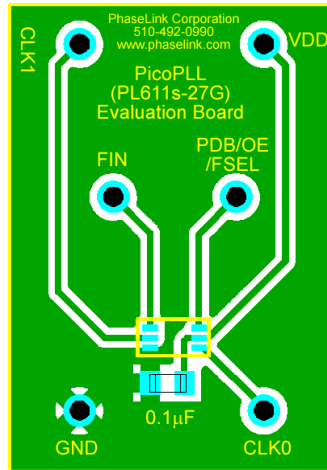
DFN-6L Evaluation Board

The following guidelines are to assist you with a performance optimized PCB design:
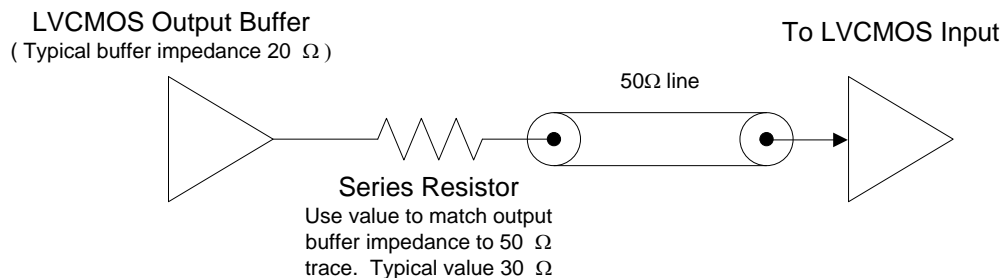
Signal Integrity and Termination Considerations

- Keep traces short!

- Trace = Inductor. With a capacitive load this equals ringing!

- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).

- Design long traces (> 1 inch) as "striplines" or "microstrips" with defined impedance.

- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply

- Multiple VDD pins should be decoupled separately for best performance.

- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources

- Value of decoupling capacitor is frequency dependant. Typical values to use are $0.1\mu F$ for designs using frequencies < 50MHz and $0.01\mu F$ for designs using frequencies > 50MHz.

Typical LVCMOS termination
Place Series Resistor as close as possible to LVCMOS output

LVCMOS Output Buffer
(Typical buffer impedance 20 Ω)

To LVCMOS Input

50Ω line

Series Resistor
Use value to match output buffer impedance to 50 Ω trace. Typical value 30 Ω

1.8V to 3.3V PicoPLL™ Programmable Clock

PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

SOT23-6L

Symbol	Dimension in MM	
	Min.	Max.
A	1.05	1.35
A1	0.05	0.15
A2	1.00	1.20
b	0.30	0.50
c	0.08	0.20
D	2.80	3.00
E	1.50	1.70
H	2.60	3.0
L	0.35	0.55
e	0.95 BSC	
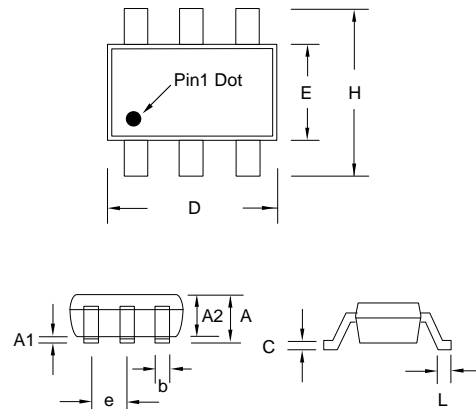
DFN-6L

Symbol	Dimension in MM	
	Min.	Max.
A	0.50	0.60
A1	0.00	0.05
A3	0.152	0.152
b	0.15	0.25
e	0.40BSC	
D	1.25	1.35
E	1.95	2.05
D1	0.75	0.85
E1	0.95	1.05
L	0.20	0.30
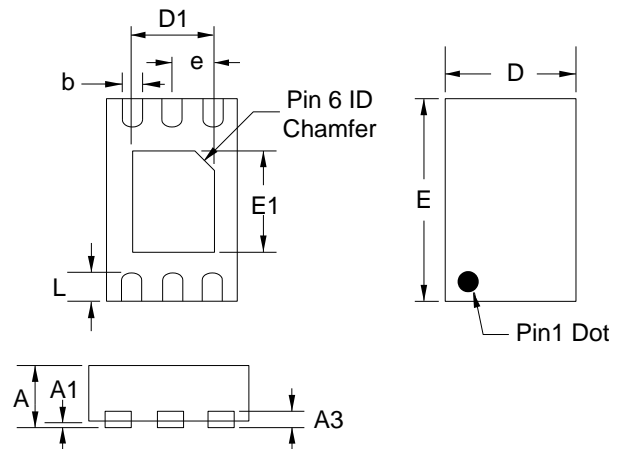
1.8V to 3.3V PicoPLL™ Programmable Clock
ORDERING INFORMATION (GREEN PACKAGE COMPLIANT)

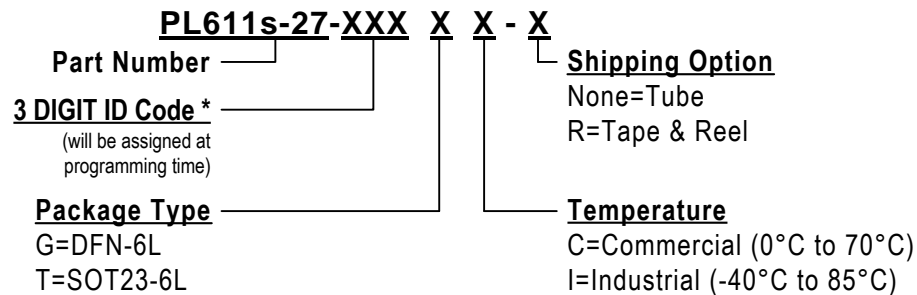*For part ordering, please contact our Sales Department:*
2180 Fortune Drive, San Jose, CA 95131, USA
Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER
The order number for this device is a combination of the following:
Part number, Package type and Operating temperature range

PL611s-27-XXX X X - X

Part Number

3 DIGIT ID Code *
(will be assigned at programming time)

Package Type
G=DFN-6L
T=SOT23-6L

Shipping Option
None=Tube
R=Tape & Reel

Temperature
C=Commercial (0°C to 70°C)
I=Industrial (-40°C to 85°C)

* Micrel will assign a unique 3-digit ID code for each approved programmed part number.

Part/Order Number	Marking†	Package Option
PL611s-27-XXXGC-R	XXX	6-Pin DFN (Tape and Reel)
PL611s-27-XXXTC-R	27XXX	6-Pin SOT23 (Tape and Reel)

† Note: 'XXX' designates marking identifier that, at times, could be independent of the part number.