PICOR
Semiconductor Power Solutions

360μΩ, 5 V/60 A N-Channel MOSFET

Product Description

The PI5101μR_{DS}(on) FET™ solution combines a high-performance 5 V, 360 μΩ lateral N-Channel MOSFET with a thermally enhanced high density 4.1mm x 8mm x 2mm land-grid-array (LGA) package to enable world class performance in the footprint area of an industry standard SO-8 package. The PI5101 offers unprecedented figure-of-merits for DC & switching applications. The PI5101 will replace up to 6 conventional "SO-8 form factor" devices for the same on-state resistance, reducing board space by ~80%. The PI5101 offers unprecedented figure-of-merit for $R_{DS(on)}$ x Q_G, gate resistance (R_G) and package inductance (L_{DS}) outperforming conventional Trench MOSFETs and enabling very low loss operation.

The PI5101 LGA package is fully compatible with industry standard SMT assembly processes.

Features

- Ultra Low "micro-Ohm" $R_{DS(on)}$
- Extremely Low Gate Charge
- Very Low Gate Resistance
- High Density, Low Profile
- Very Low Package Inductance
- Low Thermal Resistance

Applications

- Power Path Management Solutions
- Active ORing & Load Switches
- High Current DC-DC Converters

Product Summary

Symbol	Condition	Value	
I_D	T_A = 25°C	60 A_{DC}	Max
$V_{(BR)DSS}$	I_D = 5 mA	5 V	Min
$R_{DS(ON)}$	V_{GS} = 4.5 V	360 μΩ	Typ
	V_{GS} = 3.5 V	380 μΩ	Typ
Q_G	V_{GS} = 4.5 V	65 nC	Typ
R_G		0.1 Ω	Typ
L_{DS}		0.1 nH	Typ

Package Information

- 4.1mm x 8mm x 2mm
  Thermally Enhanced LGA

Order Information

Part Number	Package	Transport Media
PI5101-01-LGIZ	4.1mm x 8mm x 2mm 3-Lead LGA	T&R

Maximum Rating and Thermal Characteristics

T_A = 25°C unless otherwise specified.

Parameter		Symbol	Limit	Unit
Drain-to-Source Voltage		V_{DS}	5	V
Gate-to-Source Voltage		V_{GS}	±5	V
Drain Current	Continuous	I_D	60	A
	Pulsed	I_{DM}	150	A
Single Pulse Avalanche Current	T_{AV} <100 µs	I_{AS}	100	A
Maximum Power Dissipation	T_A = 25°C	P_D	3.1	W
	T_A = 70°C		2	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C
Thermal Resistance [1]	Junction-to-Ambient	$R_{\theta J\text{-}A}$	40	°C/W
	Junction-to-PCB	$R_{\theta J\text{-}PCB}$	6	°C/W
Lead Temperature (Soldering, 20 sec)			260	°C

[1] The thermal resistance is measured when the device is mounted on 1 inch square 4-layer 2-oz copper FR-4 PCB at 0LFM and 40A drain current

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 5 mA	5.0			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_J}$	Reference to 25°C, V_{GS} = 0 V, I_D = 5 mA		3.1		mV/°C
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 4.8 V, V_{GS} = 0 V		0.2	2	µA
Gate-to-Source Leakage	I_{GSS}	V_{GS} = 5 V, V_{DS} = 0 V		10	200	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	0.4		0.8	V
Drain-to-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 60 A		360	450	µΩ
		V_{GS} = 3.5 V, I_D = 60 A		380	475	µΩ
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 4.5 V, I_D = 60 A, R_G = 0.1Ω		14		ns
Rise Time	t_r	V_{GS} = 4.5 V, I_D = 60 A, R_G = 0.1Ω		4.5		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{GS} = 4.5 V, I_D = 60 A, R_G = 0.1Ω		23		ns
Fall Time	t_f	V_{GS} = 4.5 V, I_D = 60 A, R_G = 0.1Ω		3.5		ns
Forward Transconductance	gfs	I_D = 60 A, V_{DS} = 4 V		620		S
Gate Capacitance						
Input Capacitance	C_{iss}	V_{DS} = 5 V, V_{GS} = 0 V, f = 1MHz; See Figure 6		7600		pF
Output Capacitance	C_{oss}	V_{DS} = 5 V, V_{GS} = 0 V, f = 1MHz; See Figure 6		5200		pF
Reverse Transfer Capacitance	C_{rss}	V_{DS} = 5 V, V_{GS} = 0 V, f = 1MHz		1100		pF
Gate Charge						
Total Gate Charge	Q_g	V_{GS} = 4.5 V, V_{DD} = 4.4 V, I_D = 60 A; See Figure 3		65		nC
Gate-to-Source Charge	Q_{gs}	V_{GS} = 4.5 V, V_{DD} = 4.4 V, I_D = 60 A		7.7		nC
Gate-to-Drain Charge	Q_{gd}	V_{GS} = 4.5 V, V_{DD} = 4.4 V, I_D = 60 A		9.0		nC
Gate Resistance	R_G			0.1		Ω
Reverse Diode						
Source-to-Drain Reverse Recovery Time	t_{rr}	I_S = 16 A, di/dt = 33 A/µs		300		ns
Diode Forward Voltage	V_{SD}	I_S = 16 A, V_{GS} = 0 V (Pulse Test)		0.63	1.0	V
Package Inductance	L_{DS}			0.1		nH

Typical Characteristics

T_A = 25°C unless otherwise specified.

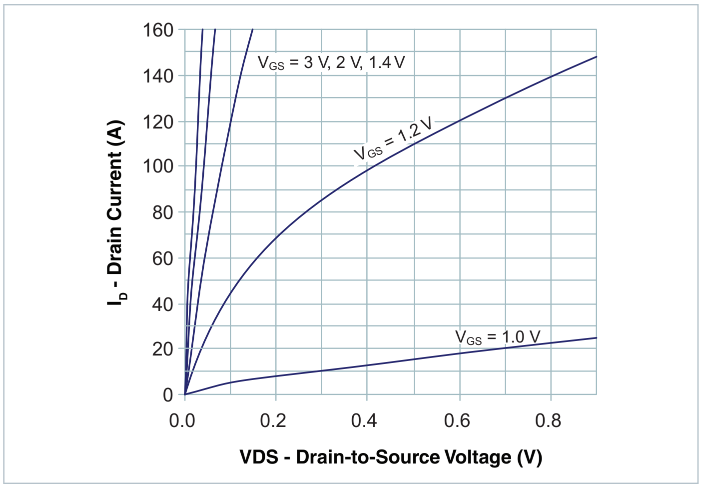


Figure 1 *— Output Characteristics (Pulsed V_{GS})*

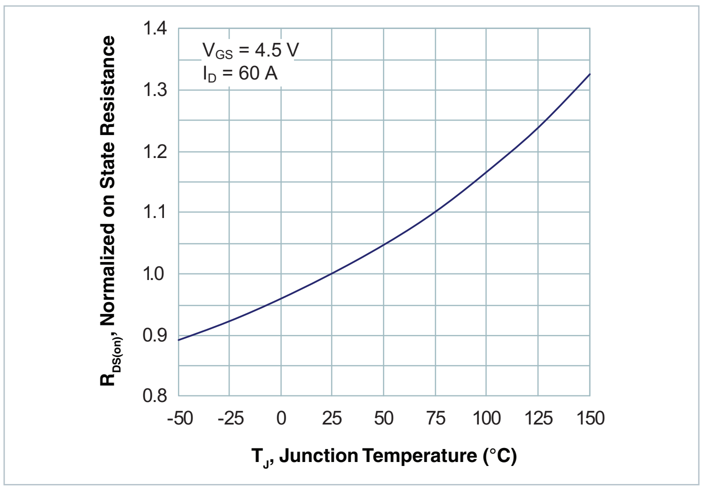


Figure 2 *— On-Resistance vs. Junction Temperature*

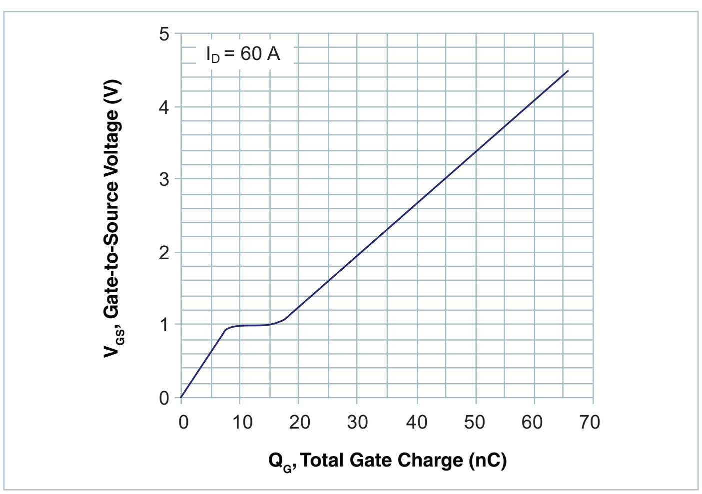


Figure 3 *— Gate Charge*

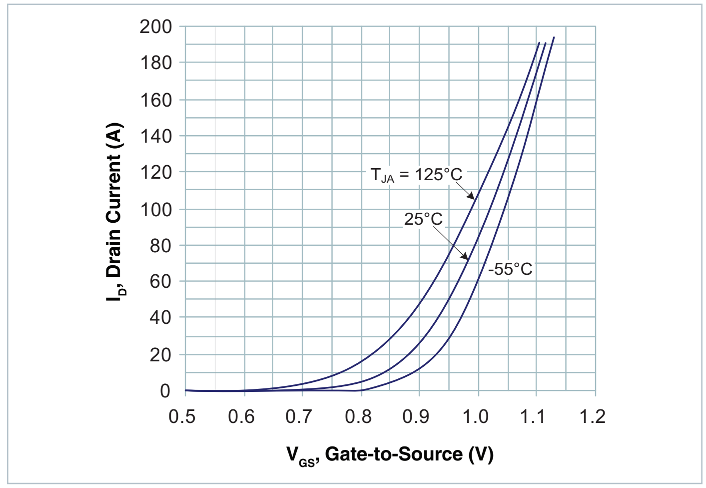


Figure 4 *— Transfer Characteristics (Pulsed V_{GS})*

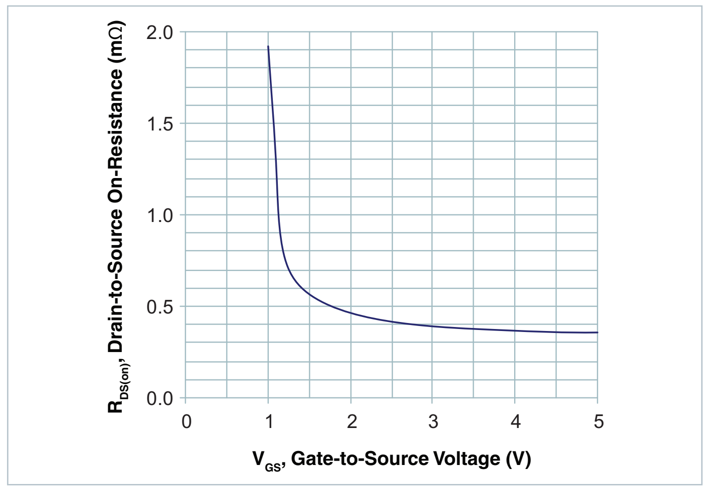


Figure 5 *— On-Resistance vs. Gate Voltage*

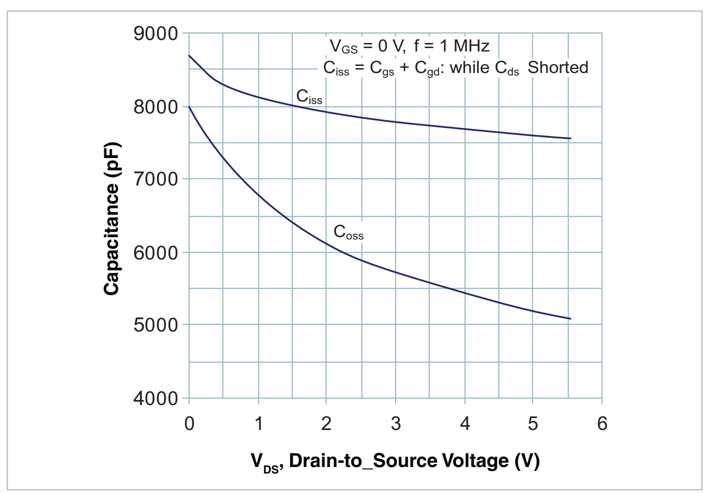


Figure 6 *— Gate Capacitance vs. Drain-to Source Voltage*

Typical Characteristics

T_A = 25°C unless otherwise specified.

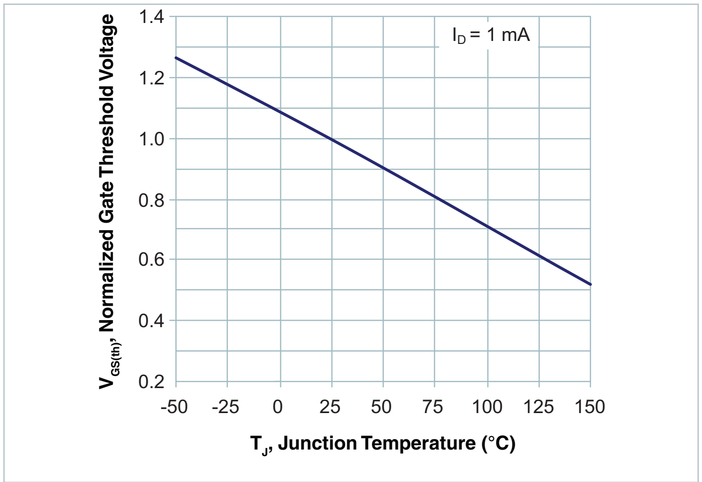


Figure 7 — Gate Threshold Voltage vs. Temperature

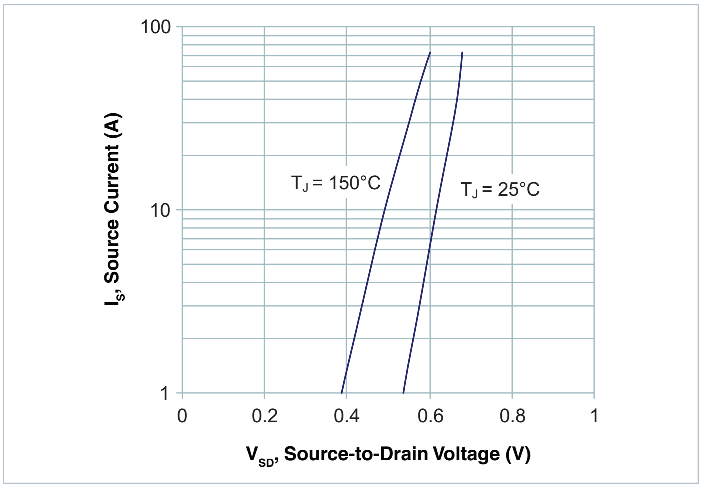


Figure 10 — Reverse Diode Forward Voltage (Pulsed Test)

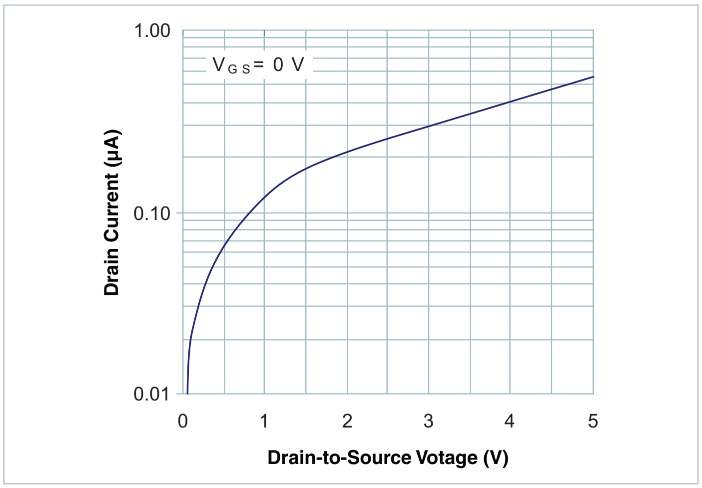


Figure 8 — Drain-to-Source Leakage Current

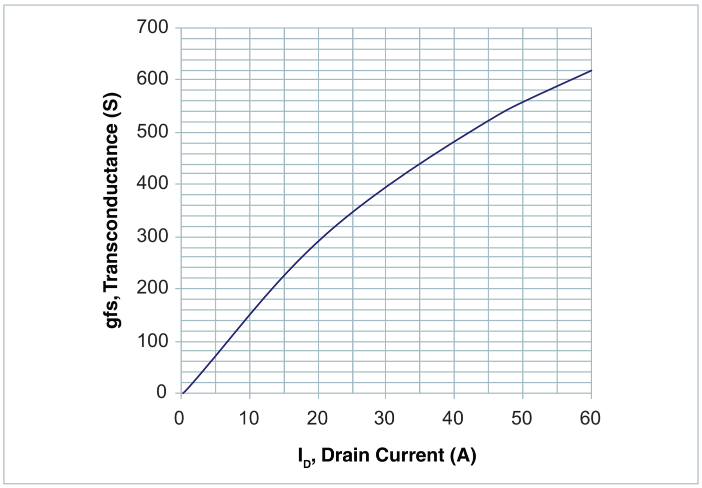


Figure 11 — Forward Transconductance

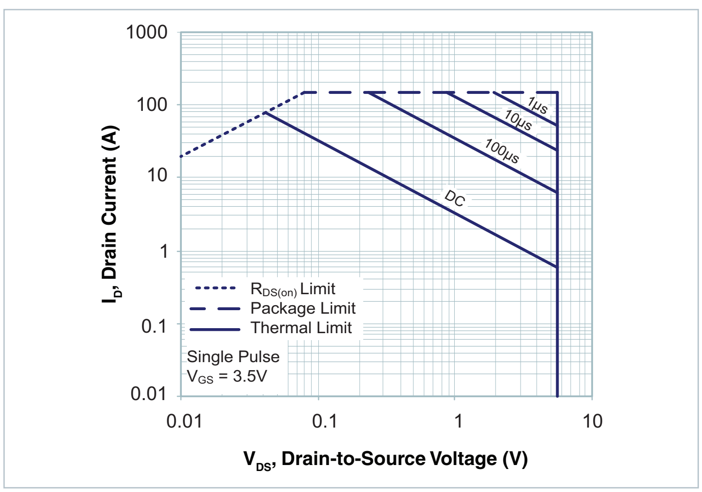


Figure 9 — Maximum Safe Operation Area

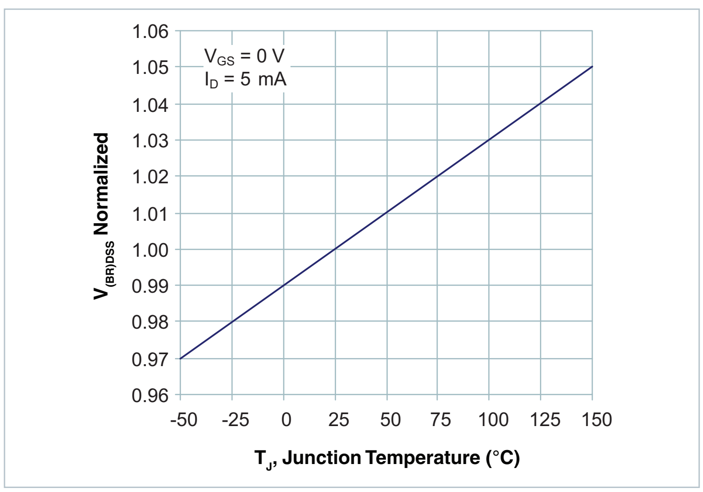


Figure 12 — Drain-to-Source Breakdown Voltage vs. temperature

Typical Characteristics

T_A = 25°C unless otherwise specified.

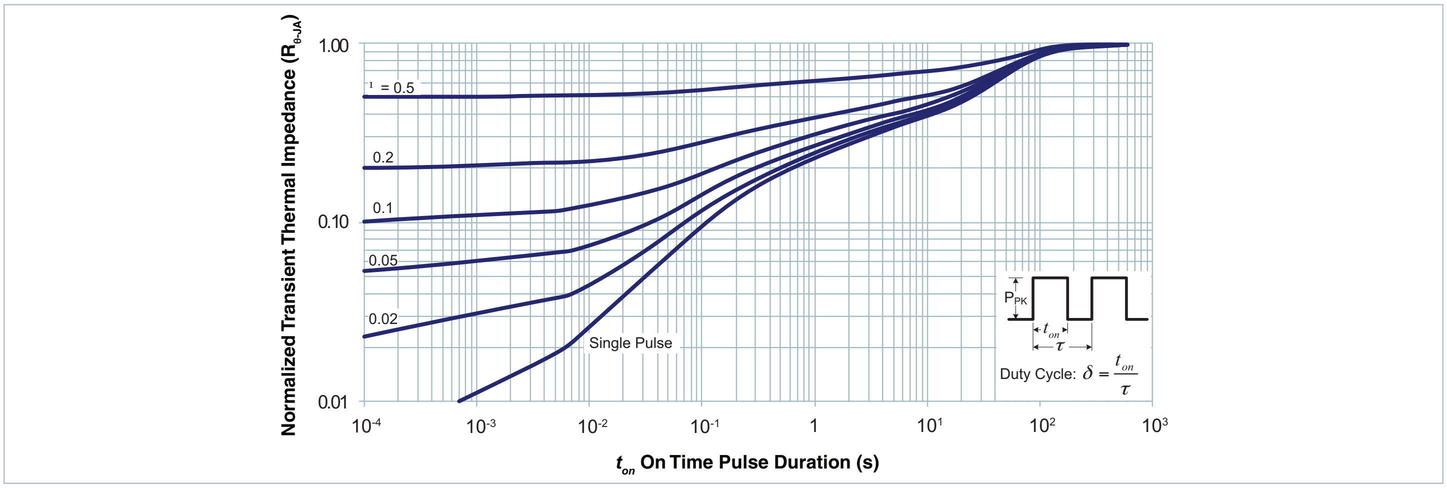


Figure 13 *— Normalized Transient Thermal Impedance, Junction-to-Ambient*

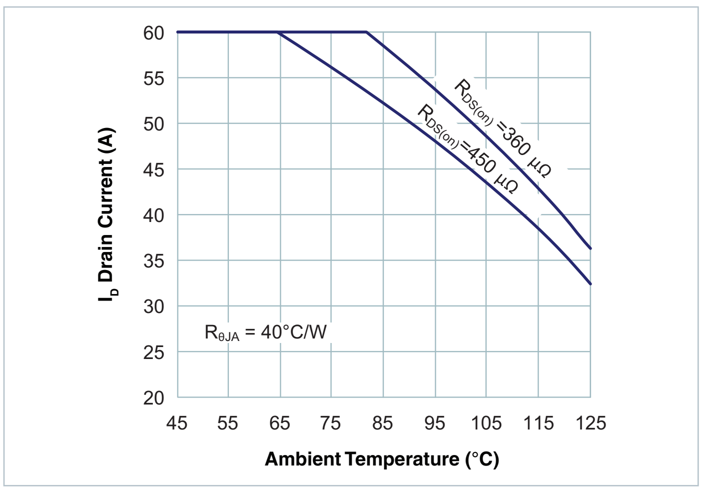


Figure 14 *— PI5101 Drain current de-rating based on the maximum TJ = 150°C vs. ambient temperature*

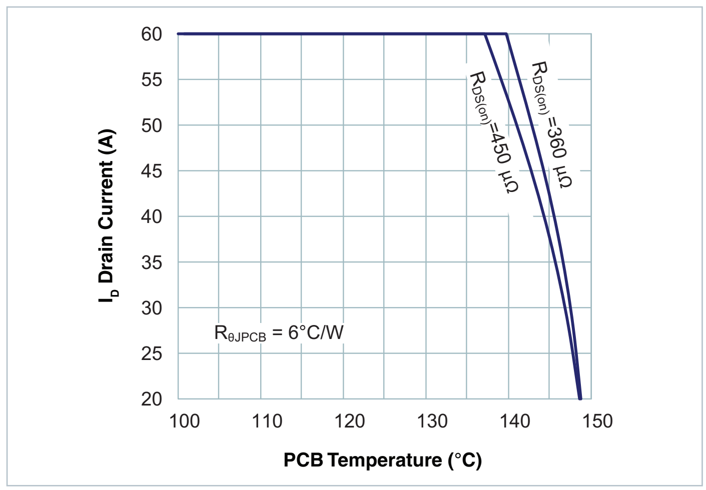


Figure 15 *— PI5101 Drain current de-rating vs. PCB temperature, for maximum TJ at 150°C*

MOSFET Power Dissipation vs. Junction Temperature

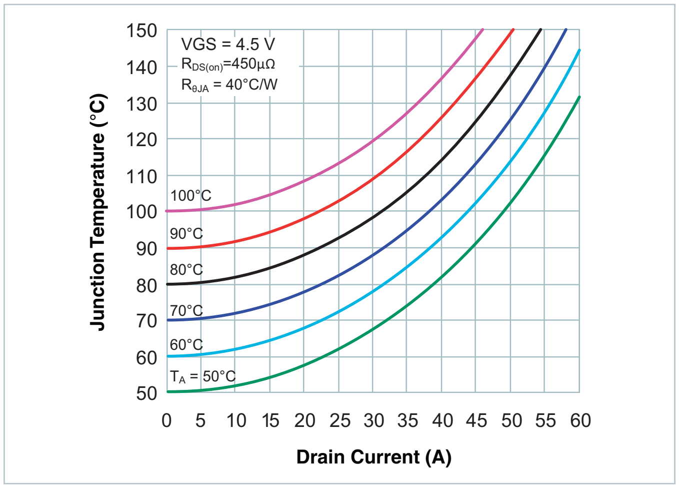


Figure 16 *— Junction Temperature vs. Drain Current for a given ambient temperature (0LFM)*

In applications such as low loss ORing Diodes or circuit breakers where the MOSFET is normally on during steady state operation, the MOSFET power dissipation is derived from the total Drain current and the on-state resistance of the MOSFET.

The PI5101 power dissipation can be calculated with the following equation:

$$P_D = I_D^2 \bullet R_{DS(on)}$$

Where:

P_D: MOSFET power dissipation
I_D : Drain Current
$R_{DS(on)}$: MOSFET on-state resistance

Note: *For the worst case condition, calculate with maximum rated $R_{DS(on)}$ at the MOSFET maximum operating junction temperature because $R_{DS(on)}$ is temperature dependent. Refer to figure 2 for normalized $R_{DS(on)}$ values over temperature. The PI5101 maximum $R_{DS(on)}$ at 25°C is 450 µΩ and will increase by 24% at 125°C junction temperature.*

The junction temperature rise is a function of power dissipation and thermal resistance.

$$T_{rise} = R_{\theta JA} \bullet P_D = R_{JA} \bullet I_D^2 \bullet R_{DS(on)}$$

Where:

$R_{\theta JA}$: Junction-to-Ambient thermal resistance (40°C/W)

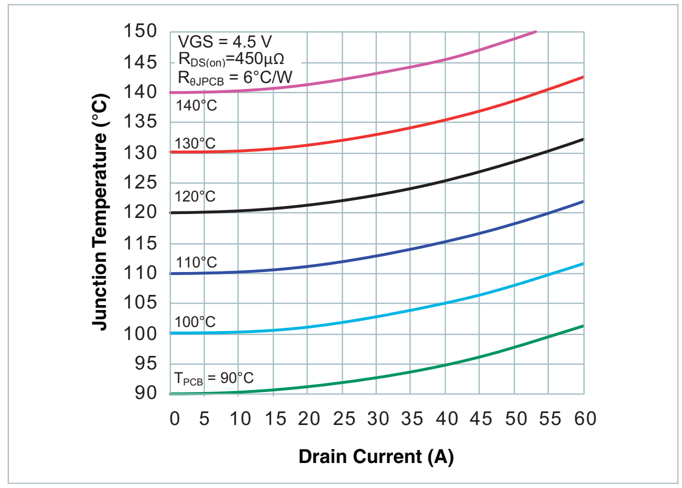


Figure 17 *— Junction Temperature vs. Drain Current for a given PCB temperature*

This may require iteration to get to the final junction temperature. figure 16 and figure 17 are added to aid the user to find the final junction temperature without the iterative calculations.

Figure 16 shows the MOSFETs final junction temperature curves versus conducted current at maximum $R_{DS(on)}$, and at given ambient temperatures at 0 LFM air flow. Figure 17 shows the MOSFETs final junction temperature curves versus conducted current at maximum $R_{DS(on)}$ at given PCB temperatures.

To find the final junction temperature for a given drain continuous DC or RMS current and a given ambient or PCB temperature; draw a vertical line from the drain current at the X-axis to intersect the ambient or PCB temperature line. At the intersection draw a horizontal line towards the Y-axis (Junction Temperature).

Example:

Assume that the MOSFET maximum drain current is 50 A and maximum operating ambient temperature is 70°C.

First use figure 16 to find the final junction temperature for 50 A drain current at 70°C ambient temperature. In figure 16 (illustrated in figure 18) draw a vertical line from 50 A to intersect the 70°C ambient temperature line (dark blue). At the intersection draw a horizontal line towards the Y-axis (Junction Temperature). The typical junction temperature with maximum $R_{DS(on)}$, at load current of 50 A and 70°C ambient is 126°C.

As a check, recalculate the junction temperature to confirm the plot results. Start from the final junction temperature, 126°C, and use the following steps:

RDS(on) is 450µΩ maximum at 25°C and will increase as the Junction temperature increases. From figure 2, at 126°C RDS(on) will increase by 24%, then RDS(on) maximum at 126°C is:

$$R_{DS(on)} = 450\ \mu\Omega \bullet 1.24 = 558\ \mu\Omega$$

Maximum power dissipation is:

$$P_{Dmax} = I_D^2 \bullet R_{DS(on)} = 50\ A \bullet 558\ \mu\Omega = 1.39\ W$$

Maximum junction temperature is:

$$T_{Jmax} = 70°C + \frac{40°C}{W}\ 50\ A^2 \bullet 558\ \mu\Omega = 125.8°C$$

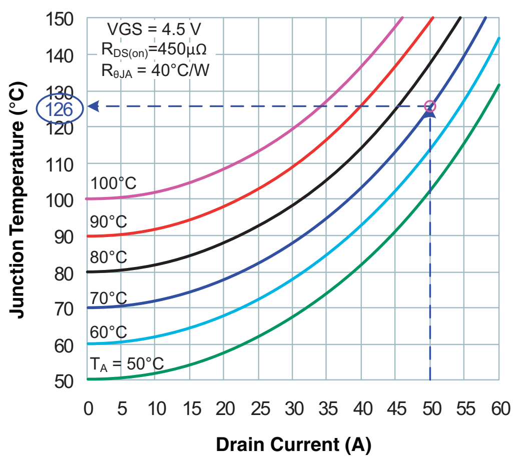
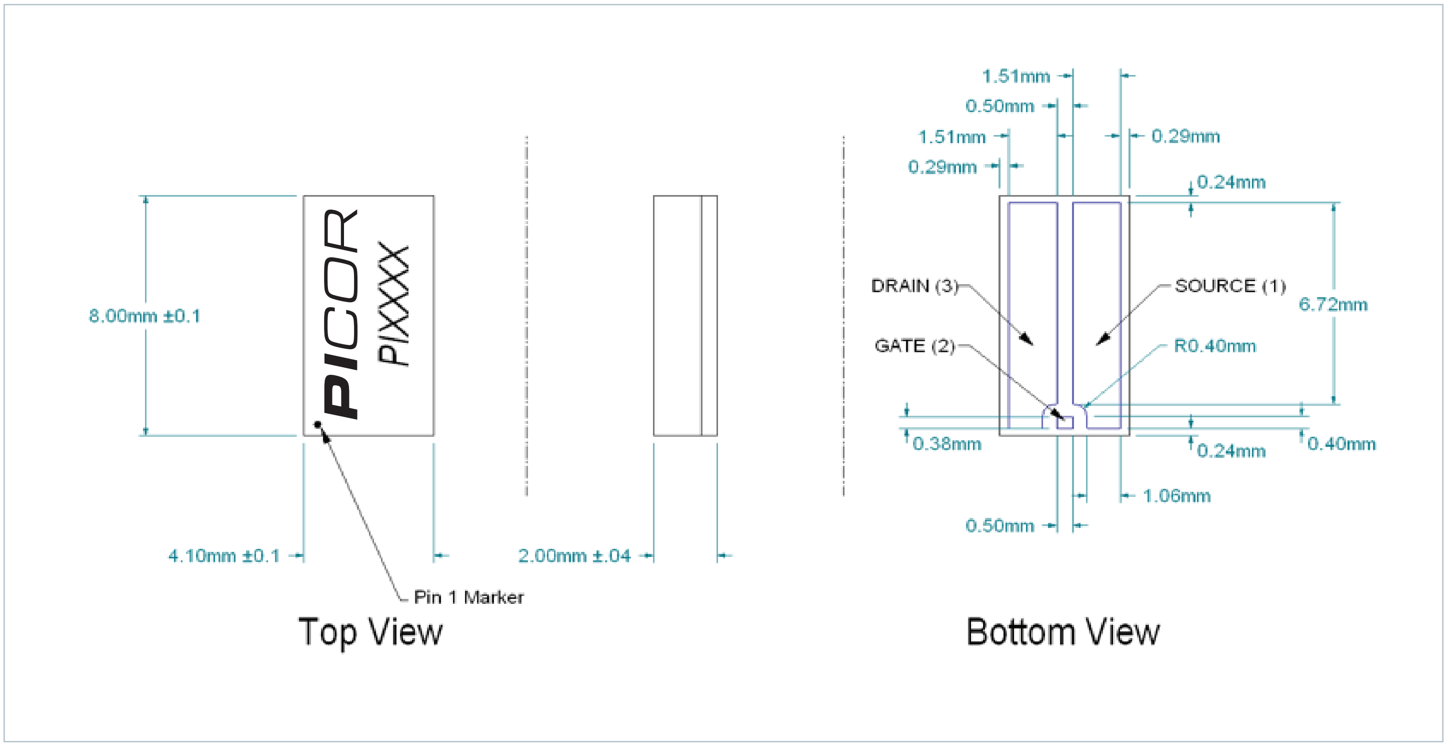
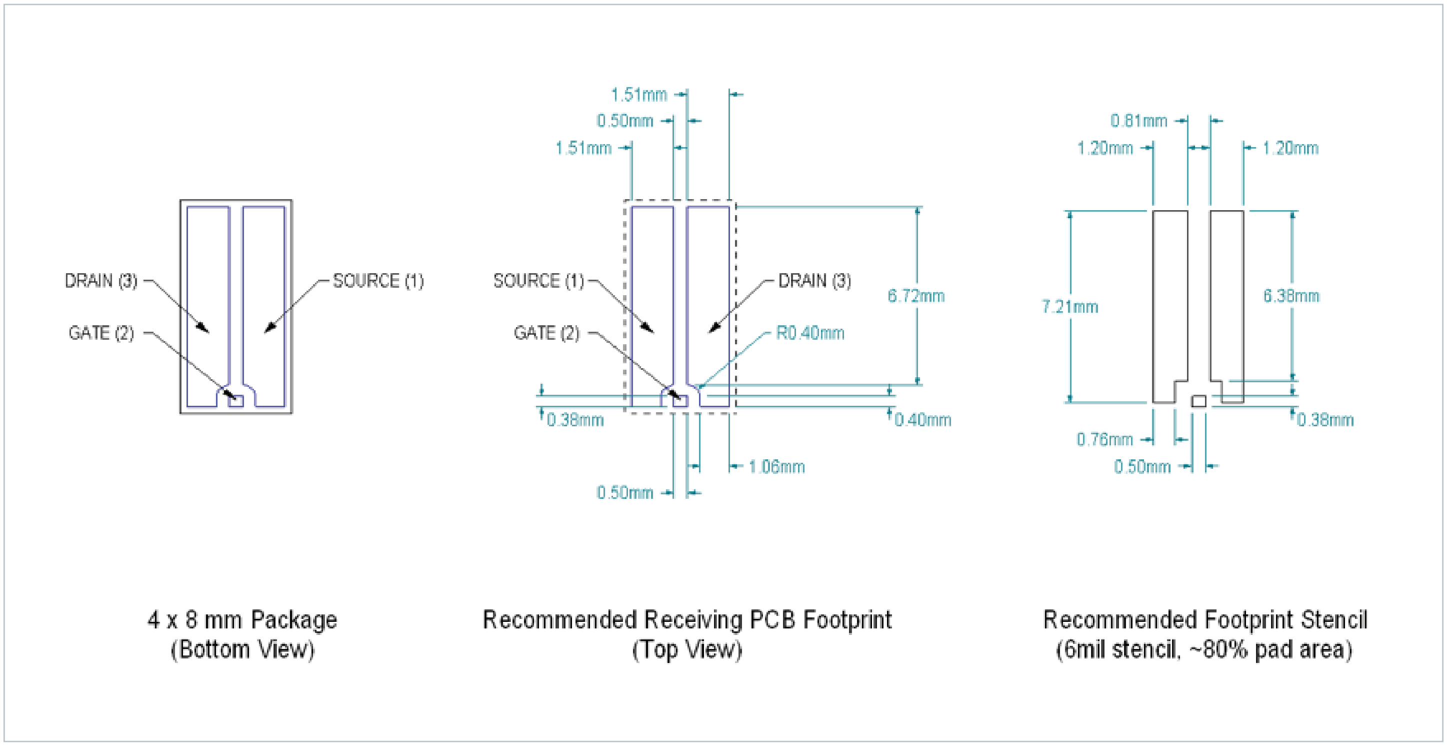


Figure 18 *— Example graphing of MOSFET junction temperature at* $I_D = 50\ A$ *and* $T_A = 70°C$

Package Drawing



Layout Recommendation



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