

PHD110NQ03LT

N-channel TrenchMOS™ logic level FET

Rev. 01 — 16 June 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Logic level threshold
- Low on-state resistance
- Low gate charge
- Surface mount package.

1.3 Applications

- Control FET in DC-to-DC converters
- Switched-mode power supplies.

1.4 Quick reference data

- $V_{DS} \leq 25 \text{ V}$
- $I_D \leq 75 \text{ A}$
- $P_{tot} \leq 115 \text{ W}$
- $R_{DS(on)} \leq 4.6 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT428 (D-PAK), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	<p style="text-align: center;">Top view MBK091</p> <p style="text-align: center;">SOT428 (D-PAK)</p>	<p style="text-align: center;">mbb076</p>
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

[1] It is not possible to make a connection to pin 2 of the SOT428 package.



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3. Ordering information

Table 2: Ordering information

Type number	Package		Version
	Name	Description	
PHD110NQ03LT	D-PAK	Plastic single-ended surface mounted package; 3 leads; one lead cropped	SOT428

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

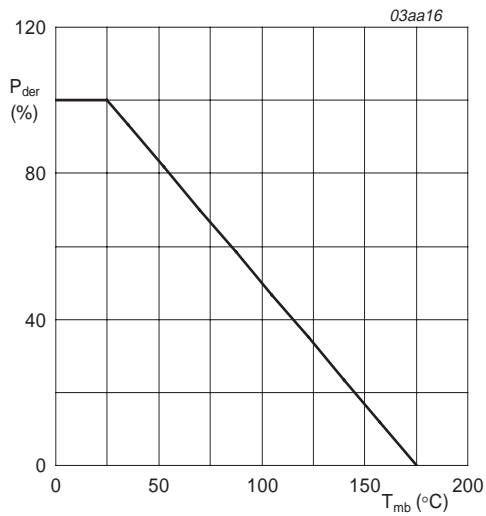
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	25	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2 and 3	-	75	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Figure 2	-	65	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	115	W
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C

Source-drain diode

I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	240	A

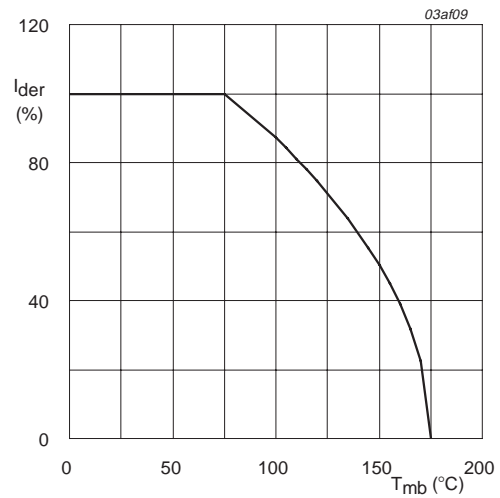
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 43\text{ A}$; $t_p = 0.25\text{ ms}$; $V_{DD} \leq 15\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; starting $T_j = 25\text{ °C}$	-	185	mJ
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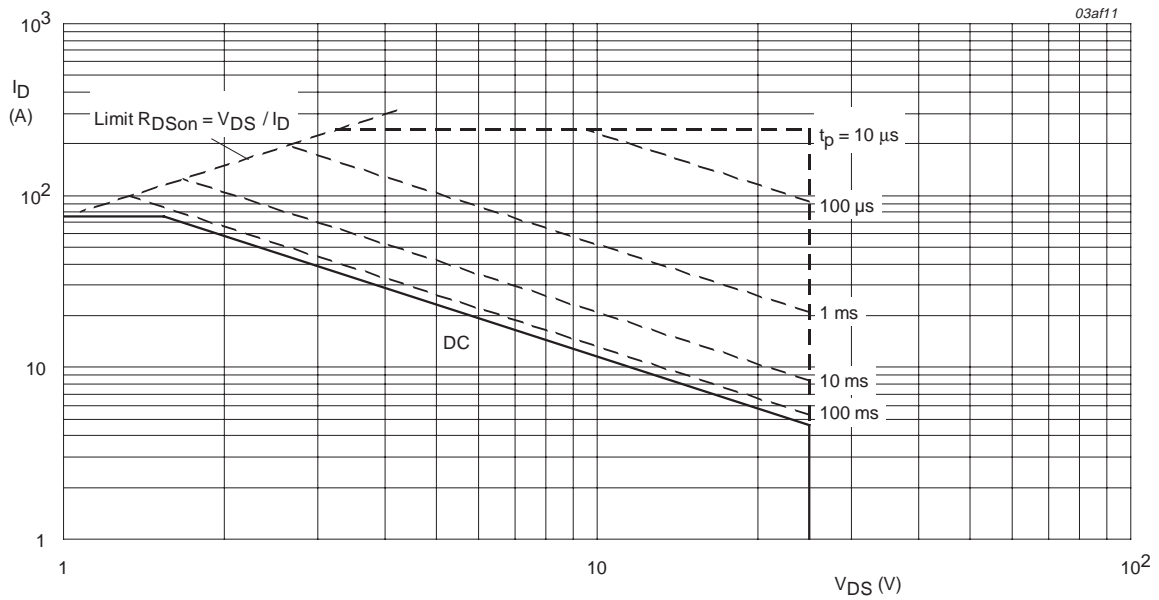
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	75	-	K/W

5.1 Transient thermal impedance

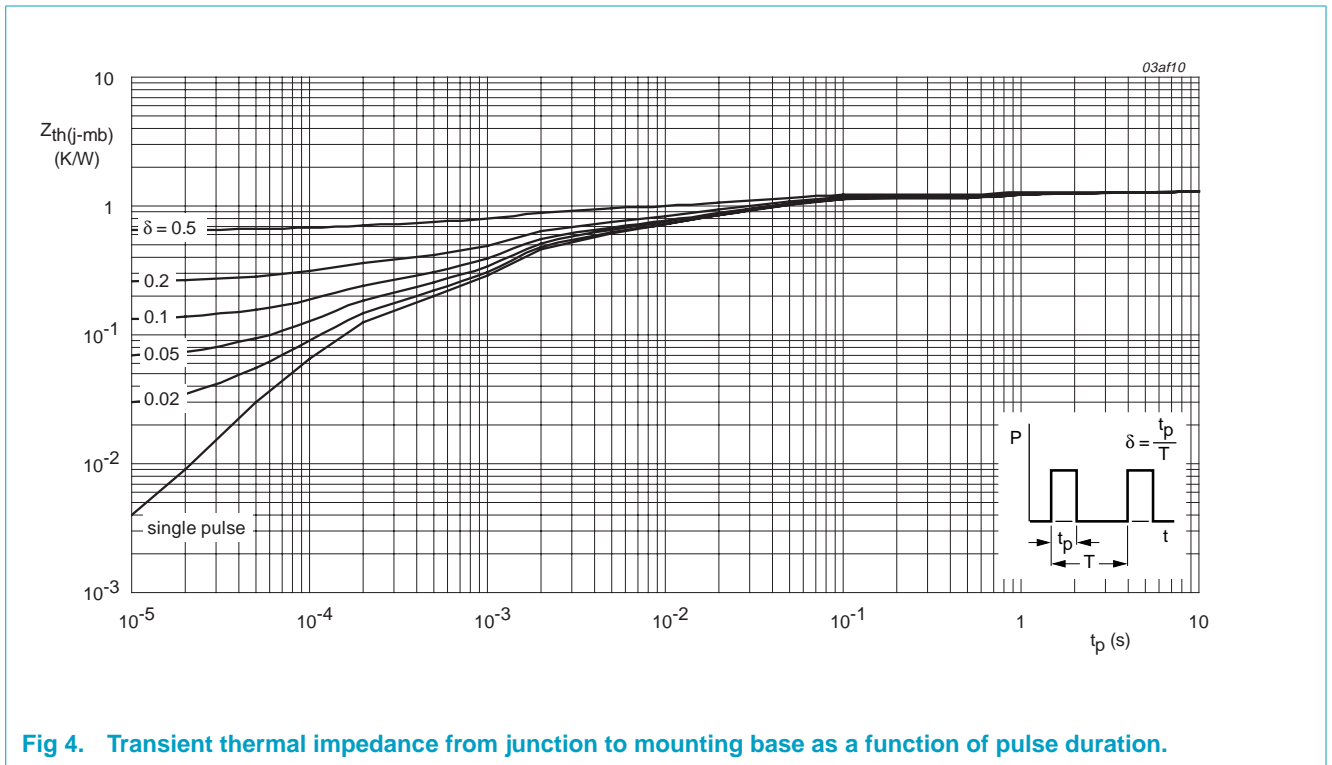


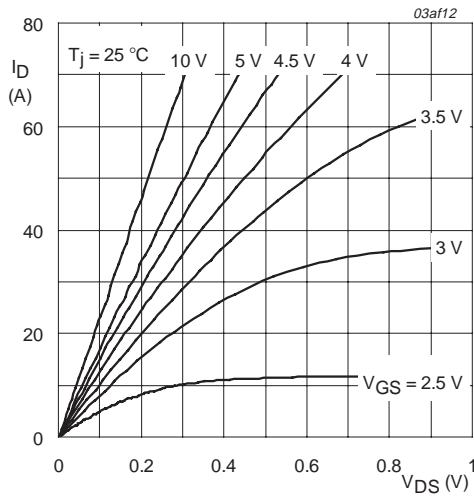
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

6. Characteristics

Table 5: Characteristics

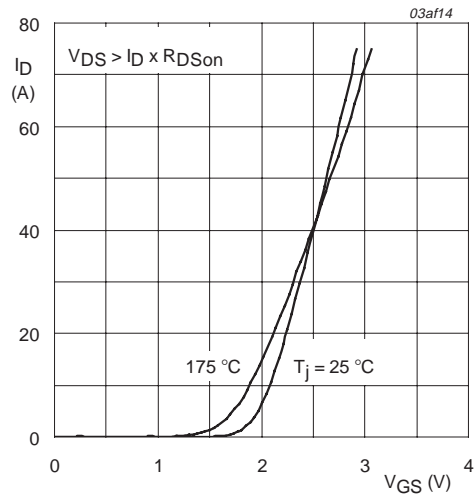
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = -55\text{ °C}$	25 22	- -	- -	V V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ \text{mA}$; $V_{DS} = V_{GS}$; Figure 9 $T_j = 25\text{ °C}$ $T_j = 150\text{ °C}$ $T_j = -55\text{ °C}$	1 0.5 -	1.5 - -	2 - 2.2	V V V
I_{DSS}	drain-source leakage current	$V_{DS} = 25\ \text{V}$; $V_{GS} = 0\ \text{V}$ $T_j = 25\text{ °C}$ $T_j = 175\text{ °C}$	- - -	0.05 - -	1 500	μA μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8 $T_j = 25\text{ °C}$ $T_j = 175\text{ °C}$ $V_{GS} = 10\ \text{V}$; $I_D = 25\ \text{A}$; Figure 7 and 8	- - -	5.3 8.3 3.9	6.2 11.2 4.6	m Ω m Ω m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 50\ \text{A}$; $V_{DD} = 15\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	26.7	-	nC
Q_{gs}	gate-source charge		-	8.5	-	nC
Q_{gd}	gate-drain (Miller) charge		-	8.4	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\ \text{V}$; $V_{DS} = 25\ \text{V}$; $f = 1\ \text{MHz}$; Figure 11	-	2200	-	pF
C_{oss}	output capacitance		-	725	-	pF
C_{rss}	reverse transfer capacitance		-	290	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$; $I_D = 12.5\ \text{A}$; $V_{GS} = 5\ \text{V}$; $R_G = 5.6\ \Omega$	-	18	-	ns
t_r	rise time		-	70	-	ns
$t_{d(off)}$	turn-off delay time		-	75	-	ns
t_f	fall time		-	70	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 25\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\ \text{A}$; $dI_S/dt = -100\ \text{A}/\mu\text{s}$; $V_{GS} = 0\ \text{V}$	-	43	-	ns
Q_r	recovered charge		-	40	-	nC



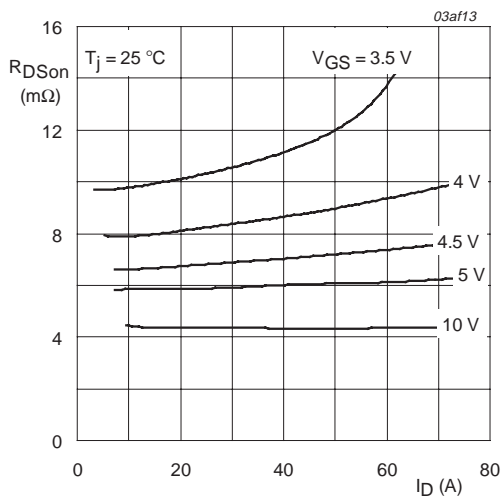
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



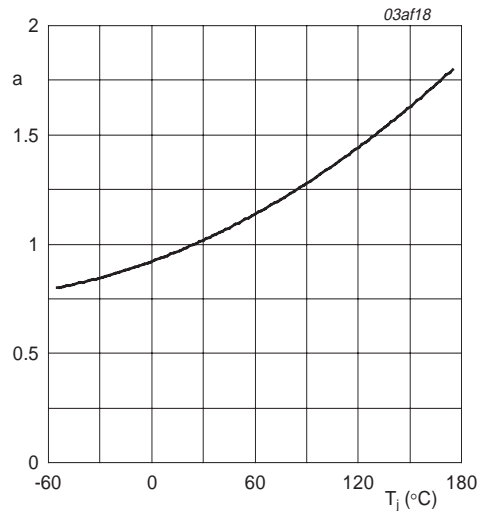
$T_j = 25\text{ }^\circ\text{C}$ and $175\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



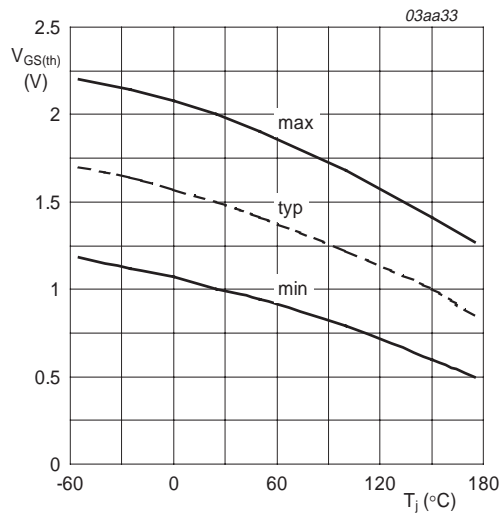
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



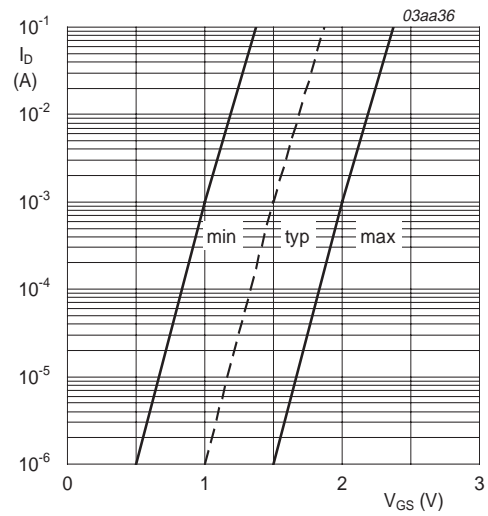
$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



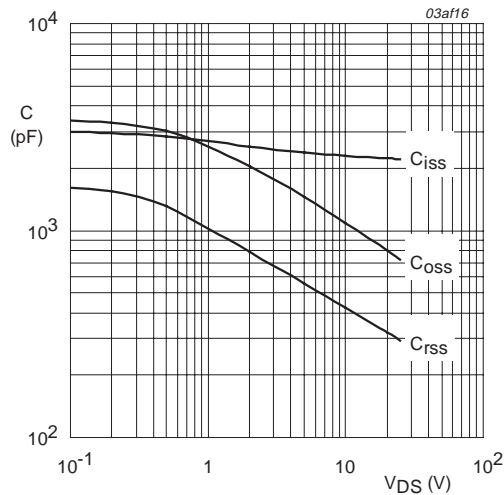
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



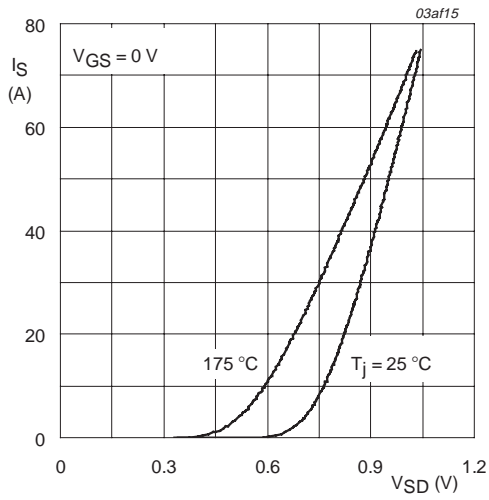
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



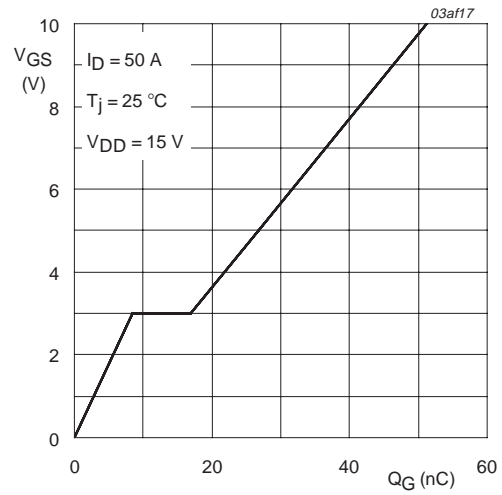
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ °C}$ and 175 °C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 50\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

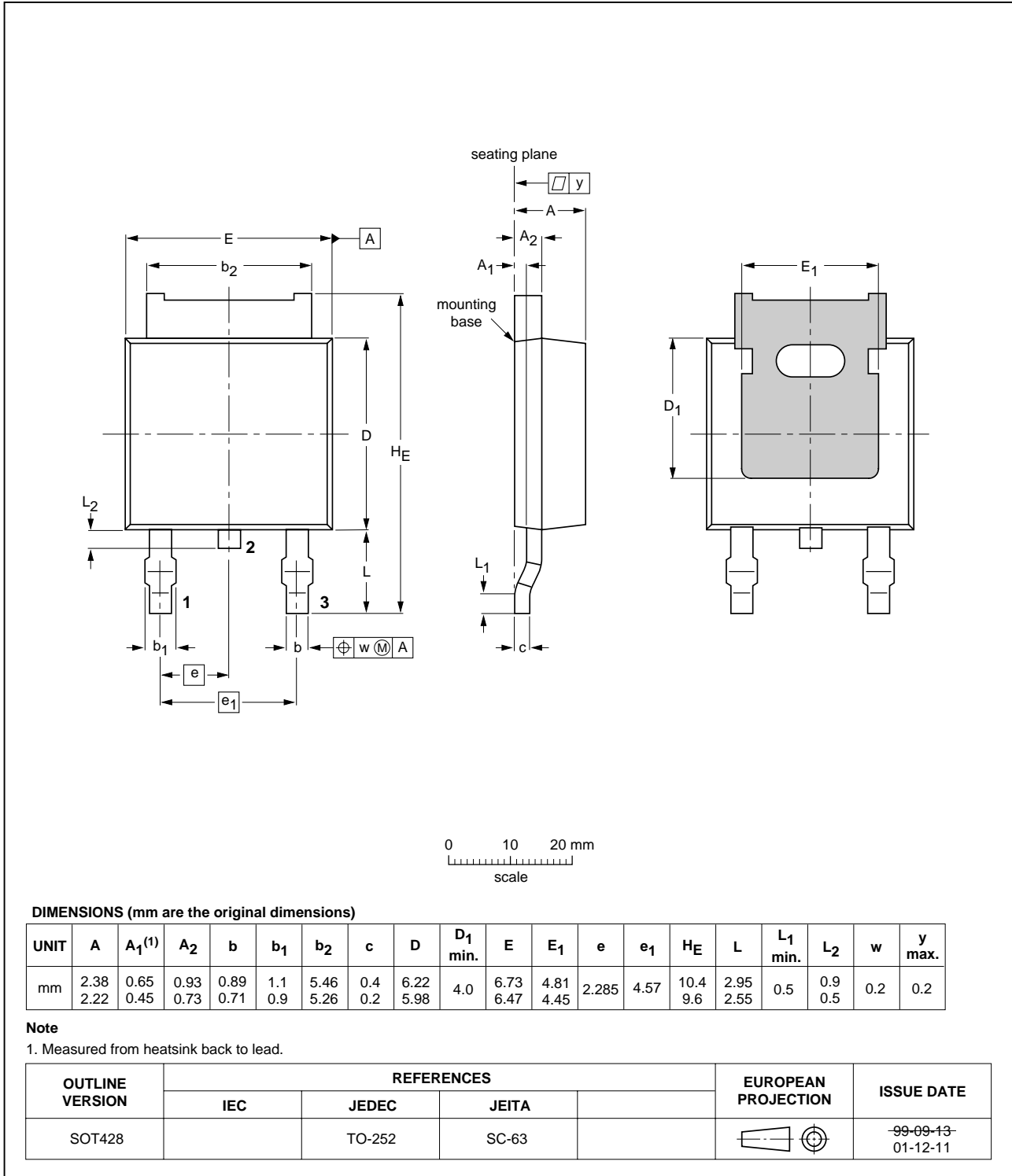


Fig 14. SOT428 (D-PAK).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20040616	-	Product data (9397 750 13468)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers	11
12	Trademarks	11

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