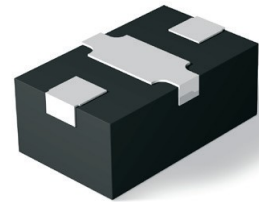


Features

- Supports up to 20 W Power
- Low Insertion Loss 0.5 dB @ 10 GHz
- High Isolation 40 dB @ 3 GHz
- RoHS* Compliant

Description

The MSWSS-040-30 is a surface mount medium power series shunt switch. The shunt device has broad band high isolation. This device can be surface mounted onto a PC board to give a low insertion loss and high Isolation switch. The device can handle up to 20 watts of power. Hot switching will depend on the speed of switch driver.



(2012) Non-Hermetic

Electrical Specifications: $T_A = +25^\circ\text{C}$

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage	$I_R = 10 \text{ mA}$	V	500	—	—
Reverse Current	$V_B = 80 \text{ V}$	nA	—	—	100
Forward Voltage	$I_F = 100 \text{ mA}$	V	—	900	—
Junction Capacitance	$V_R = 10 \text{ V}$, 1 MHz Shunt Series	pF	—	0.15 0.15	—
Series Resistance	$I_F = 100 \text{ mA}$, 100 MHz Shunt Series	Ω	—	0.8 0.8	1.0 1.0
Lifetime	$I_F = 10 \text{ mA}$, $I_R = 6 \text{ mA}$, 50% Shunt Series	ns	—	2200 1500	—
I-Region	Shunt Series	μm	—	80 80	—
Insertion Loss	$I = -50 \text{ mA}$ $F = <8 \text{ GHz}$ $F = <3 \text{ GHz}$	dB	—	0.15 0.3	0.3 0.5
Isolation	$I = -50 \text{ mA}$ $F = <8 \text{ GHz}$ $F = <3 \text{ GHz}$	dB	35 25	45 30	—
Return Loss	$I = -50 \text{ mA}$ $F = <8 \text{ GHz}$	dB	23	28	—

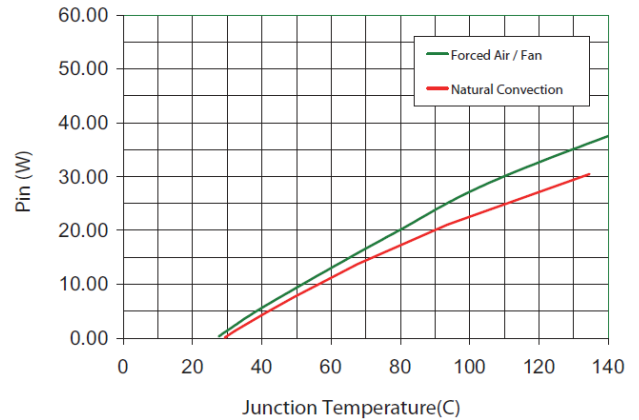
* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Absolute Maximum Ratings^{3,4}

Parameter	Absolute Maximum
Breakdown Voltage	500 V
Forward Current	500 mA
Thermal Resistance	30 W CW
Junction Temperature	+150°C
Storage Temperature	-65°C to +125°C
Solder Temperature	+260°C per JEDEC STD-J-20C

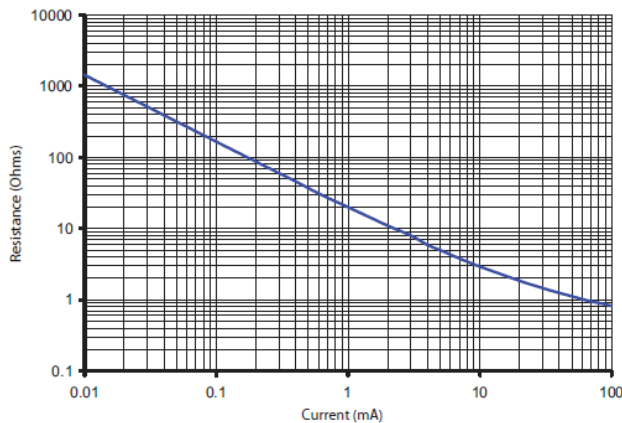
- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.

Input Power vs. Junction Temperature (mounted on heat sink @ 25°C, 1.3 GHz)

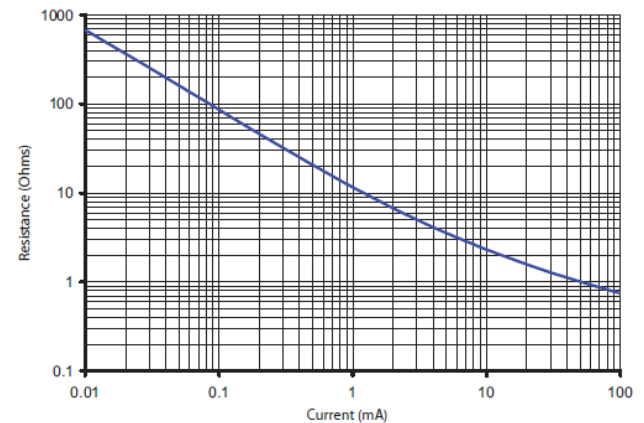


Typical Performance Curves @ +25°C

Resistance vs. Current Series Diode

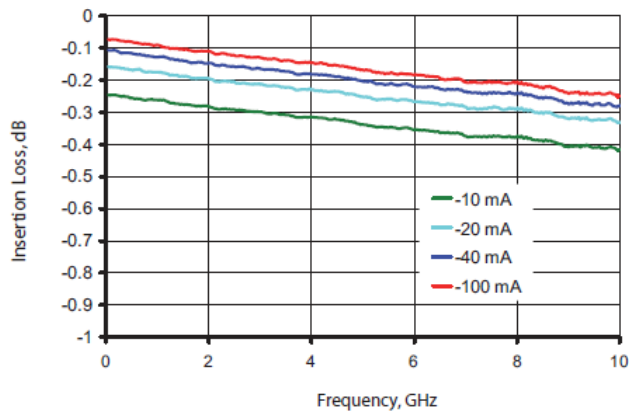


Resistance vs. Current Shunt Diode

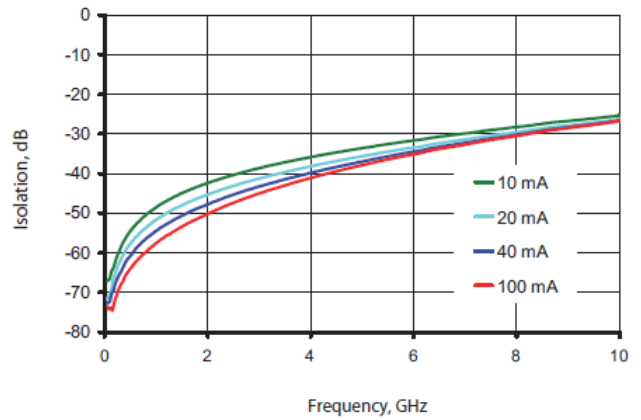


Typical Performance Curves @ +25°C

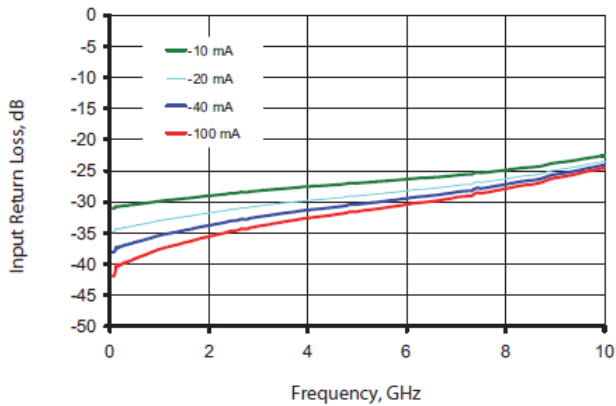
Insertion Loss



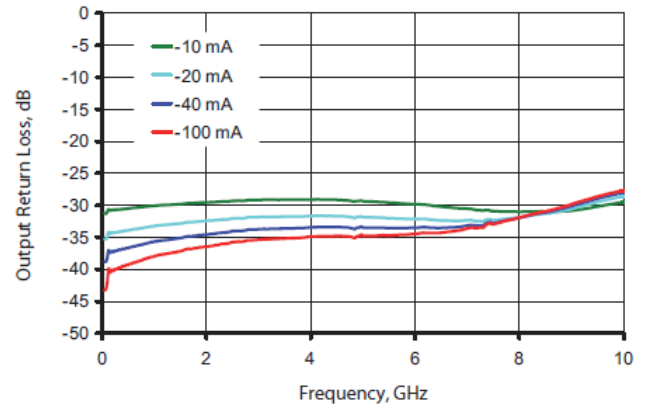
Isolation



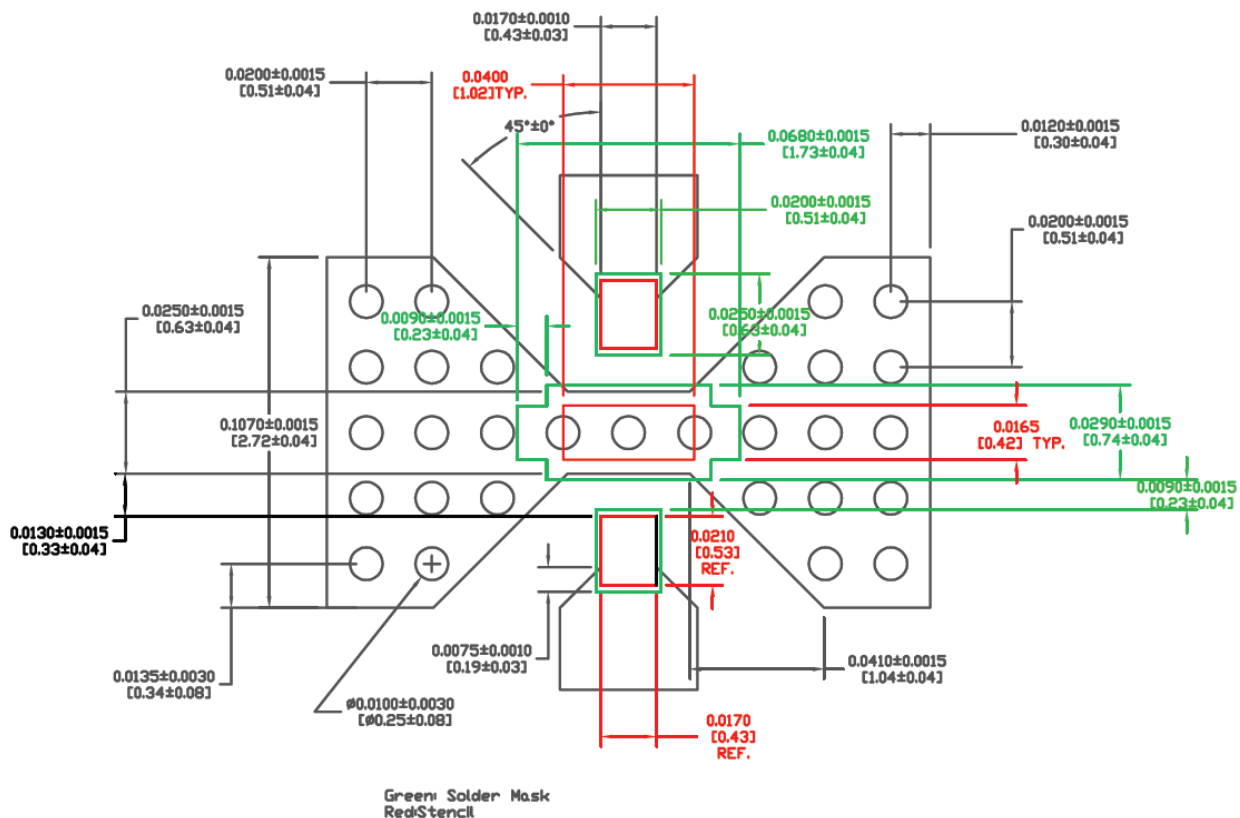
Input Return Loss



Output Return Loss



Printed Circuit Board Layout



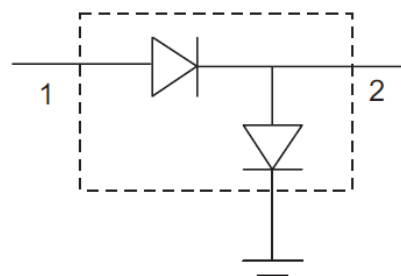
Assembly

If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.

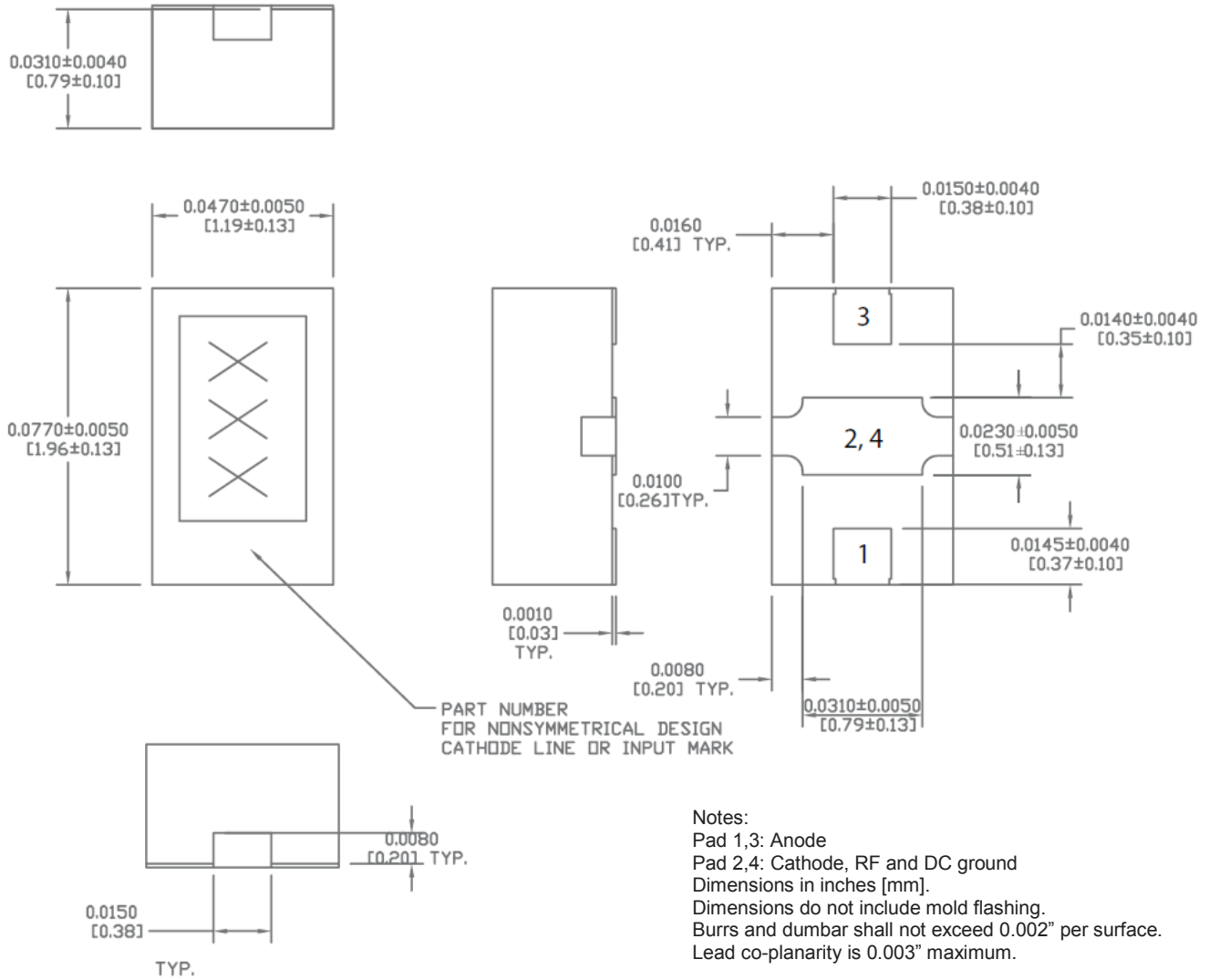
Solder mask should provide a 60 µm clearance between copper pad and solder mask underneath package and 125 µm clearance on outside edges of package. Rounded package pads should have matching rounded solder mask openings.

Use circles or squares for the thermal land stencil such that there is only 50% to 80% solder paste coverage.

Electrical Schematic



Outline: 2012 (molded plastic DFN)



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