19-3949 Rev 0; 4/06

EVALUATION KIT AVAILABLE

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

General Description

The MAX8723 is a high-efficiency, switch-mode, step-down regulator with a 14V internal power switch. With only a few external passive components, this low-cost regulator can generate a fixed 3.3V or adjustable DC output voltage of 2.0V to 3.6V of 2.0V to 3.6V (dual mode) from a 6V to 13.2V DC source. The 13.2V input voltage range makes this part ideal for LCD displays, point-of-load regulators, and other 8/12V-powered industrial equipment applications.

The MAX8723 can deliver up to 2A. It features an internal power MOSFET, a built-in bootstrap diode for its MOSFET driver, and an interface for an external synchronous rectifier MOSFET drive to replace the Schottky diode and improve efficiency. Its fixed-frequency PWM/skip-mode operation and current-mode control architecture provide fast load-transient response without compensation. The switching frequency is a pin-selectable 500kHz, 1MHz, or 1.5MHz, minimizing the size of external components.

The MAX8723 has built-in soft-start, current-limit, thermal-shutdown, and timer-delayed output-fault shutdown functions. The soft-start function limits inrush current during startup, avoiding transients that can trigger front-end protection circuits and lock up the system. The current limit, thermal-shutdown, and timer-delayed output-fault shutdown functions protect the power supply against fault conditions.

The MAX8723 also includes a linear regulator (VL), which provides a fixed 5V output (25mA) to support small external loads. The reference output is high-precision (2V ± 1%) and can also supply small external load currents.

The MAX8723 is available in the 16-pin 4mm x 4mm thin QFN package.

Applications

LCD TVs

LCD Monitors

Digital System Power Supplies

Point-of-Load Regulators

8/12V Industrial Equipment

Pin Configuration appears at end of data sheet.

Features

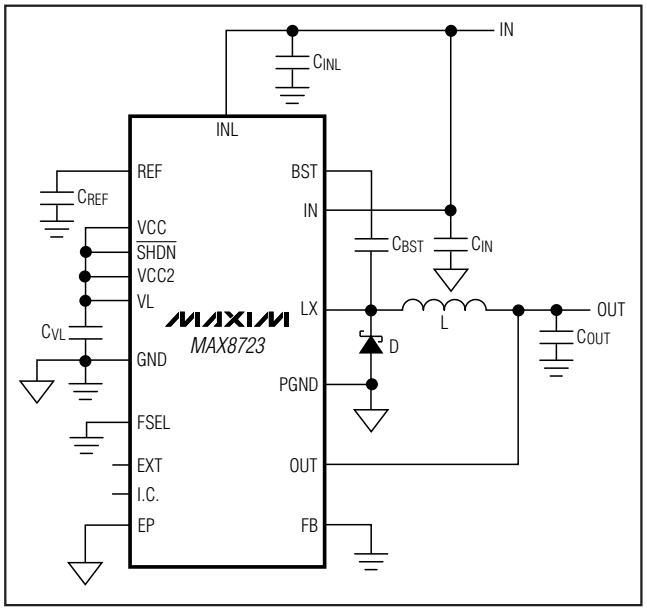
- **6V to 13.2V Input Supply Range**
- **Integrated 14V 2A n-Channel MOSFET Switch**
- **Preset 1.5% Accurate 3.3V Fixed Output Voltage or 2.0V to 3.6V Adjustable Output (Dual Mode)**
- **Current-Mode PWM Operation**
- **Frequency-Selectable 500kHz/1MHz/1.5MHz**
- **Internal 5V Linear Regulator Supports Up to 25mA External Load**
- **2V Precision Reference (1%)**
- **Integrated Bootstrap Diode for High-Side MOSFET Drive**
- **External Synchronous Rectifier Driver**
- **Built-In Soft-Start**
- **200µA Standby Mode**
- **Timer-Delayed Output Fault Protection**
- **Thermal Shutdown Protection**
- **Small 16-Pin 4mm x 4mm Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8723ETE+	-40°C to +85°C	16-pin Thin QFN 4mm x 4mm	T1644-4

+Denotes lead-free package.

Simplified Operating Circuit



Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

ABSOLUTE MAXIMUM RATINGS

IN, INL to GND .....-0.3V to +14V
SHDN, VCC2, OUT, VL, VCC, I.C. to GND.....-0.3V to +6V
FB, FSEL, REF to GND.....-0.3V to VCC + 0.3V
EXT to GND.....-0.3V to VL + 0.3V
GND to PGND .....-0.3V to +0.3V
BST to GND.....-0.3V to +20V
LX to BST.....-6V to +0.3V
LX to GND.....-0.3V to IN + 0.3V
VL Short Circuit to GND.....Momentary
RMS LX Current 1.6A
Continuous Power Dissipation (T_A = +70°C)
16-Pin 4mm x 4mm Thin QFN
(derated 25mW/°C above +70°C).....2000mW
Operating Temperature Extended.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = +3.3V, PGND = GND = 0, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, INL Input Voltage Range		6.0		13.2	V
INL Quiescent Current	FB = 1.8V, EXT unconnected		6	12	mA
INL Standby Supply Current	V_{INL} = 6V to 13.2V, SHDN = GND			0.5	mA
Operating Frequency	FSEL = GND	1275	1500	1725	kHz
	FSEL = VCC	850	1000	1150	
	FSEL = REF	425	500	590	
VL REGULATOR					
VL Output Voltage	6V < V_{INL} < 13.2V, V_{FB} = 1.8V, EXT unconnected, I_{VL} = 25mA	4.9	5.0	5.1	V
VL Undervoltage Lockout Threshold	VL rising, hysteresis = 2.5%	3.6	4.0	4.4	V
REFERENCE					
REF Output Voltage	No external load	1.98	2.00	2.02	V
REF Load Regulation	0 < I_{LOAD} < 50µA			10	mV
REF Sink Current	In regulation	10			µA
REF Undervoltage Lockout Threshold	Rising edge		1.5		V
	Falling edge		1.3		
STEP-DOWN REGULATOR					
OUT Voltage in Fixed Mode	V_{IN} = 6.0V to 13.2V, I_{OUT} = 0.5A (Note 1)	3.25	3.30	3.35	V
FB Voltage in Adjustable Mode	Duty cycle = 20% to 35%, I_{OUT} = 0.5A (Note 1)	1.97	2.00	2.03	V
FB Adjustable-Mode Threshold Voltage	Dual-mode comparator	0.10	0.15	0.20	V
Output Voltage Adjust Range		2.0		3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = +3.3V, PGND = GND = 0, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Step-Down Regulator Fault Trip Level	3.3V fixed mode, OUT falling		2.640		V
	FB adjustable mode, FB falling	1.536	1.600	1.664	
FB Input Bias Current	V_{FB} = 2.0V	50	125	200	nA
Low-Frequency Operation OUT Threshold			1.3		V
Low-Frequency Operation Switching Frequency	FSEL = GND		250		kHz
	FSEL = VCC		167		
	FSEL = REF		83		
DC Load Regulation	0 < I_{OUT} < 2A		0.5		%
DC Line Regulation	6V <V_{IN} <13.2V		0.1		%/V
LX-to-IN Switch On-Resistance			200	300	mΩ
LX-to-GND Switch On-Resistance		10	20	30	Ω
LX Current Limit		2.40	2.75	3.10	A
Soft-Start Ramp Time			1.7		ms
Maximum Duty Cycle		65	73	80	%
EXTERNAL FET DRIVER					
EXT On-Resistance	Sourcing or sinking		2	5	Ω
EXT Output Driver Current	Sourcing or sinking, EXT = VCC/2	0.5	1		A
LOGIC AND I/O CONTROL					
$\overline{SHDN}$, Input Voltage Low				0.4	V
$\overline{SHDN}$, Input Voltage High		2			V
$\overline{SHDN}$, Input Current				1	µA
SWITCHING FREQUENCY SELECTION					
FSEL Input Levels	FSEL = VCC (1MHz)	VCC - 0.4			V
	FSEL = REF (0.5MHz)	1.6		2.4	
	FSEL = GND (1.5MHz)			0.5	
FSEL Input Current	Forced to VL		10		µA
FAULT DETECTION					
Duration to Trigger Fault			50		ms
Thermal Shutdown Threshold	Typical hysteresis = 15°C		+160		°C

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = +3.3V, PGND = GND = 0, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL					
IN, INL Input Voltage Range		6.0		13.2	V
INL Quiescent Current	FB = 1.8V, EXT unconnected			12	mA
INL Standby Supply Current	V_{INL} = 6V to 13.2V, $\overline{SHDN}$ = GND			0.5	mA
Operating Frequency	FSEL = GND	1275		1725	kHz
	FSEL = VCC	850		1150	
	FSEL = REF	425		590	
VL REGULATOR					
VL Output Voltage	6V < V_{INL} < 13.2V, V_{FB} = 1.8V, EXT unconnected, I_{VL} = 25mA	4.9		5.1	V
VL Undervoltage Lockout Threshold	VL rising, hysteresis = 2.5%	3.6		4.4	V
REFERENCE					
REF Output Voltage	No external load	1.98		2.02	V
REF Load Regulation	0 < I_{LOAD} < 50µA			10	mV
STEP-DOWN REGULATOR					
OUT Voltage in Fixed Mode	V_{IN} = 6.0V to 13.2V, I_{OUT} = 0.5A (Note 1)	3.24		3.35	V
FB Voltage in Adjustable Mode	Duty cycle = 20% to 35%, I_{OUT} = 0.5A (Note 1)	1.97		2.03	V
Output Voltage Adjust Range		2.0		3.6	V
Step-Down Regulator Fault Trip Level	Falling edge	1.536		1.664	V
LX-to-IN Switch On-Resistance				300	mΩ
LX-to-GND Switch On-Resistance		9		30	Ω
Positive Current Limit		2.30		3.10	A
Maximum Duty Cycle		65		80	%
EXTERNAL FET DRIVER					
EXT On-Resistance	Sourcing or sinking			5	Ω
EXT Output Driver Current	Sourcing or sinking, EXT = VCC/2	0.5			A
LOGIC AND I/O CONTROL					
$\overline{SHDN}$, Input Voltage Low				0.4	V
$\overline{SHDN}$, Input Voltage High		2			V
SWITCH FREQUENCY SELECTION					
FSEL Input Levels	FSEL = VCC (1MHz)	VCC - 0.4			V
	FSEL = REF (0.5MHz)	1.6		2.4	V
	FSEL = GND (1.5MHz)			0.5	V

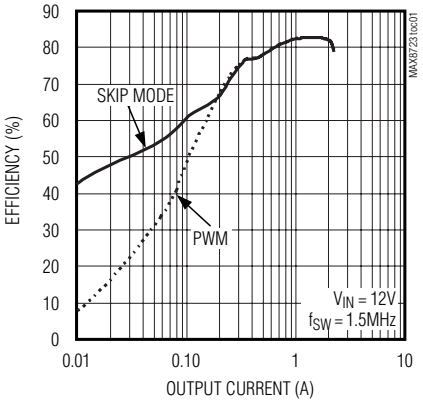
Note 1: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the output voltage ripple.

Note 2: Specifications to -40°C are guaranteed by design, not production tested.

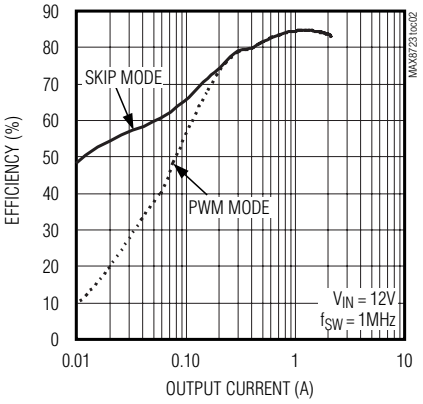
Typical Operating Characteristics

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

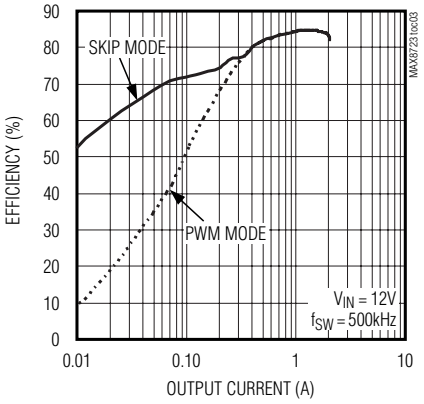
EFFICIENCY vs. LOAD CURRENT WITHOUT EXTERNAL SYNCHRONOUS RECTIFIER



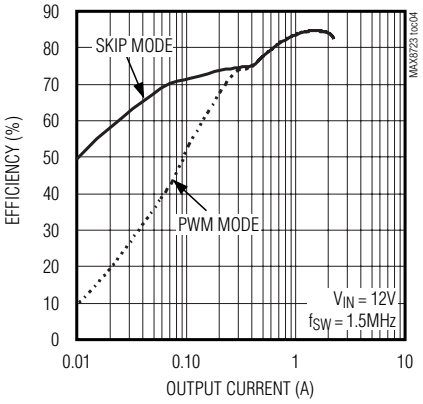
EFFICIENCY vs. LOAD CURRENT WITHOUT EXTERNAL SYNCHRONOUS RECTIFIER



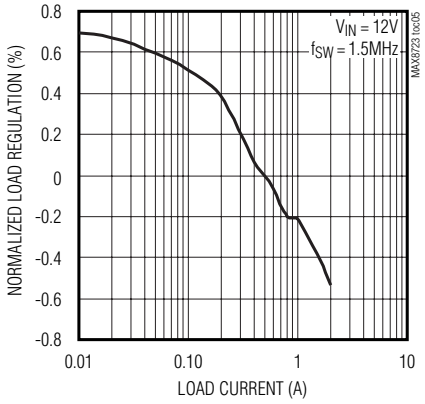
EFFICIENCY vs. LOAD CURRENT WITHOUT EXTERNAL SYNCHRONOUS RECTIFIER



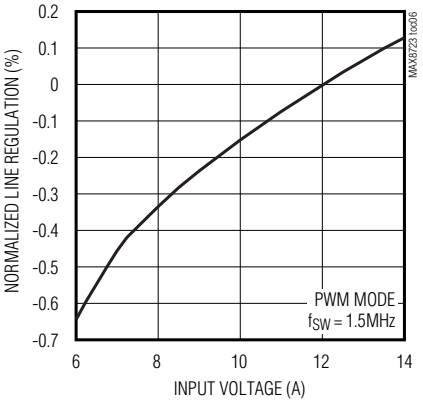
EFFICIENCY vs. LOAD CURRENT WITHOUT EXTERNAL SYNCHRONOUS RECTIFIER



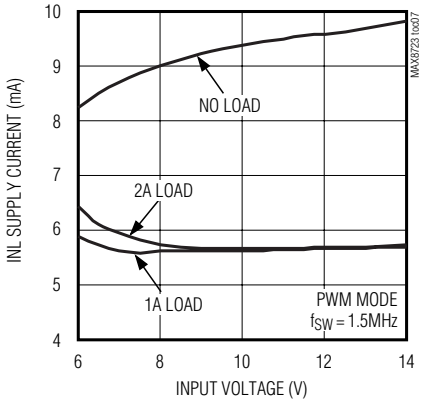
NORMALIZED LOAD REGULATION vs. LOAD CURRENT



NORMALIZED LINE REGULATION vs. INPUT VOLTAGE



INL SUPPLY CURRENT vs. INL VOLTAGE

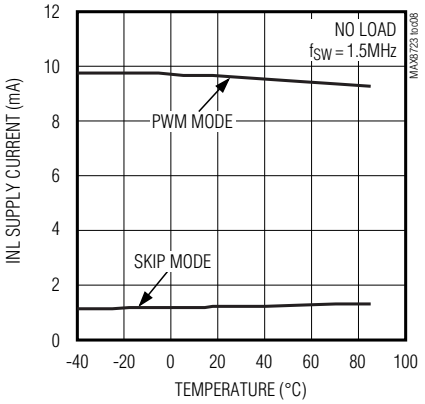


Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

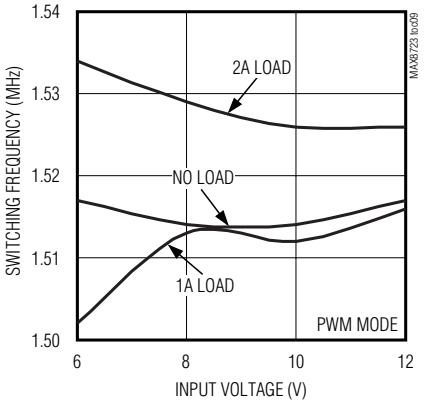
Typical Operating Characteristics (continued)

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

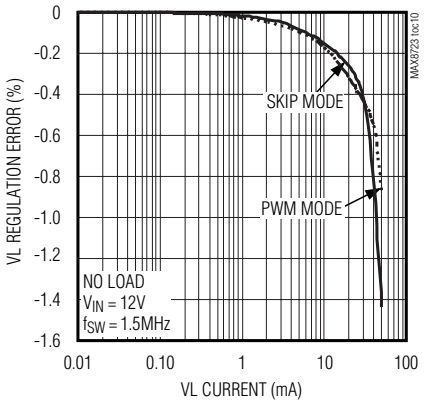
INL SUPPLY CURRENT vs. TEMPERATURE



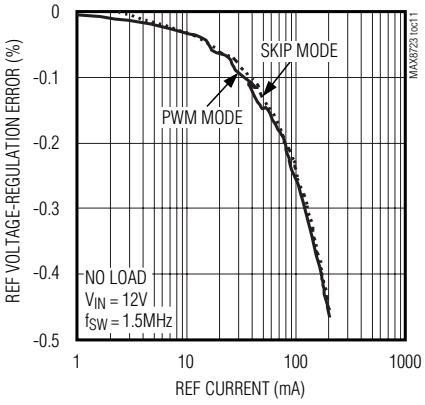
SWITCHING FREQUENCY vs. INPUT VOLTAGE



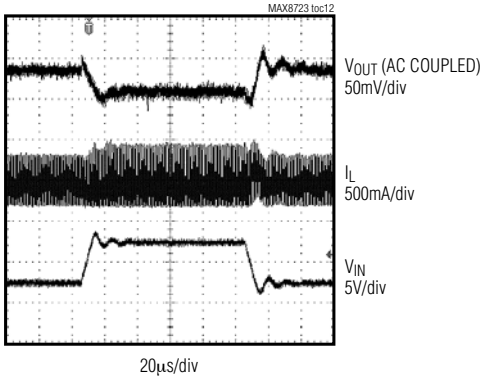
VL LOAD REGULATION



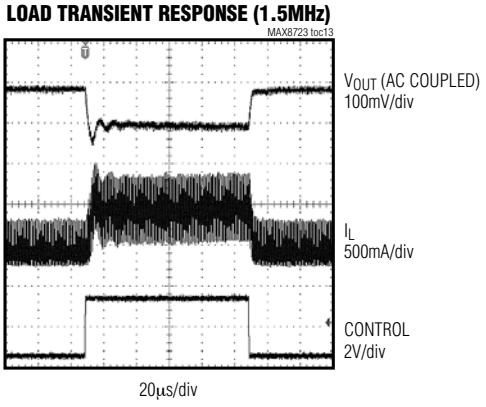
REFERENCE VOLTAGE REGULATION



LINE TRANSIENT RESPONSE



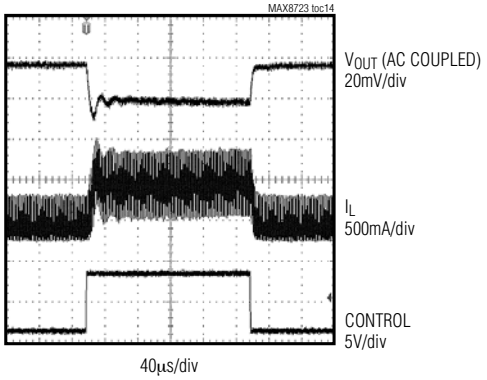
LOAD TRANSIENT RESPONSE (1.5MHz)



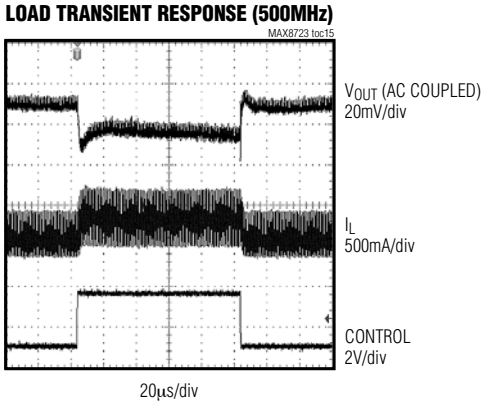
Typical Operating Characteristics (continued)

(Circuit of Figure 1 with 1.5MHz components of Table 1, unless otherwise specified. V_{IN} = V_{INL} = 12V, V_{OUT} = 3.3V, T_A = +25°C, unless otherwise noted.)

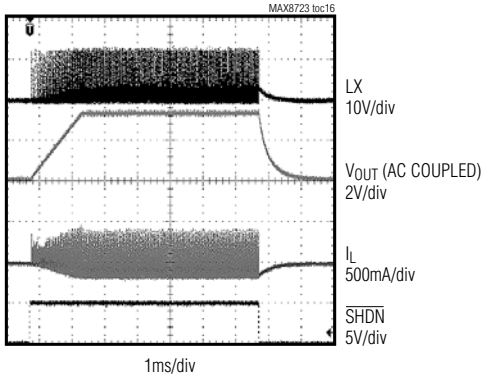
LOAD TRANSIENT RESPONSE (1.0MHz)



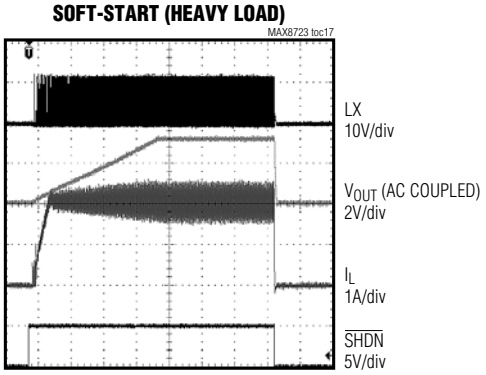
LOAD TRANSIENT RESPONSE (500MHz)



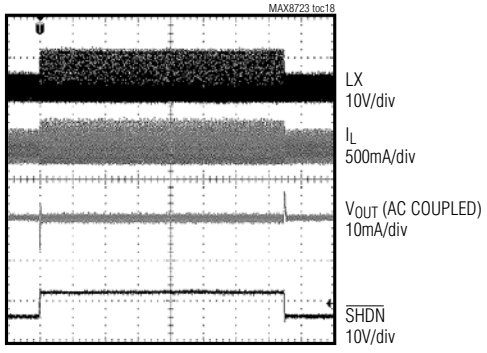
STEP-DOWN REGULATOR SOFT-START/SHUTDOWN



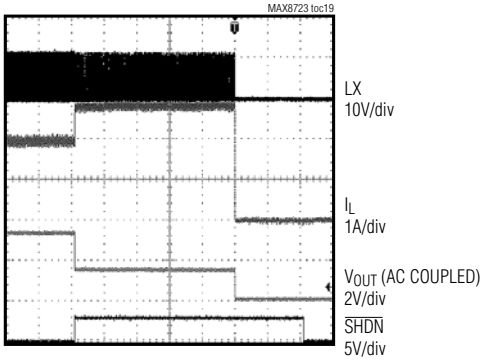
STEP-DOWN REGULATOR SOFT-START (HEAVY LOAD)



LINEAR REGULATOR VL LINE TRANSIENT RESPONSE



TIMER DELAY LATCH RESPONSE TO OVERLOAD



Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

Pin Description

PIN	NAME	FUNCTION
1	IN	Step-Down Regulator Input Voltage (6V to 13.2V). Bypass IN to PGND with a minimum 4.7µF ceramic capacitor close to the IC.
2	LX	Step-Down Regulator Inductor Connection. Internally connected to the junction of the internal high-side and low-side MOSFETs.
3	BST	Step-Down Regulator Bootstrap Capacitor Connection for High-Side Gate Driver. Connect a 0.1µF ceramic capacitor from BST to LX.
4	I.C.	Internal Connection. Make no connection to this pin.
5	OUT	Output Voltage-Sense Input and the Negative Input to the Current-Sense Amplifier. Connect OUT to the step-down regulator output.
6	FB	Step-Down Converter Feedback Input: 1) Connect FB to GND for a fixed 3.3V output. 2) Connect FB to the center tap of a resistive voltage-divider between the step-down regulator output and GND for an adjustable output from 2.0V to 3.6V.
7	PGND	Step-Down Regulator Power Ground
8	EXT	External Synchronous Rectifier Gate Driver Output. To use a synchronous rectifier (optional), connect EXT to the gate of the external MOSFET. EXT is low in shutdown.
9	INL	Internal 5V Linear Regulator Supply Input. Bypass INL to GND with a 0.22µF ceramic capacitor close to the IC.
10	VL	5V Internal Linear Regulator Output. Bypass VL to GND with a 1µF minimum ceramic capacitor. VL is enabled in shutdown and during faults. See the *Linear Regulator (VL)* section for further information.
11	VCC	Internal Reference Supply Input. Connect VCC to VL.
12	GND	Analog Ground
13	REF	Reference Output. Bypass REF to GND with 0.22µF ceramic capacitor.
14	FSEL	Switching Frequency Selection Input. This tri-level logic input sets the SMPS's switching frequency: FSEL = GND, f_{SW} = 1.5MHz FSEL = VCC, f_{SW} = 1.0MHz FSEL = REF, f_{SW} = 500kHz
15	$\overline{SHDN}$	Shutdown Control Input. When $\overline{SHDN}$ is low, the step-down regulator power output is disabled, but REF and VL remain on.
16	VCC2	Connect VCC to VL.
EP	EP	Exposed Backside Pad. For better thermal management, this pad should be soldered to an analog ground plane connected to sufficient copper through multiple vias.

Typical Operating Circuit

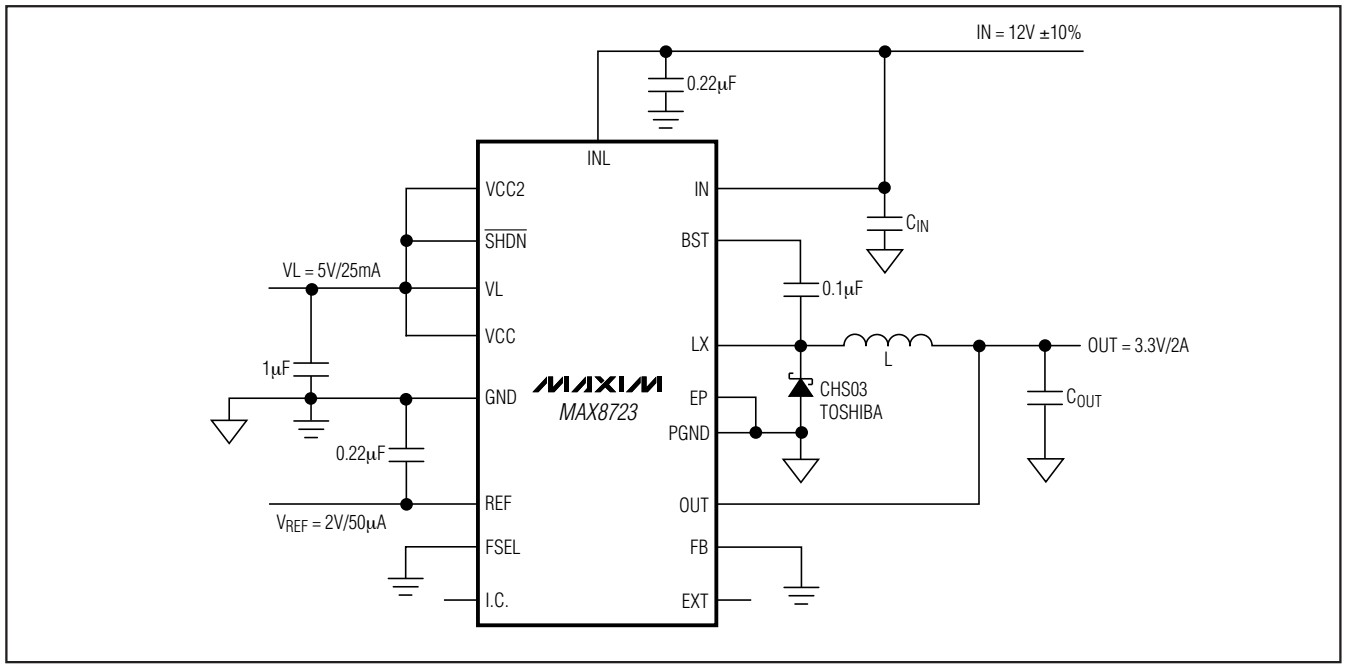


Figure 1. Typical Operating Circuit, Fixed 3.3V Output

The typical operating circuit (Figure 1) is a complete power supply that generates a +3.3V, 2A output from a 12V ±10% input. Tables 1 and 2 list the key components and the contact information for the respective suppliers. The inductor and capacitor component values showing in Figure 1 are for 1.5MHz switching frequency operation. For other operating frequencies (500kHz/1MHz), substitute these values with the ones from Table 1 corresponding to that frequency.

Table 1. Component Selection

FREQUENCY	500kHz	1MHz	1.5MHz
Inductor (L)	6.8µH	3.9µH	2.2µH, 3A Ferrite Sumida CDRH5018NP-2R2NC
Input Capacitors (C_{IN})	2 x 10µF, 16V ceramic	10µF, 16V ceramic	4.7µF, 16V ceramic TDK C2012X5R1C475K
Output Capacitor (C_{OUT})	2 x 47µF, 6.3V ceramic	47µF, 6.3V ceramic	22µF, 6.3V X5R ceramic TDK C2012X5R0J226M

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Fairchild Semiconductor	408-822-2000	408-822-2102	www.fairchildsemi.com
Sumida	847-545-6700	847-545-6720	www.sumida.com
TDK	847-803-6100	847-390-4405	www.component.tdk.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

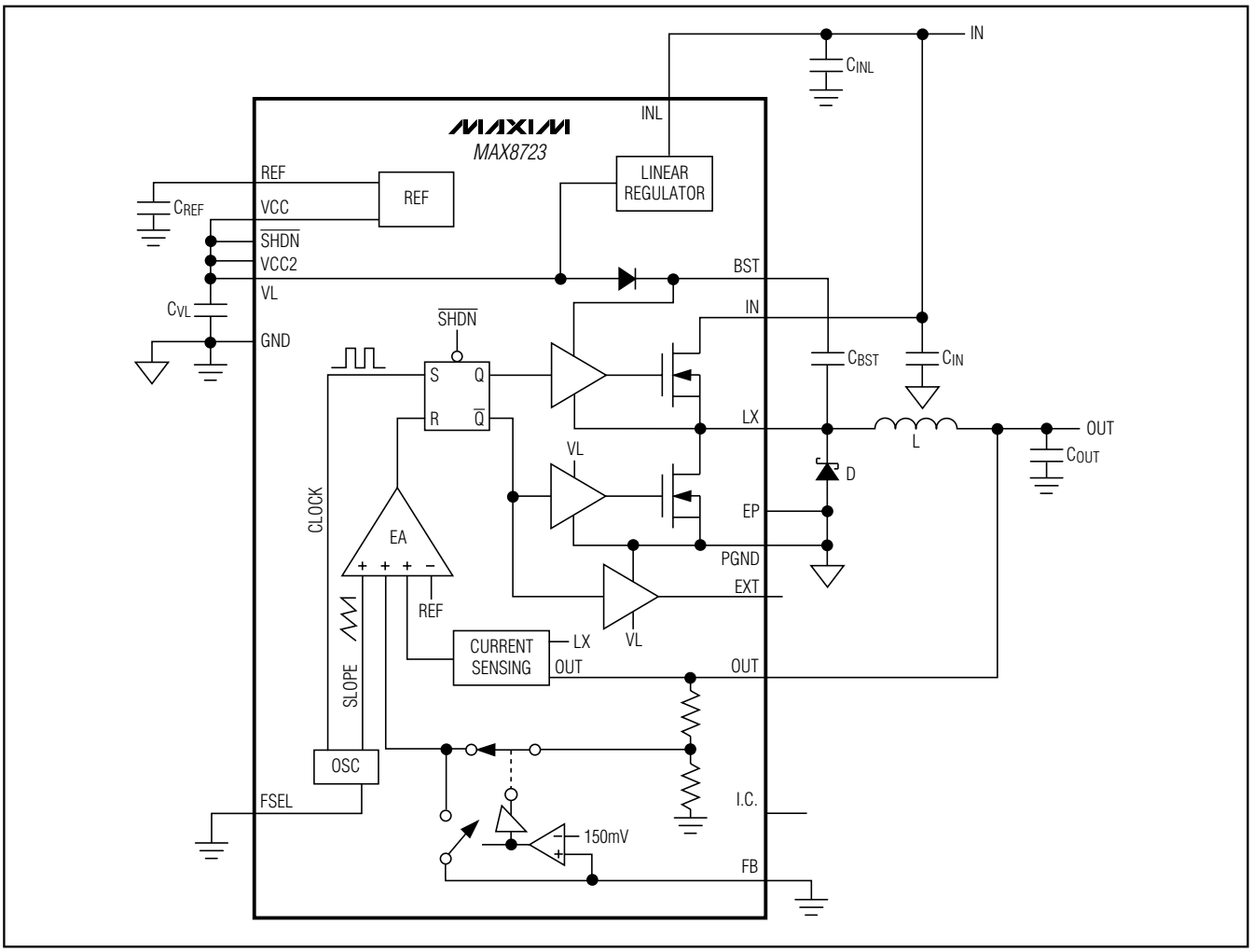


Figure 2. Functional Diagram

Detailed Description

The MAX8723 is a high-efficiency switching regulator designed primarily for TFT LCD display applications. It operates from 6V to 13.2V inputs and provides a fixed 3.3V or an adjustable output voltage. It can deliver up to 2A of load current. Although the MAX8723 is designed to supply power for logic control circuits used in TFT LCD monitors and TVs, it can be used to supply other logic control circuits as well.

The MAX8723 contains a step-down switching-regulator, which generates a fixed 3.3V or an adjustable output for the logic supply rail. The step-down switching-regulator features a fixed-frequency current-mode control architecture, digital soft-start, timer-delayed fault protection, and thermal-overload protection. An internal oscillator offers three pin-selectable frequency options (500kHz/1MHz/1.5MHz), allowing optimized designs based on the specific application requirements. In addition, the MAX8723 provides a 5V linear regulator output and a 2V reference output. Figure 2 shows the MAX8723 functional block diagram.

The step-down regulator consists of an internal n-channel MOSFET with gate driver, an internal inductor DC resistance-based current-sense network, a cycle-by-cycle current-limit comparator, and a PWM controller block. The external power stage consists of an inductor, input and output capacitors, and a freewheeling device, such as a Schottky diode rectifier or a MOSFET synchronous rectifier.

The output voltage is regulated by changing the duty cycle of the high-side MOSFET. A bootstrap circuit that uses a 0.1µF flying capacitor between LX and BST provides the supply voltage for the high-side gate driver. Although the MAX8723 also includes a low-side MOSFET (20Ω, typ), this switch is only used to charge the bootstrap capacitor during startup and maintain fixed-frequency operation at no load, or to sink a small amount load current. This MOSFET cannot be used as a synchronous rectifier; an external Schottky diode or MOSFET is required (Figure 1). If an external low-side MOSFET switch (driven by EXT) is used as a synchronous rectifier (Figure 3), the Schottky diode can be omitted or replaced by a smaller device for even greater efficiency.

PWM Controller Block

The heart of the PWM control block is a multi-input, open-loop comparator that sums three signals: the output voltage-feedback signal with respect to the reference voltage, the current-sense signal, and the slope compensation. The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

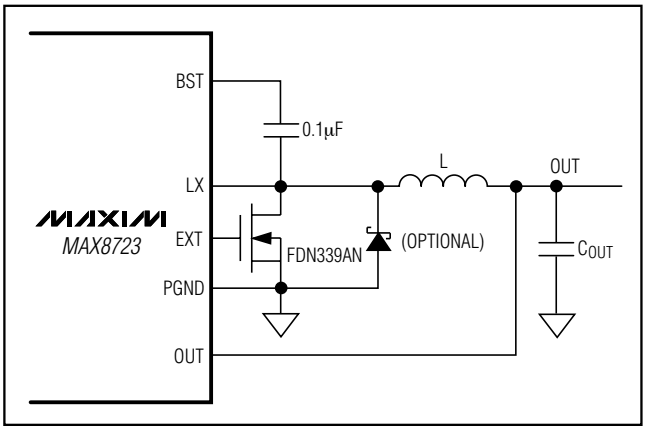


Figure 3. Optional Synchronous Rectifier External MOSFET

The PWM controller operates in a fixed-frequency mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch until the PWM comparator changes state. As the high-side switch turns off, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

Inductor DCR Current Sensing and Current Limiting

The MAX8723 employs a type of current-mode control. An internal sense network is built for this control method. The sense network derives a current-sense signal from the voltage across the inductor's DC resistance. This sensing method does not require additional external components, thus, is cost, space, and power efficient. The internal current-sense signal is AC-coupled into the PWM comparator, eliminating most DC output voltage variation under different load current.

The current-limit circuit turns off the high-side MOSFET switch whenever the voltage across the high-side MOSFET exceeds an internal voltage threshold that corresponds to an actual current of 2.75A (typ). This feature guarantees the safe operation of MAX8723 under various load conditions.

Soft-Start

To limit the inrush current during startup, the step-down regulator includes a 7-bit DAC that steps its internal reference voltage from 0 to 2V in 128 steps. The soft-start time is 1.7ms (typ) and FB fault detection is disabled during soft-start. See Waveforms in the *Typical Operating Characteristics* section.

Low-Frequency Operation

The step-down regulator of the MAX8723 enters low-frequency operating mode if the voltage on OUT is below 1.3V. In the low-frequency mode, the step-down regulator switching frequency drops to 1/6 of the oscillator frequency. This feature prevents potentially uncontrolled inductor current if OUT is overloaded or shorted to ground.

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

Dual-Mode Feedback

The step-down regulator of the MAX8723 supports both fixed output and adjustable output. Connect FB to GND to enable the 3.3V fixed-output voltage (Figure 1). Connect a resistive voltage-divider between OUT and GND with the center tap connected to FB to adjust the output voltage (Figure 4). Choose RB to be between 5kΩ and 50kΩ, and solve for RA using the equation:

$$RA = RB \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 2V, and V_{OUT} can vary from 2V to 3.6V.

Frequency Selection (FSEL)

The FSEL input selects the internal oscillator switching frequency. Table 3 shows the switching frequency based on the FSEL connection. High-frequency (1.5MHz) operation optimizes the application for the smallest component size, trading off efficiency because of higher switching losses. Low-frequency (500kHz) operation offers the best overall efficiency at the expense of component size and board space.

Table 3. Frequency Selection

FSEL	SWITCHING FREQUENCY (kHz)
GND	1500
VCC	1000
REF	500

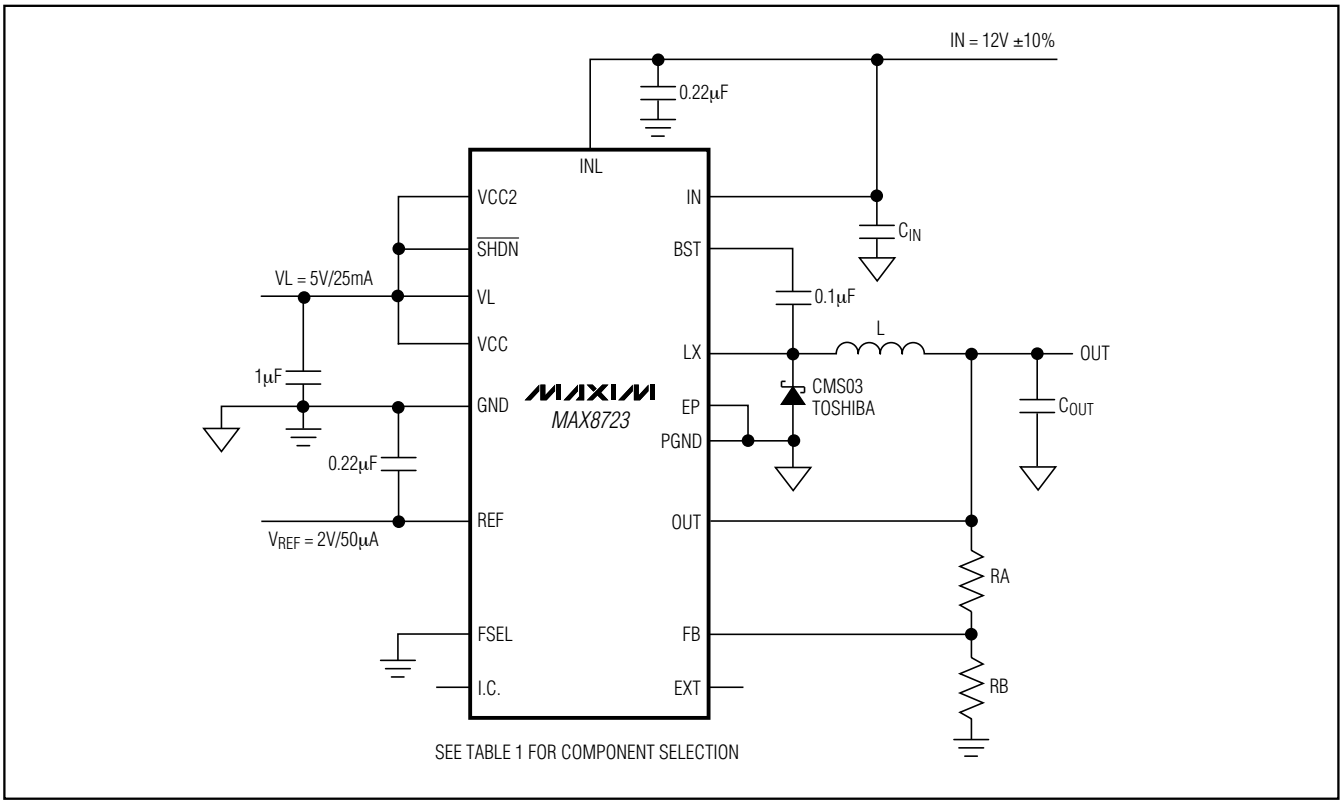


Figure 4. Typical Operating Circuit, Adjustable Output

Power Sequence Control

The linear regulator output VL is enabled when the MAX8723 input voltage rises high enough to lift VL above its undervoltage lockout (UVLO) threshold. When the reference voltage (REF) is above its UVLO threshold and $\overline{SHDN}$ is logic-high, the step-down regulator starts up. At this time, an internal reference voltage steps from zero to REF, making the output of the step-down converter gradually increase to its regulation point. This soft-start takes about 1.7ms and prevents large inrush currents. The FB undervoltage fault detection is blanked during the soft-start and is enabled after the step-down regulator reaches regulation.

The MAX8723 step-down regulator is disabled when $\overline{SHDN}$ is logic-low or when the fault protection latch is set.

Fault Protection

The MAX8723 monitors OUT (fixed-output mode) or FB (adjustable-output mode) for undervoltage conditions. During steady-state operation, if the voltage drops below 80% (typ) of the nominal regulation point, the MAX8723 activates an internal fault timer. If the fault persists longer than the fault timer duration (50ms, typ), the MAX8723 sets a fault latch, shutting down step-down regulator output. The linear regulator output VL and reference output REF remain active during output undervoltage faults. Once the fault condition is removed, toggle $\overline{SHDN}$ or cycle the input voltage to clear the fault latch and restart the step-down switching regulator.

Thermal-Overload Protection

The thermal-overload protection prevents excessive power dissipation from overheating the MAX8723. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates a fault-protection circuit, which shuts down OUT, allowing the device to cool down. Once the device cools down by approximately 15°C, the MAX8723 automatically restarts the step-down regulator. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Reference Voltage (REF)

The reference output is nominally 2V, and can source at least 50µA (see *Typical Operating Characteristics*). VCC is the supply input of the internal reference block. Bypass REF with a 0.22µF ceramic capacitor connected between REF and GND.

Linear Regulator (VL)

The MAX8723 includes an internal linear regulator (VL). INL is the supply input of the linear regulator and the input voltage range is between 6V and 13.2V. The VL output voltage is set to 5V. VL powers the internal MOSFET driver circuit, the external MOSFET driver circuit (if used), the PWM controller, and logic circuits. Through VCC, VL powers the internal reference, current-limit circuitry, and other sensitive blocks.

Bypass VL with at least a 1µF ceramic capacitor. VL can supply at least 25mA to external loads when bypassed with a 2.2µF ceramic capacitor. VL can supply power for on/off monitoring and remote-control receiver circuitry.

Design Procedure

Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of peak-to-peak inductor ripple current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple. A good compromise between size and losses is typically found at a 30% ripple current-to-load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times the DC load current:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{OUT(MAX)} \times LIR}$$

where $I_{OUT(MAX)}$ is the maximum DC load current, and the switching frequency f_{SW} is 1.5MHz when FSEL is tied to AGND, 1MHz when FSEL is tied to V_{CC}, and 500kHz when FSEL is tied to REF. The exact inductor value is not critical and can be adjusted to make tradeoffs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values reduce output ripple and improve efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels.

The inductor's saturation current must exceed the peak inductor current. The peak current can be calculated by:

$$I_{OUT\_RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}}$$

$$I_{OUT\_PEAK} = I_{OUT(MAX)} + \frac{I_{OUT\_RIPPLE}}{2}$$

The inductor's DC resistance should be low for good efficiency. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. Shielded-core geometries help keep noise, EMI, and switching waveform jitter low.

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

Input Capacitors

The input filter capacitors reduce peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the regulator's switching. They are usually selected according to input ripple current requirements and voltage rating, rather than capacitance value. The input voltage and load current determine the RMS input ripple current (I_{RMS}):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The worst case is $I_{RMS} = 0.5 \times I_{OUT}$, which occurs at $V_{IN} = 2 \times V_{OUT}$.

For most applications, ceramic capacitors are used because of their high ripple current and surge-current capabilities. For optimal circuit long-term reliability, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current corresponding to the maximum load current. If necessary, add multiple capacitors in parallel to distribute the ripple current.

Output Capacitor Selection

Since the MAX8723's step-down regulator is internally compensated, it is stable with any reasonable amount of output capacitance. However, the actual capacitance and equivalent series resistance (ESR) affect the regulator's output ripple voltage and transient response. The rest of this section deals with how to determine the output capacitance and ESR needs according to the ripple voltage and load transient requirements.

The output voltage ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

$$V_{OUT\_RIPPLE} = V_{OUT\_RIPPLE(ESR)} + V_{OUT\_RIPPLE(C)}$$

$$V_{OUT\_RIPPLE(ESR)} = I_{OUT\_RIPPLE} \times R_{ESR\_OUT}$$

$$V_{OUT\_RIPPLE(C)} = \frac{I_{OUT}}{8 \times C_{OUT} \times f_{SW}}$$

where I_{OUT_RIPPLE} is defined in the *Inductor Selection* section, C_{OUT} is the output capacitance, and R_{ESR_OUT} is the ESR of the output capacitor C_{OUT}. In Figure 1's circuit, the inductor peak-to-peak ripple current is 0.6A. If the voltage-ripple requirement of Figure 1's circuit is ±1% of the 3.3V output, then the total peak-to-peak ripple voltage should be less than 66mV. Assuming that the ESR ripple and the capacitive ripple each should be less than 50% of the total peak-to-peak ripple, then the ESR should be less than 55mΩ and the output capacitance should be more than 1.5µF to meet the total ripple requirement. A 22µF capacitor with ESR (including PC board trace resistance) of 10mΩ is selected for the standard application circuit in Figure 1, which easily meets the voltage-ripple requirement.

The step-down regulator's output capacitor and ESR also affect the voltage undershoot and overshoot when the load steps up and down abruptly. The undershoot and overshoot also have two components: the voltage steps caused by ESR, and voltage sag and soar due to the finite capacitance and inductor slew rate. Use the following formulas to check if the ESR is low enough and the output capacitance is large enough to prevent excessive soar and sag.

The amplitude of the ESR step is a function of the load step and the ESR of the output capacitor:

$$V_{OUT\_ESR\_STEP} = \Delta I_{OUT} \times R_{ESR\_OUT}$$

The amplitude of the capacitive sag is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle:

$$V_{OUT\_SAG} = \frac{L_{OUT} \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the capacitive soar is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{OUT\_SOAR} = \frac{L_{OUT} \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Given the component values in the 1.5MHz circuit of Figure 1, during a 2A step-load transient, the voltage step due to capacitor ESR is negligible. The voltage sag and soar are 40.2mV and 71.6mV, respectively.

Rectifier Diode

The MAX8723's high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. Based on the 2A capability of the high-side switch, a 2A Schottky diode works well for most applications. The Schottky diode's current rating can be reduced or the diode can be omitted entirely, if an external synchronous rectifier MOSFET is used.

External MOSFET

To improve efficiency, an external synchronous rectifier MOSFET can be driven by EXT. When this MOSFET is used, the Schottky diode's current rating can be reduced or the diode can be omitted entirely. Choose a MOSFET with low $R_{DS(ON)}$. Ensure that EXT is not pulled up by the internal high-side switch turning on due to parasitic drain-to-gate capacitance, causing cross-conduction problems. Switching losses are not an issue for the synchronous rectifier in the step-down topology, since it is a zero-voltage switched device.

Applications Information

Thermal Considerations

The MAX8723 has a built-in power MOSFET switch and gate-driver circuits. Although the step-down regulator operates with high efficiency, inevitably the IC internal power circuits consume some power and heat the IC up, especially under heavy-load conditions. To ensure the best performance of the silicon, thermal management is critical in the application.

The built-in low-side MOSFET is not dedicated for synchronous rectifier application and has high on-resistance. An external freewheeling device such as Schottky diode or MOSFET is essential for the circuit operation. Without this freewheeling device, the heat generated by the built-in low-side MOSFET imperils the MOSFET and the IC operation, especially under heavy-load conditions such as 2A load.

The TQFN package provides an exposed metal pad on the MAX8723 backside. This back pad also serves as heat sink to the internal silicon circuitry, as well as a ground substrate. Soldering the exposed backside pad to a large copper plane on PC board can significantly help to dissipate heat generated inside the IC. Typically, the large copper plane is not available on the component side of PC board. Place a large solder pad under the IC with multiple vias connecting to a large ground plane on another board layer and solder the IC exposed back pad to this solder pad.

PC Board Layout and Grounding

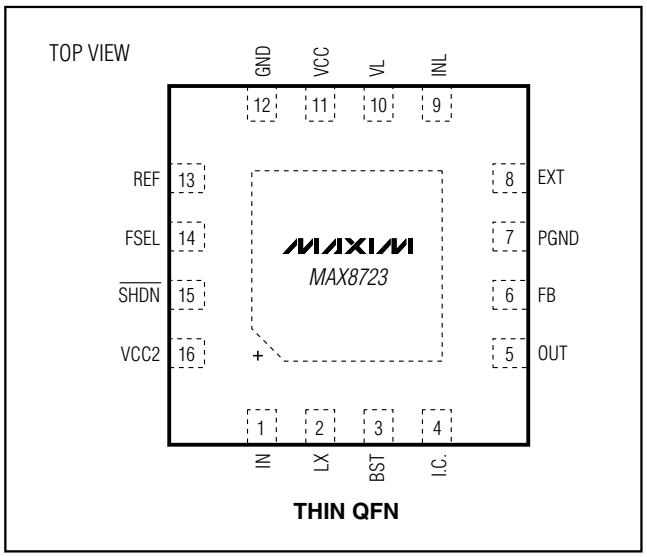
Good layout is necessary to achieve the MAX8723's intended output power level, high efficiency, and low noise. Good layout includes the use of ground planes, careful component placement, and correct routing of traces using appropriate trace widths. The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND together with short, wide traces or a small ground plane. Connect the resulting island to GND at only one point.
2) Connect the input filter capacitor less than 5mm away from IN. Place INL pin and REF pin bypass capacitors as close to the device as possible, no more than 5mm. The ground connection of the INL bypass capacitor should be connected directly to the GND pin with a wide trace.
3) Connect high-current loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
4) Place the LX node components as close together and as near to the device as possible. Minimize the length of the LX node while keeping it wide and short. This reduces resistive and switching losses, as well as noise. Keep the LX node away from FB feedback node and analog ground. Use inner layers etc., as shield if necessary.
5) Place feedback voltage-divider resistors as close to the FB feedback pin as possible. The divider's center trace should be kept short. Placing the resistors far away causes the FB traces to become antennas that can pick up switching noise. Care should be taken to avoid running any feedback trace near LX.
6) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
7) Ground planes are essential for optimum performance. In most applications, the circuit is located on a multilayer board and full use of the four or more layers is recommended. For heat dissipation, connect the exposed backside pad to a large analog ground plane, preferably on a surface of the board that receives good airflow. If the ground is not located on the IC component side of PC board, use multiple vias to the IC backside pad to lower thermal resistance. Typical applications use multiple ground planes to reduce thermal resistance. Avoid large AC currents through the analog ground plane.

Refer to the MAX8723 evaluation kit for an example of proper board layout.

Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

Pin Configuration



THIN QFN

Chip Information

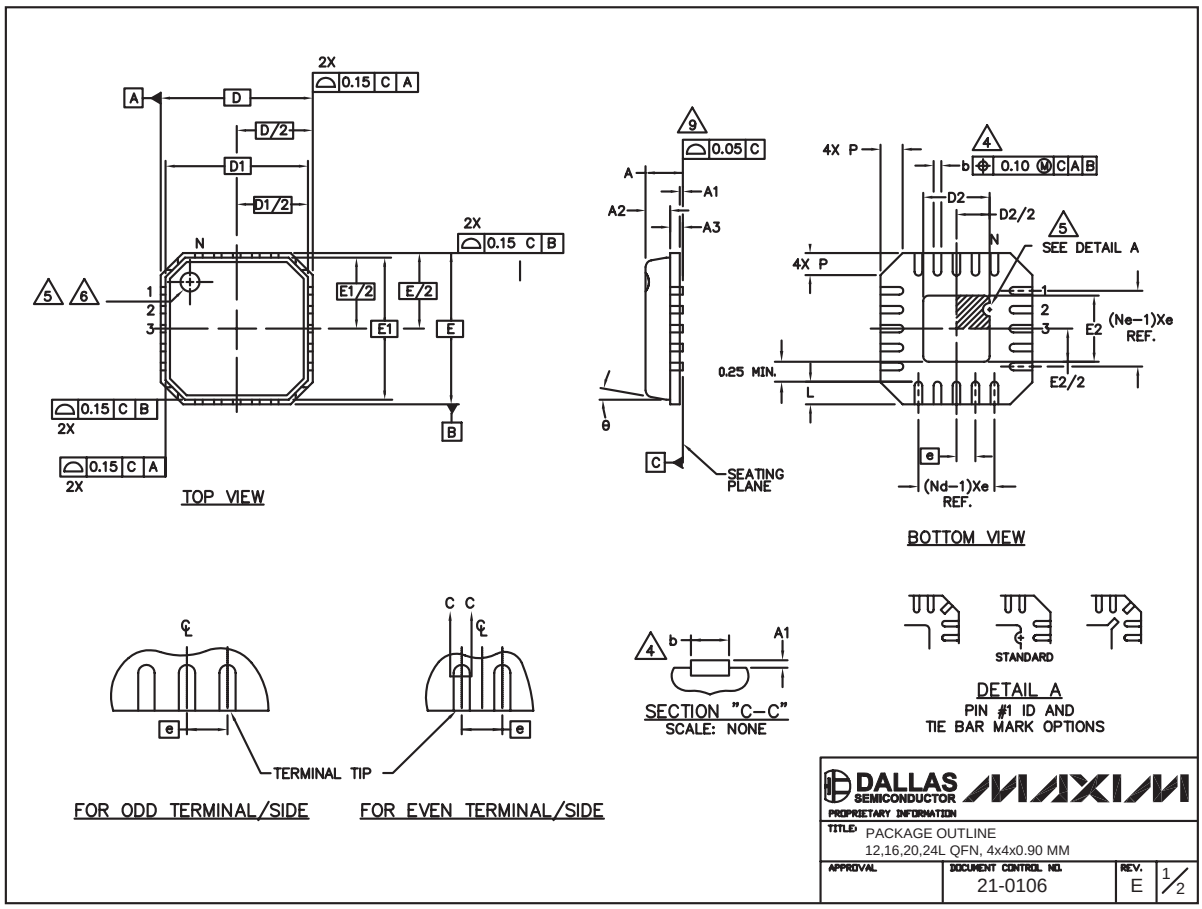
TRANSISTOR COUNT: 4127

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

12,16,20, 24L QFN.EPS



Low-Cost, Internal-Switch, Step-Down Regulator for LCD Displays

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM).
2. DIMENSIONING & TOLERANCES CONFORM MUST TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/LASER MARKED. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220; EXCEPT DIMENSION "b".
11. THIS PACKAGE OUTLINE APPLIES TO PUNCHED QFN (STEPPED SIDES).

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ	0°	–	12°	
P	0.24	0.42	0.60	

SYMBOL	PITCH VARIATION A MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION B MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION C MIN.	NOM.	MAX.	NOTE	SYMBOL	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e		0.80 BSC			e		0.65 BSC			e		0.50 BSC			e		0.50 BSC		
N		12		3	N		16		3	N		20		3	N		24		3
Nd		3		3	Nd		4		3	Nd		5		3	Nd		6		3
Ne		3		3	Ne		4		3	Ne		5		3	Ne		6		3
L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.50	0.60	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

PKG. CODE	EXPOSED PAD VARIATION D2 MIN.	NOM.	MAX.	E2 MIN.	NOM.	MAX.
G1244–2	1.95	2.10	2.25	1.95	2.10	2.25
G1644–1	1.95	2.10	2.25	1.95	2.10	2.25
G2044–3	1.95	2.10	2.25	1.95	2.10	2.25
G2044–4	1.55	1.70	1.85	1.55	1.70	1.85
G2444–1	1.95	2.10	2.25	1.95	2.10	2.25

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12,16,20,24L QFN, 4x4x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0106	E	2/2