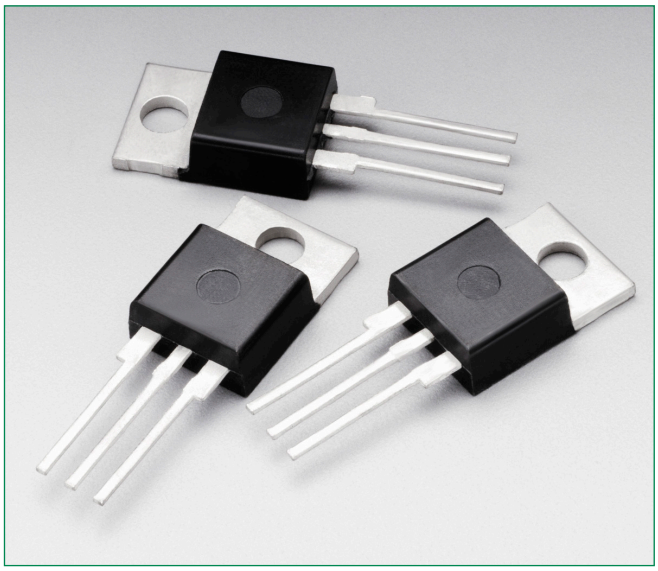
MAC8SDG, MAC8SMG, MAC8SNG



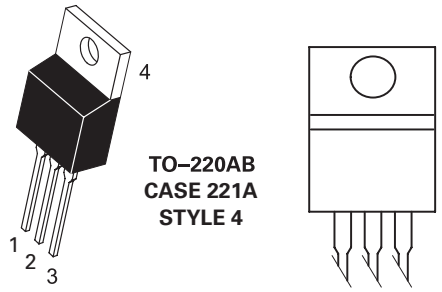
Description

Designed primarily for full-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half–wave silicon gate–controlled, solid–state devices are needed.

Features

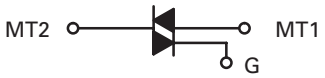
- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Uniform Gate Trigger Currents in Three Quadrants; Q1, Q2, and Q3
- High Immunity to dv/dt – 25 V/µs Minimum at 110°C
- High Commutating di/dt – 8.0 A/ms Minimum at 110°C
- Maximum Values of IGT, VGT and IH Specified for Ease of Design
- On–State Current Rating of 8 Amperes RMS at 70°C
- High Surge Current Capability – 70 Amperes
- Blocking Voltage to 800 Volts
- Rugged, Economical TO–220 Package
- These Devices are Pb–Free and are RoHS Compliant

Pin Out



TO–220AB
CASE 221A
STYLE 4

Functional Diagram



Additional Information

Datasheet | **Resources** | **Samples**

Revised: 08/30/17

Maximum Ratings (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (Gate Open, Sine Wave 50 to 60 Hz, T_J = 25° to 100°C) MAC8SDG MAC8SMG MAC8SNG	V_{DRM}, V_{RRM}	 400 600 800	V
On-State RMS Current (Full Cycle Sine Wave, 60 Hz, T_C = 100°C)	$I_{T\ (RMS)}$	8.0	A
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, T_J = 125°C)	I_{TSM}	70	A
Circuit Fusing Consideration (t = 8.3 ms)	I^2t	20	A^2sec
Peak Gate Power (Pulse Width ≤ 1.0 µs, T_L = 80°C)	P_{GM}	16	W
Average Gate Power (t = 8.3 ms, T_C = 80°C)	$P_{G\ (AV)}$	0.35	W
Operating Junction Temperature Range	T_J	-40 to +110	°C
Storage Temperature Range	T_{stg}	-40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

Rating	Symbol	Value	Unit
Thermal Resistance, Junction–to–Case (AC) Junction–to–Ambient	R_{8JC} R_{8JA}	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

Revised: 08/30/17

Electrical Characteristics - OFF (T_J = 25°C unless otherwise noted ; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak Repetitive Blocking Current ($V_D = V_{DRM} = V_{RRM}$; Gate Open)	T_J = 25°C	I_{DRM}, I_{RRM}	-	-	0.01	mA
	T_J = 110°C		-	-	2.0	

Electrical Characteristics - ON (T_J = 25°C unless otherwise noted; Electricals apply in both directions)

Characteristic		Symbol	Min	Typ	Max	Unit
Peak On–State Voltage (Note 4) (I_{TM} = ±11 A)		V_{TM}	–	–	1.85	V
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ω)	MT2(+), G(+)	I_{GT}	–	2.0	5.0	mA
	MT2(+), G(–)		–	3.0	5.0	
	MT2(–), G(–)		–	3.0	5.0	
Holding Current (V_D = 12 V, Gate Open, Initiating Current = ±150 mA))		I_H	–	3.0	10	mA
Latching Current (V_D = 24 V, I_G = 5 mA)	MT2(+), G(+)	I_L	_	5.0	15	mA
	MT2(+), G(–)		_	10	20	
	MT2(–), G(–)		_	5.0	15	
Gate Trigger Voltage (V_D = 12 V, R_L = 100 Ω)	MT2(+), G(+)	V_{GT}	0.45	0.62	1.5	V
	MT2(+), G(–)		0.45	0.60	1.5	
	MT2(–), G(–)		0.45	0.65	1.5	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

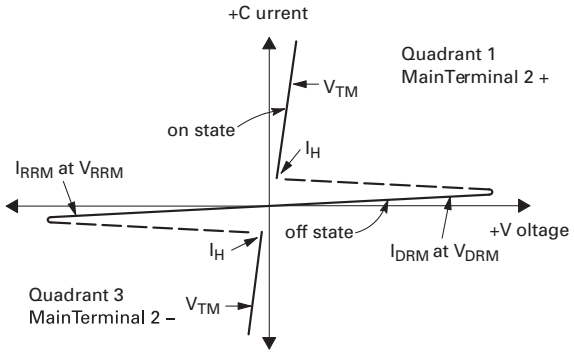
Dynamic Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Rate of Change of Commutating Current See Figure 10. (V_D = 400 V, I_{TM} = 4.4 A, Commutating dv/dt = 18 V/µs,Gate Open, TJ = 125°C, f = 250 Hz, No Snubber) C_L = 10 µF L_L = 40 mH	dV/dt	8.0	10	–	A/ms
Critical Rate of Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, R_{GK} = 510 Ω, T_J = 110°C)	dV/dt	25	75	–	V/µs

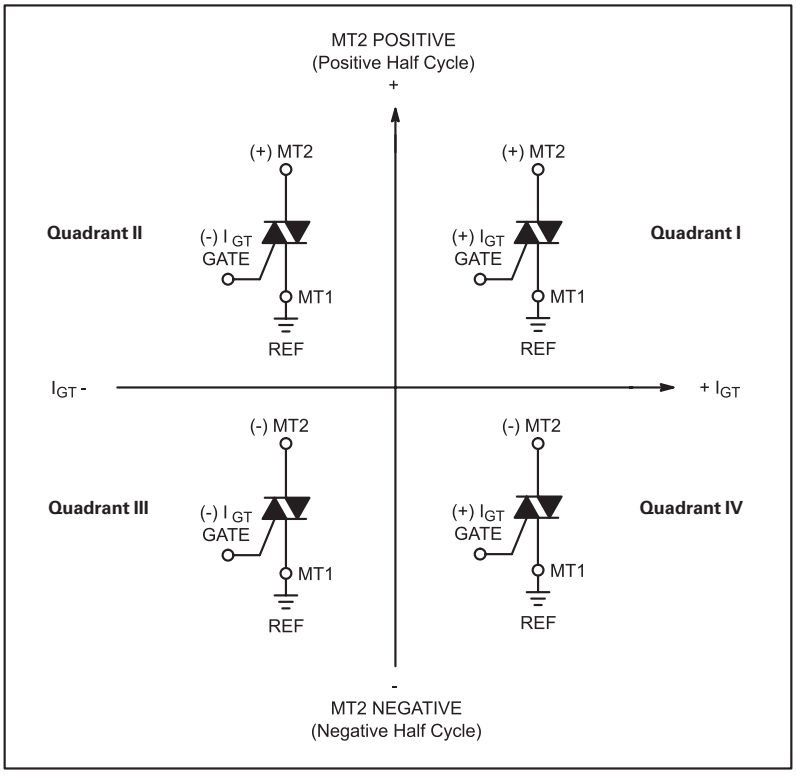
Revised: 08/30/17

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions for a Triac



All polarities are referenced to MT1.

With in–phase signals (using standard AC lines) quadrants I and III are used.

Revised: 08/30/17

Figure 1. RMS Current Derating

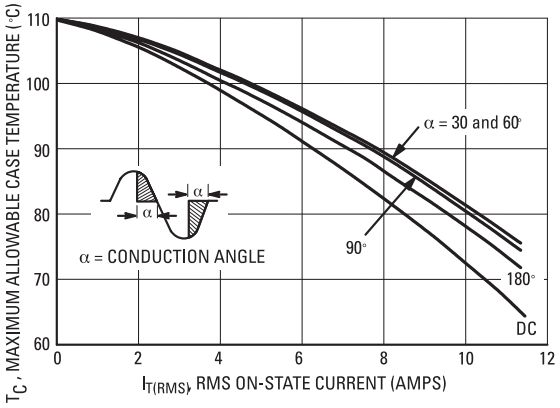


Figure 2. Maximum On-State Power Dissipation

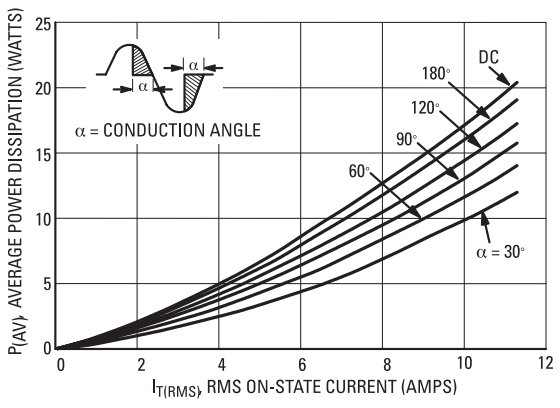


Figure 3. On–State Characteristics

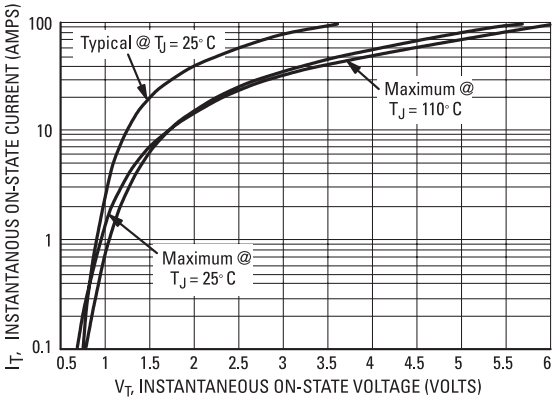


Figure 4. Transient Thermal Response

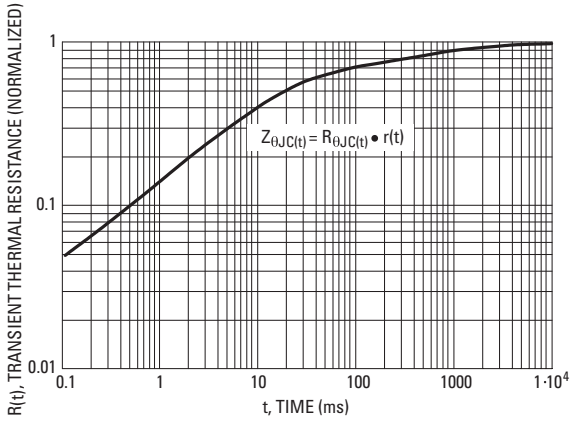


Figure 5. Typical Holding Current Vs. Junction Temperature

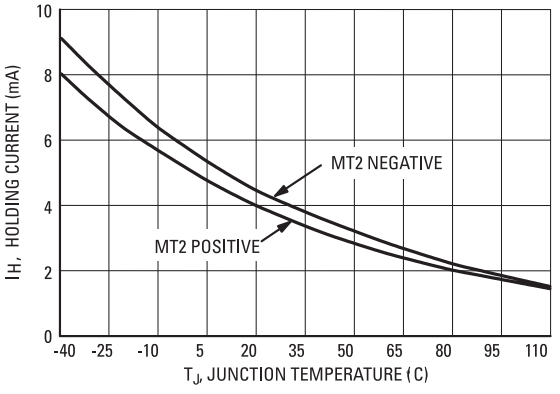
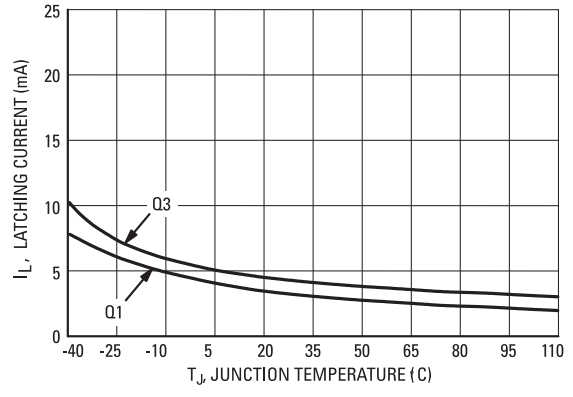


Figure 6. Typical Latching Current Vs. Junction Temperature



Revised: 08/30/17

Figure 7. Typical Gate Trigger Current Vs. Junction Temperature

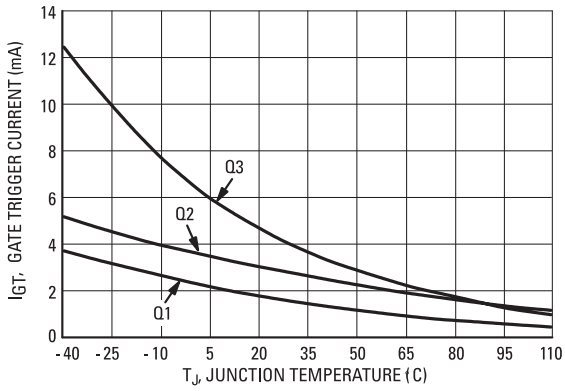


Figure 8. Typical Gate Trigger Voltage Vs. Junction Temperature

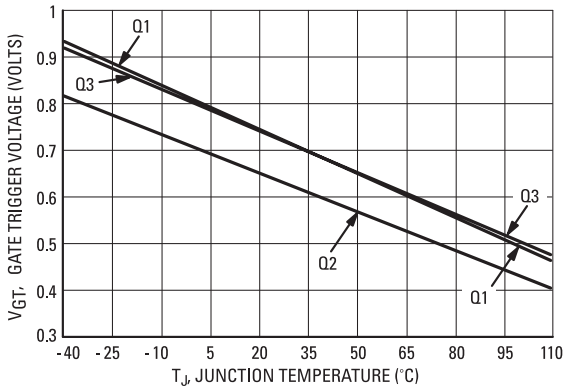


Figure 9. Typical Exponential Static dv/dt Vs. Gate–MT1 Resistance, MT2(+)

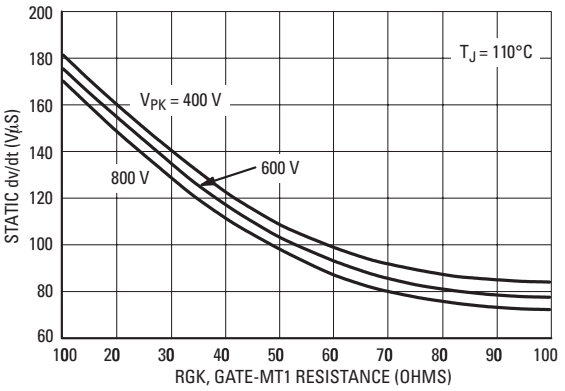


Figure 10. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(+)

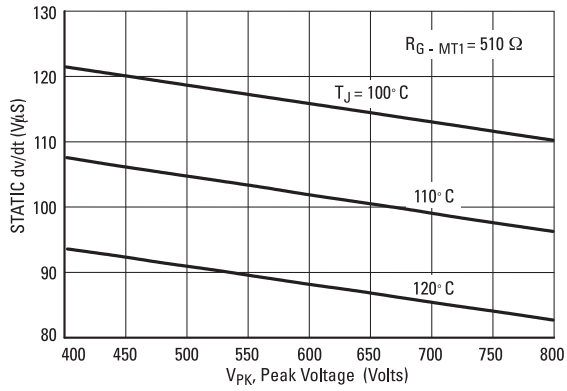


Figure 11. Typical Exponential Static dv/dt Vs. Junction Temperature, MT2(+)

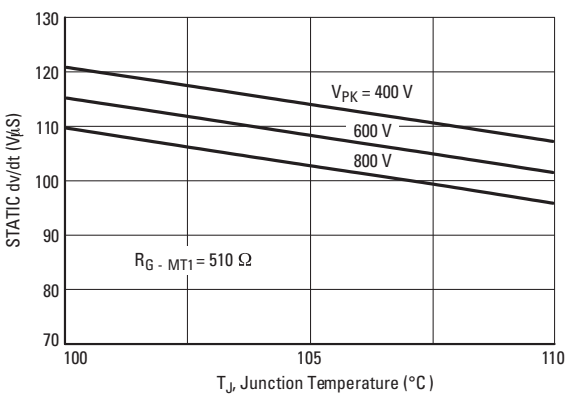


Figure 12. Typical Exponential Static dv/dt Vs. Peak Voltage, MT2(–)

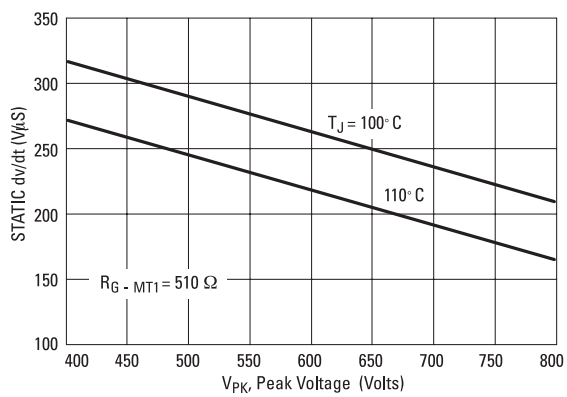


Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(–)

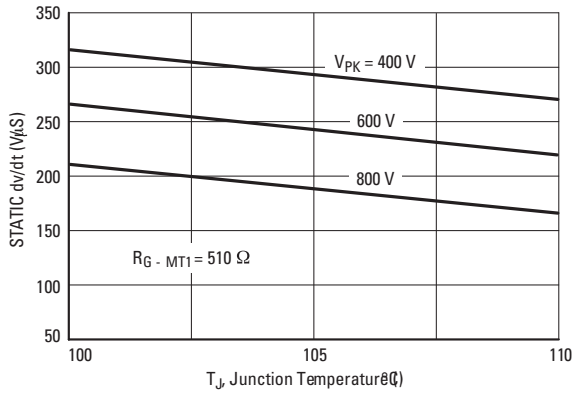


Figure 14. Typical Exponential Static dv/dt Versus Gate–MT1 Resistance, MT2(–)

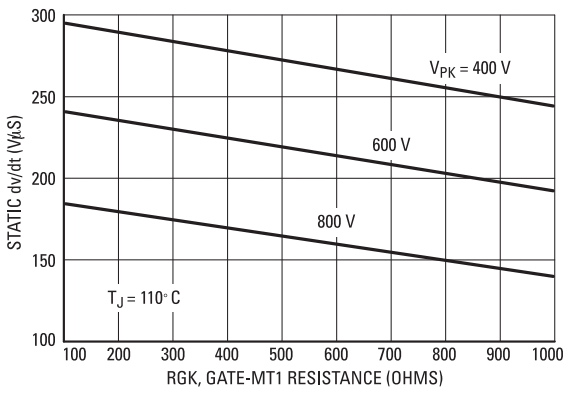


Figure 15. Critical Rate of Rise of Commutating Voltage

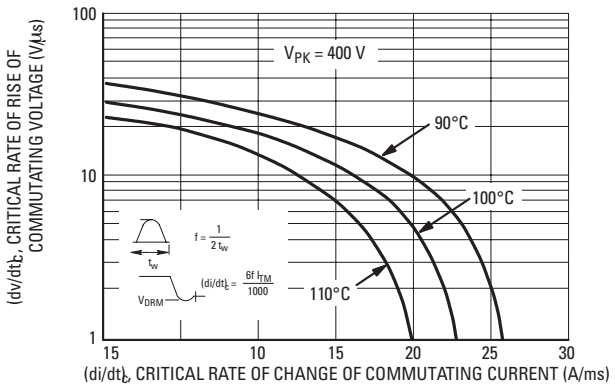
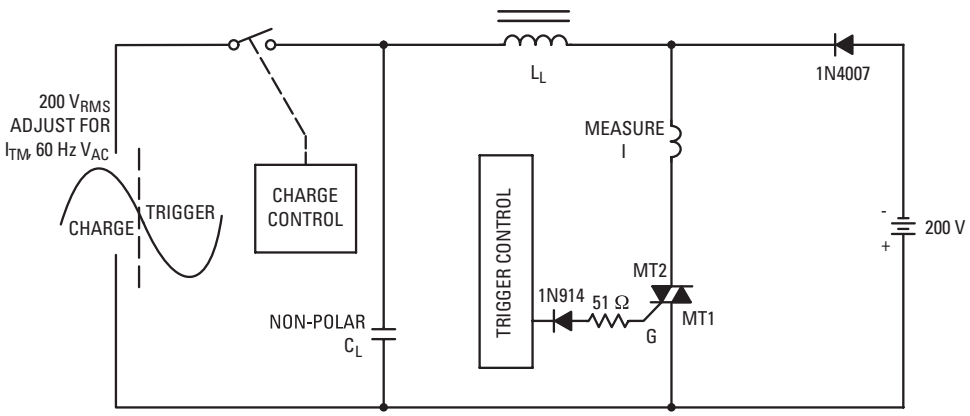


Figure 16. Simplified Test Circuit to Measure the Critical Rate of Rise of Commutating Current (di/dt)

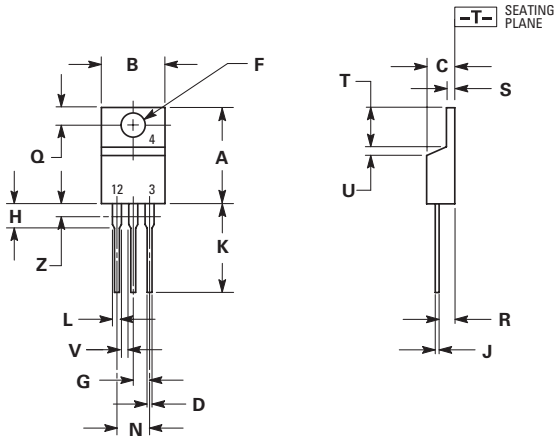


Note: Component values are for verification of rated $(di/dt)_c$. See AN1048 for additional information.

Thyristors

Surface Mount – 50V > MAC8SDG, MAC8SMG, MAC8SNG

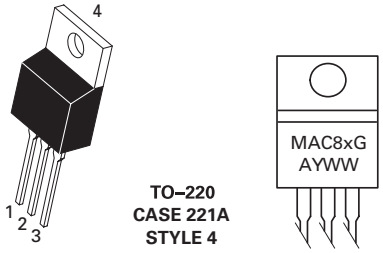
Dimensions



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

Part Marking System



TO–220
CASE 221A
STYLE 4

x= D, M, or N
A= Assembly Location (Optional)*
Y= Year
WW = Work Week
G = Pb–Free Package

* The Assembly Location code (A) is optional. In cases where the Assembly Location is stamped on the package the assembly code may be blank.

Pin Assignment

1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

Ordering Information

Device	Package	Shipping
MAC8SDG	TO-220AB (Pb-Free)	50 Units / Rail
MAC8SMG		
MAC8SNG		