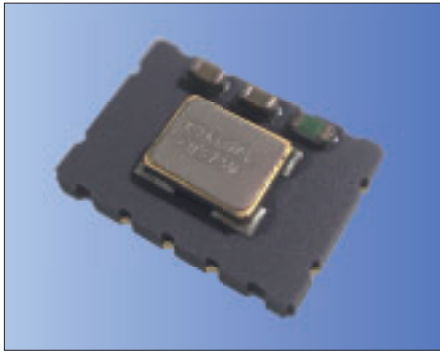


7.0×5.0mm



RoHS Compliant

**Features**

- High stability and high reliability
- 2.7 to 5.5V drive available
- Clipped sine wave or CMOS level output
- Low phase noise
- Disable Function (KT7050A)

**Applications**

- 5G, Smallcell, Stratum3
- SONET/ SDH/ Ethernet

**How to Order**

KT7050 □ 20000 □ A □ 33 T xx  
 ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

- ① Series
- ② Land Type
- ③ Output Frequency
- ④ Freq. Temp. Chrst.
- ⑤ Lower Operating Temp.
- ⑥ Upper Operating Temp.

	④	⑤	⑥
<b>KAW</b>	±0.28×10 <sup>-6</sup>	-40°C	+85°C
<b>KAY</b>	±0.28×10 <sup>-6</sup>	-40°C	+105°C
<b>AAV</b>	±0.10×10 <sup>-6</sup>	-40°C	+105°C

⑦ Supply Voltage	⑧ Voltage Control Function
<b>33</b>	<b>T</b>
3.3V	TCXO
	<b>Spec. Code*</b>
	VCTCXO

\*Please contact us for Spec. Code.

- ⑨ Individual Specification

Packaging (Tape & Reel 1000 pcs./ reel)

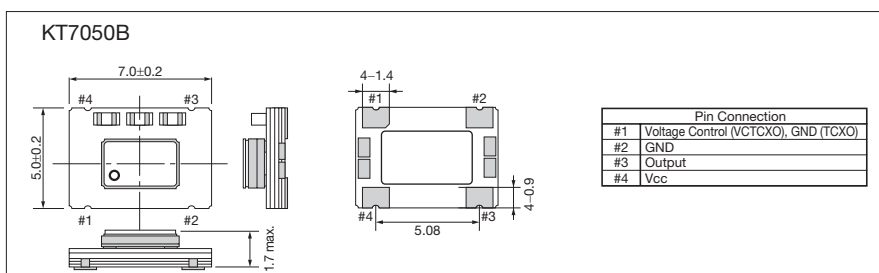
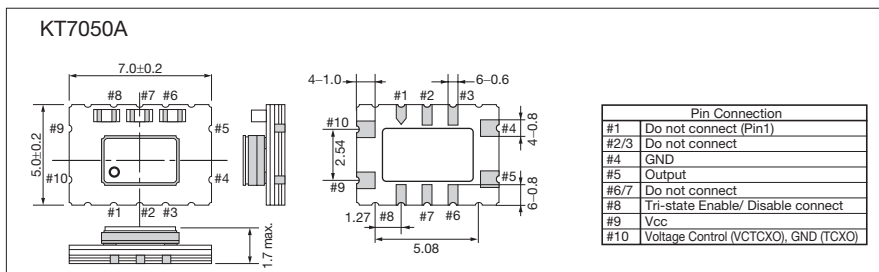
- Compliant to the GR1244-Core & GR253-Core
- Recommended in Microsemi's ZLAN-68 app. note for Stratum3 applications based on tests performed by Kyocera.

**Specifications**

Item	Symbol	Conditions	Min.	Max.	Units	
<b>Output Frequency Range</b>	f <sub>o</sub>	Standard Frequency: 10, 19.2, 20, 24.576, 26, 30.72, 38.88, 40 vs Temperature (-10 to +105°C) [±(fmax-fmin)/ 2fo]	10	40	MHz	
<b>Frequency Tolerance</b>	f <sub>tol</sub>	vs Temperature (-40 to +85°C/ +105°C) [±(fmax-fmin)/ 2fo] vs Voltage	-0.1	+0.1	×10 <sup>-6</sup>	
			-0.1	+0.1		
<b>Supply Voltage</b>	V <sub>CC</sub>		+2.7	+5.5	V	
<b>Current Consumption</b>	I <sub>CC</sub>	CMOS Output	—	6	mA	
<b>Frequency Aging</b>	f <sub>age</sub>	20years aging @40°C Including temp characteristics, initial tolerance, rated power supply voltage change and load change.	-4.6	+4.6	×10 <sup>-6</sup>	
<b>Voltage Control Range</b>	f <sub>cont</sub>	Positive *100k ohm min	±5	±20	×10 <sup>-6</sup>	
<b>Output Level</b>	V <sub>pp</sub>	Clipped Sine, Load: 10k ohm // 10pF	0.8	—	Vp-p	
<b>Low Level Output Voltage</b>	V <sub>OL</sub>	CMOS, Load: 15pF I <sub>OL</sub> = 4mA	—	10% V <sub>CC</sub>	V	
<b>High Level Output Voltage</b>	V <sub>OH</sub>	CMOS, Load: 15pF I <sub>OH</sub> = -4mA	90% V <sub>CC</sub>	—	V	
<b>Rise / Fall Time (10%V<sub>CC</sub> to 90%V<sub>CC</sub>)</b>	tr/ tf	CMOS, Load: 15pF	—	8	ns	
<b>Symmetry</b>	SYM	50% V <sub>CC</sub>	45	55	%	
<b>Phase Noise</b>	—	@20MHz	@10Hz offset	—	-90	dBc/ Hz
			@100Hz offset	—	-120	
			@1kHz offset	—	-140	
			@10kHz offset	—	-150	
			@100kHz offset	—	-150	

\* Please contact us for other specifications.

**Dimensions**



**Recommended Land Pattern (Unit: mm)**

