ISL94208

4- to 6-Cell Li-ion Battery Management Analog Front-End

FN8306
Rev.2.00
May 1, 2017

The ISL94208 battery management IC is designed for use with a microcontroller and features an analog front-end with overcurrent protection for multi-cell Li-ion battery packs. The ISL94208 supports battery packs consisting of four to six cells in series and one or more cells in parallel.

Using an internal analog multiplexer, the ISL94208 allows a separate microcontroller with an A/D converter to monitor each cell voltage plus internal and external temperature.

The ISL94208 provides integral overcurrent and short-circuit protection circuitry, an internal 3.3V voltage regulator, internal cell balancing switches, and drive circuitry for external FET devices for control of pack charge and discharge.

Related Literature

- For a full list of related documents, visit our website
  - ISL94208 product page

Features

- Software selectable overcurrent protection levels and variable protect detection times
  - 4 discharge overcurrent thresholds
  - 4 short-circuit thresholds
  - 4 charge overcurrent thresholds
  - 8 overcurrent delay times (charge)
  - 8 overcurrent delay times (discharge)
  - 2 short-circuit delay times (discharge)
- Automatic FET turn-off and cell balance disable on reaching external (battery) or internal (IC) temperature limit
- Automatic cell balance turn off on IC over-temperature
- Integrated charge/discharge FET drive circuitry
- Internal cell balancing FETs handle up to 200mA of balancing current for each cell
- Sleep operation with negative or positive edge wake-up
- <10µA Sleep mode

Applications

- Power tools
- Portable equipment
- Battery backup systems
- Military electronics

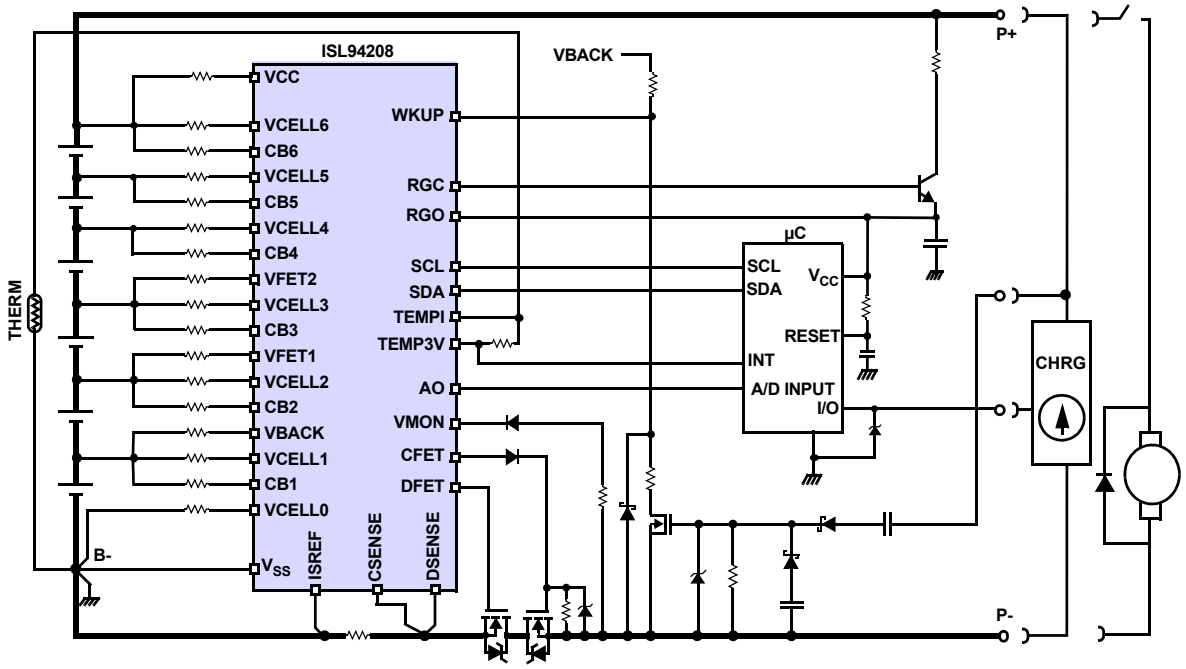

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS- COMPLIANT)	PKG. DWG. #
ISL94208IRZ	94208 IRZ	-40 to +85	32 Ld 5x5 QFN	L32.5x5B
ISL94208EVZ	Evaluation Board			

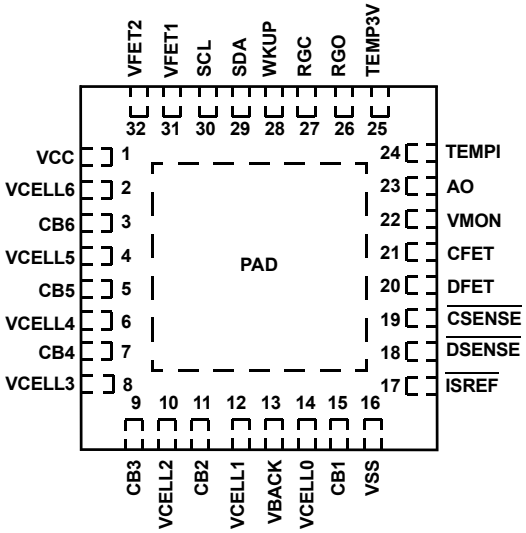
1. Add “-T” suffix for 6k unit or “-T7A” suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the product information page for ISL94208. For more information on MSL, see tech brief TB363

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

	CELLS SUPPORTED		PACK VOLTAGE (Op)				CHARGE/DISCHARGE FET			SUPPLY CURRENT (Typ)				
PART #	MIN	MAX	MIN (V)	MAX (V)	CELL BALANCE	CURRENT SENSE	CONTROL	ARRANGEMENT	LOCATION	NORMAL	SLEEP	STAND-ALONE CAPABLE	INTERNAL ADC	DAISY CHAIN
ISL94202	3	8	4	36	External	High Side	Yes	One Path	High Side	348µA	13µA	Yes	Yes	No
ISL94203	3	8	4	36	External	High Side	Yes	Two Path	High Side	348µA	13µA	Yes	Yes	No
ISL94208	4	6	8	26.4	Internal	Low Side	Yes	Both	Low Side	850µA	2µA	No	No	No
ISL94212	6	12	6	60	External	No	No	N/A	N/A	3.31mA	12µA	No	Yes	Yes

Pin Configuration

ISL94208
(32 LD QFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VCC	**VCC supply.** This pin provides the operating voltage for the IC circuitry. Connect to the positive terminal of the battery pack through a filter.
14, 12, 10, 8, 6, 4, 2	VCELL0, VCELL1, VCELL2, VCELL3, VCELL4, VCELL5, VCELL6	**Battery terminal N voltage input**. For N = 1 to 6, VCELLN connects to the positive terminal of CELLN and the negative terminal of CELLN + 1.
13	VBACK	**Sleep mode backup supply.** This pin is used to power the logic when the device is asleep and the RGO output turns off.
31, 32	VFET1, VFET2	**FET Drivers power supply.** These pins are used to provide the reference voltages for the power FET gate drivers. Typically VFET2 connects to VCELL3 (or equivalent voltage) and VFET1 connects to VCELL2 (or equivalent voltage).
15,11, 9 7, 5, 3	CB1, CB2, CB3, CB4, CB5, CB6	**Cell balancing FET driver output** N (N = 1 to 6). An internal FET between the CBN and the VCELL(N - 1) can be turned on to discharge CELLN more than other cells, or to shunt some of the charging current away from CELLN. This function is used to reduce the voltage on an individual cell relative to other cells in the pack. The cell balancing FETs are turned on or off by an external controller, using the I^2C interface.
16	VSS	**Ground**. This pin connects to the most negative terminal in the battery string.
17	$\overline{\text{ISREF}}$	**Current sense reference.** This input provides a separate reference point for the charge and discharge current monitoring circuits. With a separate reference connection, it is possible to minimize errors that result from voltage drops on the ground lead when the load is drawing large currents. If a separate reference is not necessary, connect this pin to VSS.
18	$\overline{\text{DSENSE}}$	**Discharge current sense monitor.** This input monitors the discharge current by monitoring a voltage across a sense resistor, across the discharge path FET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to ISREF.
19	$\overline{\text{CSENSE}}$	**Charge current sense monitor.** This input monitors the charge current by monitoring a voltage across a sense resistor, the voltage across the charge path FET, or by using a FET with a current sense pin. The voltage on this pin is measured with reference to ISREF.
20	DFET	**Discharge FET control.** The ISL94208 controls the gate of a discharge path FET through this pin. The power FET is an N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL94208 also turns off the FET in the event of an overcurrent or short-circuit condition. If the microcontroller detects an undervoltage condition on any of the battery cells, it can turn off the discharge FET by controlling this output with a control bit.
21	CFET	**Charge FET control.** The ISL94208 controls the gate of a charge path FET through this pin. The power FET is an N-Channel device. The FET is turned on only by the microcontroller. The FET can be turned off by the microcontroller, but the ISL94208 also turns off the FET in the event of an overcurrent condition. If the microcontroller detects an overvoltage condition on any of the battery cells, it can turn off the FET by controlling this output with a control bit.
22	VMON	**Discharge load monitoring.** In the event of an overcurrent or short-circuit condition, the microcontroller can enable an internal resistor that connects between the VMON pin and VSS. When the FETs open because of an overcurrent or short-circuit condition and the load remains, the voltage at VMON will be near the VCC voltage. When the load is released, the voltage at VMON drops below a threshold indicating that the overcurrent or short-circuit condition is resolved. At this point, the LDFAIL flag is cleared and operation can resume.
23	AO	**Analog multiplexer output.** The analog output pin is used to monitor the cell voltages and temperature sensor voltages. An external microcontroller selects the specific voltage being applied to the output by writing to a control register.
24	TEMPI	**Temperature monitor input.** The voltage across a thermistor is monitored at this pin to determine the temperature of the battery cells. When this input drops below TEMP3V/13, an external over-temperature condition is reported. The TEMPI voltage can be fed to the AO output pin through an analog multiplexer to be monitored by the microcontroller.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
25	TEMP3V	**Temperature monitor output control.** This pin outputs a voltage to be used in a divider that consists of a fixed resistor and a thermistor. The thermistor is located in close proximity to the battery cells. The TEMP3V output is connected internally to the RGO voltage through a PMOS switch only during a measurement of the temperature, otherwise the TEMP3V output is off. The TEMP3V output can be turned on continuously with a special control bit. Microcontroller wake-up control. The TEMP3V pin is also turned on when any of the DSC, DOC, or COC bits are set. This can be used to wake up a sleeping microcontroller to respond to overcurrent conditions with its own control mechanism.
26	RGO	**Regulated output voltage.** This pin connects to the emitter of an external NPN transistor and works in conjunction with the RGC pin to provide a regulated 3.3V. The voltage at this pin provides feedback for the regulator and power for many of the ISL94208 internal circuits as well as providing the 3.3V output voltage for the microcontroller and other external circuits.
27	RGC	**Regulated output control.** This pin connects to the base of an external NPN transistor and works in conjunction with the RGO pin to provide a regulated 3.3V. The RGC output provides the control signal for the external transistor to provide the 3.3V regulated voltage on the RGO pin.
28	WKUP	**Wake-up voltage.** This input wakes up the device when the voltage crosses a turn-on threshold (wake-up is edge triggered). The condition of the pin is reflected in the WKUP bit (the WKUP bit is level sensitive). WKPOL bit = '1': the device wakes up on the rising edge of the WKUP pin. The WKUP bit is HIGH only when the WKUP pin voltage > threshold. WKPOL bit = '0', the device wakes up on the falling edge of the WKUP pin. The WKUP bit is HIGH only when the WKUP pin voltage < threshold.
29	SDA	**Serial Data.** This is the bidirectional data line for an I^2C interface. This pin should be pulled up to 3.3V using a resistor.
30	SCL	**Serial Clock.** This is the clock input for an I^2C communication link. This pin should be pulled up to 3.3V using a resistor.
-	PAD	**Thermal Pad.** Connect to VSS.

Block Diagram

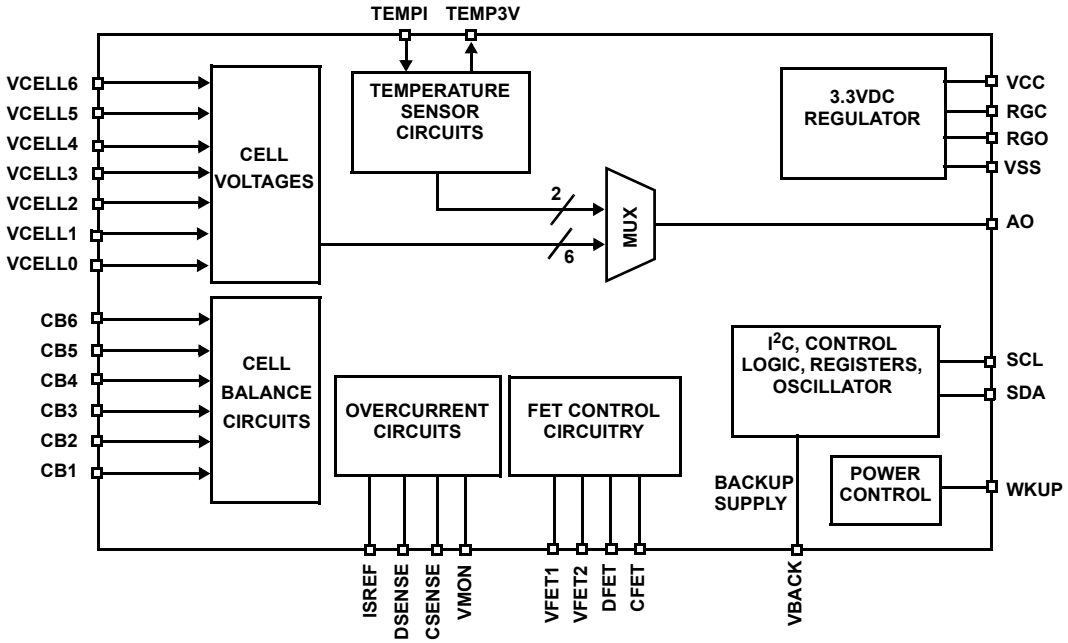


FIGURE 2. BLOCK DIAGRAM

Absolute Maximum Ratings (Note 4)

Power Supply Voltage, V_{CC} ..... -0.5V to 36.0V
Cell Voltage, VCELL
- VCELLn (n = 5, 6) ..... -0.5V to 27.0V
- VCELLn (n = 3, 4) ..... -0.5V to 18.0V
- VCELLn (n = 1, 2) ..... -0.5V to 9.0V
- VCELLn - VCELLn-1 (n = 1, 2, 3, 4, 5, 6) ..... -0.5V to 5V
- VCELL1 ..... -0.5V to 5V
- VCELL0 ..... -0.5V to 0.5V

Cell Balance, CB
- CB6 ..... -0.5V to 36V
- CB6 ..... -0.5V to V_{CC} + 0.5V
- CB4, CB5 ..... -0.5V to 27V
- CB4, CB5 ..... -0.5V to V_{CC} + 0.5V
- CB2, CB3 ..... -0.5V to 18.0V
- CB1 ..... -0.5V to 7.0V
- CBn -VCn-1 (n = 1, 2, 3, 4, 5, 6) ..... -0.5V to 7.0V

FET Control
- VFET2 ..... 0.5 to 18V
- VFET1 ..... 0.5 to 13V
- VFET2-VFET1 ..... -0.5 to 5V
- CFET ..... -18.0V to 18V
- CFET ..... -18.0V to V_{VFET2} + 0.5V
- DFET ..... -0.5V to 18V
- DFET ..... -0.5V to V_{VFET2} + 0.5V

Terminal Voltage,
- SCL, SDA, C_{SENSE}, D_{SENSE}, TEMPI, RGO, AO, TEMP3V ..... - 0.5 to V_{RGO} + 0.5V
- ISREF ..... - 0.5V to V_{SS} + 0.5
- VBACK, RGC ..... - 0.5 to 5V
- VMON ..... - 0.5V to 36V
- VMON ..... - 0.5V to V_{CC} + 0.5V
- WKUP ..... - 0.5V to 27V
- WKUP ..... - 0.5V to V_{CC} + 0.5V

ESD Rating
- Human Body Model (Tested per JESD22-A114F) 2kV
- Machine Model (Tested per JESD22-A115-A) 250V
- Capacitive Discharge Model (Tested per JESD22-C101D) 1.5kV

Latch-Up (Tested per JESD-78D; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN (Notes 5, 6)	30	1.7

Continuous Package Power Dissipation 400mW
Storage Temperature Range ..... -55 to +125°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions (Note 4)

Temperature Range ..... -40°C to +85°C
Operating Voltage:
- VCC ..... 8V to 26.4V
- SCL, SDA ..... 0V to 3.6V
- VBACK ..... VCELL1 or 2.0V to 4.6V
- VCELL1 - VSS ..... 2.0V to 4.3V
- VCELLn - VCELLn-1 ..... 2.0V to 4.3V
- VFET1 ..... 4.2 to 8.6
- VFET2 ..... 8.4 to 12.9
- VFET2 - VFET1 ..... 2.8V to 4.5V
- ISREF - VSS ..... -0.1V to 0.1V
- (C_{SENSE} - ISREF), (D_{SENSE} - ISREF) ..... -0.5V to 1.5V
- DFET ..... -0.5V to V_{FET2}
- CFET ..... -0.5V to V_{FET2}
- WKUP (WKPOL=0) ..... -0.5V to V_{BACK}
- WKUP (WKPOL=1) ..... -0.5V to 27V
- VMON ..... -0.5V to V_{CC}

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. All Absolute Maximum Ratings and Recommended Operating Conditions referenced to VSS, unless otherwise noted.
5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
6. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Power-Up Condition 1	V_{PORVCC}	V_{CC} voltage (Note 8)		4	**6.5**	V
Power-Up Condition 2 Threshold (Rising)	V_{POR}	V_{BACK} - V_{SS} (rising) (Note 8)		1.6	**2.05**	V
		0°C to +60°C		1.55	1.95	V
Power-Up Condition 2 Threshold Hysteresis	V_{HYS}	V_{BACK} - V_{SS} (falling) (Note 8)	**0.02**	0.1	**0.30**	V
3.3V Regulated Voltage	V_{RGO}	0µA < I_{RGC} < 350µA	**3.0**	3.3	**3.6**	V

Electrical Specifications V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
3.3VDC Voltage Regulator Control Current Limit	I_{RGC}	(Control current at output of RGC. Recommend NPN with gain of 70+)	**0.35**	0.50		mA
V_{CC} Supply Current	I_{VCC1}	Power-up defaults, WKUP pin = 0V		300	**510**	µA
	I_{VCC2}	LDMONEN bit = 1, VMON floating, CFET = 1, DFET=1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H		400	**700**	µA
	I_{VCC3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1		1	**10**	µA
VFET1 Supply Current (Normal or Sleep Mode)	I_{VFET1}			0.1	**1.5**	µA
VFET2 Supply Current (Normal or Sleep Mode)	I_{VFET3}	DFET, CFET outputs floating		0.1	**1**	µA
RGO Supply Current	I_{RGO1}	Power-up defaults, WKUP pin = 0V		300	**410**	µA
	I_{RGO2}	LDMONEN bit = 1, VMON floating, CFET = 1, DFET=1, WKPOL bit = 1, VWKUP = 10V, [AO3:AO0] bits = 03H		450	**650**	µA
	I_{RGO3}	Default register settings, except SLEEP bit = 1. WKUP pin = VCELL1		0.4	**1**	µA
VBACK Input Current (Falling edge wake-up; WKPOL = 0) (Normal or Sleep Mode)	$I_{VBACK01}$	WKUP ≤ V_{WKUP2}(max)		7	**12**	µA
	$I_{VBACK02}$	V_{WKUP2}(max) < WKUP < 5V		0.5	**3**	µA
VBACK Input Current (Rising edge wake-up; WKPOL = 1) (Normal Mode)	$I_{VBACK11}$	WKUP < V_{WKUP1}(min) or; WKUP > V_{WKUP1}(max)		0.5	**3**	µA
	$I_{VBACK12}$	V_{WKUP1}(min) ≤ WKUP ≤ V_{WKUP1}(max)		120	**300**	µA
(Sleep Mode)	$I_{VBACK13}$	WKUP ≥ V_{WKUP1}(min)		180	**500**	µA
	$I_{VBACK14}$	WKUP < V_{WKUP1}(min)		0.5	**3**	µA
VCELL Input Current (Monitoring)	I_{VCELLA}	Sinking current at: VCELL6 (measure VCELL6 or VCELL5) and VCELL5 (measure VCELL6 or VCELL5) and VCELL4 (measure VCELL5)		40	**65**	µA
	I_{VCELLB}	Sinking current at: VCELL4 (measure VCELL4) and VCELL3 (measure VCELL4 or VCELL3) and VCELL2 (measure VCELL3)		30	**50**	µA
	I_{VCELLC}	Sourcing current at: VCELL2 (measure VCELL2) and VCELL1 (measure VCELL2)	**-40**	-20		µA
	I_{VCELLD}	Sourcing current at: VCELL1 (measure VCELL1) and VCELL0 (measure VCELL1)	**-38**	-18		µA
VCELL Input Current Differential (Monitoring)	$I_{VCELLDIFF}$	Difference in monitoring current between VCELLn and VCELL(n-1); n = 1, 2, 3, 4	**-2**		**2**	µA
		Difference in monitoring current between VCELLn and VCELL(n-1); n = 5, 6	**-4**		**4**	µA
VCELL Input Current (Non-Monitoring)	I_{VCELLN}	VCELLn and VCELL(n-1) (n = 1, 2, 3, 4, 5, or 6) n is a non-selected cell	**-1**	±0.1	**1**	µA

Electrical Specifications V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
OVERCURRENT/SHORT-CIRCUIT PROTECTION SPECIFICATIONS						
Discharge Overcurrent Detection Threshold Sense Voltage Relative To ISREF (Default Highlighted)	V_{OCD}	V_{OCD} = 0.10V (OCDV1, OCDV0 = 0, 0)	**0.08**	0.10	**0.12**	V
		V_{OCD} = 0.12V (OCDV1, OCDV0 = 0, 1)	**0.10**	0.12	**0.14**	V
		V_{OCD} = 0.14V (OCDV1, OCDV0 = 1, 0)	**0.12**	0.14	**0.16**	V
		V_{OCD} = 0.16V (OCDV1, OCDV0 = 1, 1)	**0.14**	0.16	**0.18**	V
Charge Overcurrent Detection Threshold Sense Voltage Relative to ISREF (Default Highlighted)	V_{OCC}	V_{OCC} = 0.10V (OCCV1, OCCV0 = 0, 0)	**-0.12**	-0.10	**-0.07**	V
		V_{OCC} = 0.12V (OCCV1, OCCV0 = 0, 1)	**-0.14**	-0.12	**-0.09**	V
		V_{OCC} = 0.14V (OCCV1, OCCV0 = 1, 0)	**-0.16**	-0.14	**-0.11**	V
		V_{OCC} = 0.16V (OCCV1, OCCV0 = 1, 1)	**-0.18**	-0.16	**-0.13**	V
Short Current Detection Threshold Voltage Relative to ISREF (Default Highlighted)	V_{SC}	V_{SC} = 0.20V (SCDV1, SCDV0 = 0, 0)	**0.15**	0.20	**0.25**	V
		V_{SC} = 0.35V (SCDV1, SCDV0 = 0, 1)	**0.30**	0.35	**0.40**	V
		V_{SC} = 0.65V (SCDV1, SCDV0 = 1, 0)	**0.60**	0.65	**0.70**	V
		V_{SC} = 1.20V (SCDV1, SCDV0 = 1, 1)	**1.10**	1.20	**1.30**	V
Load Monitor Input Threshold (Falling Edge)	V_{VMON}	LDMONEN bit = '1'	**1.1**	1.45	**1.8**	V
Load Monitor Input Threshold (Hysteresis)	V_{VMONH}	LDMONEN bit = '1'		0.25		mV
Load Monitor Current	I_{VMON}	V(VMON) between VVMON and V(V_{CC})	**20**	40	**60**	µA
Short-Circuit Time-out (Default Highlighted)	t_{SCD}	Short-circuit detection delay (SCLONG bit = '0')	**90**	190	**290**	µs
		Short-circuit detection delay (SCLONG bit = '1')	**5**	10	**15**	ms
Over Discharge Current Time-out (Default Highlighted)	t_{OCD}	t_{OCD} = 160ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 0)	**80**	160	**240**	ms
		t_{OCD} = 320ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 0)	**160**	320	**480**	ms
		t_{OCD} = 640ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 0)	**320**	640	**960**	ms
		t_{OCD} = 1280ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 0)	**640**	1280	**1920**	ms
		t_{OCD} = 2.5ms (OCDT1, OCDT0 = 0, 0 and DTDIV = 1)	**1.25**	2.50	**3.75**	ms
		t_{OCD} = 5ms (OCDT1, OCDT0 = 0, 1 and DTDIV = 1)	**2.5**	5	**7.5**	ms
		t_{OCD} = 10ms (OCDT1, OCDT0 = 1, 0 and DTDIV = 1)	**5**	10	**15**	ms
		t_{OCD} = 20ms (OCDT1, OCDT0 = 1, 1 and DTDIV = 1)	**10**	20	**30**	ms

Electrical Specifications V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Over Charge Current Time-out (Default Highlighted)	t_{OCC}	t_{OCC} = 80ms (OCCT1,OCCT0 = 0, 0 and CTDIV = 0)	**40**	80	**120**	ms
		t_{OCC} = 160ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 0)	**80**	160	**240**	ms
		t_{OCC} = 320ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 0)	**160**	320	**480**	ms
		t_{OCC} = 640ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 0)	**320**	640	**960**	ms
		t_{OCC} = 2.5ms (OCCT1, OCCT0 = 0, 0 and CTDIV = 1)	**1.25**	2.50	**3.75**	ms
		t_{OCC} = 5ms (OCCT1, OCCT0 = 0, 1 and CTDIV = 1)	**2.5**	5	**7.5**	ms
		t_{OCC} = 10ms (OCCT1, OCCT0 = 1, 0 and CTDIV = 1)	**5**	10	**15**	ms
		t_{OCC} = 20ms (OCCT1, OCCT0 = 1, 1 and CTDIV = 1)	**10**	20	**30**	ms
OVER-TEMPERATURE PROTECTION SPECIFICATIONS						
Internal Temperature Shutdown Threshold	T_{INTSD}			125		°C
Internal Temperature Hysteresis	T_{HYS}	Temperature drop needed to restore operation after over-temperature shutdown		20		°C
Internal Over-temperature Turn-On Delay Time	t_{ITD}			128		ms
External Temperature Output Current	I_{XT}	Current output capability at TEMP3V pin	**1.2**			mA
External Temperature Limit Threshold	T_{XTF}	Voltage at V_{TEMPI}; Relative to $\frac{V_{TEMP3V}}{13}$ falling edge	**-20**	0	**+20**	mV
External Temperature Limit Hysteresis	T_{XTH}	Voltage at V_{TEMPI} relative to $\frac{V_{TEMP3V}}{13}$	**60**	110	**160**	mV
External Temperature Monitor Delay	t_{XTD}	Delay between activating the external sensor and the internal over-temperature detection		1		ms
External Temperature Autoscan On Time	t_{XTAON}	TEMP3V is ON (3.3V)		5		ms
External Temperature Autoscan Off Time	t_{XTAOFF}	TEMP3V output is off		635		ms
ANALOG OUTPUT SPECIFICATIONS						
Cell Monitor Analog Output Voltage Accuracy	V_{AOC}	$[V_{CELLN} - V_{CELLN-1}]/2$ - AO	**-15**	4	**30**	mV
Cell Monitor Analog Output External Temperature Accuracy	V_{AOXT}	External temperature monitoring accuracy. Voltage error at AO when monitoring TEMPI voltage (measured with TEMPI = 1V)	**-10**		**10**	mV
Internal Temperature Monitor Output Voltage Slope	V_{INTMON}	Internal temperature monitor voltage change		-3.5		mV/°C
Internal Temperature Monitor Output	T_{INT25}	Output at +25°C		1.31		V

Electrical Specifications V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
AO Output Stabilization Time	t_{VSC}	From SCL falling edge at data bit 0 of command to AO output stable within 0.5% of final value. AO voltage steps from 0V to 2V. (C_{AO} = 10pF). (Note 10)			**0.1**	ms
CELL BALANCE SPECIFICATIONS						
Cell Balance Transistor $r_{DS(ON)}$	R_{CB}			5	**10**	Ω
Cell Balance Transistor Current	I_{CB}				**200**	mA
WAKE-UP/SLEEP SPECIFICATIONS						
Device WKUP Pin Voltage Threshold (WKUP Pin Active High - Rising Edge)	V_{WKUP1}	WKUP pin rising edge (WKPOL = 1) Device wakes up and sets WKUP flag HIGH	**3.5**	5.0	**7.0**	V
Device Wkup Pin Hysteresis (WKUP Pin Active High)	$V_{WKUP1 HYS}$	WKUP pin falling edge hysteresis (WKPOL = 1) sets WKUP flag LOW (does not automatically enter sleep mode)		100		mV
Input Resistance On WKUP	R_{WKUP}	Resistance from WKUP pin to VSS (WKPOL = 1)	**250**	360	**450**	kΩ
Device WKUP Pin Active Voltage Threshold (WKUP Pin Active Low-Falling Edge)	V_{WKUP2}	WKUP pin falling edge (WKPOL = 0) Device wakes up and sets WKUP flag HIGH	**V_{BACK} - 2.2**	V_{BACK} - 1.8	**V_{BACK} - 1.4**	V
Device WKUP Pin Hysteresis (WKUP Pin Active Low)	$V_{WKUP2 HYS}$	WKUP pin rising edge hysteresis (WKPOL = 0) sets WKUP flag LOW (does not automatically enter sleep mode)		200		mV
Device Wake-up Delay	t_{WKUP}	Delay after voltage on WKUP pin crosses the threshold (rising or falling) before activating the WKUP bit	**20**	40	**60**	ms
FET CONTROL SPECIFICATIONS						
VFET1 Voltage	V_{VFET1A}		**5.6**		**10.8**	V
	V_{VFET1B}	0°C to +85°C	4.4		10.8	V
VFET2 Voltage	V_{VFET2A}		**8.4**		**14.4**	V
	V_{VFET2B}	0°C to +85°C	6.6		14.4	V
Control Outputs Response Time (CFET, DFET)	t_{CO}	Bit 0 to start of control signal (DFET) Bit 1 to start of control signal (CFET)		1.0		µs
CFET Gate Voltage	VCFET	No load on CFET	**V_{FET2}- 0.5**		**V_{FET2}**	V
DFET Gate Voltage	VDFET	No load on DFET	**V_{FET2}- 0.5**		**V_{FET2}**	V
FET Turn On Current (DFET)	I_{DF}(ON)	DFET voltage = 0 to V_{FET2} -1.5V -20°C to +85°C	80	200	450	µA
FET Turn On Current (CFET)	I_{CF}(ON)	CFET voltage = 0 to V_{FET2} - 1.5V -20°C to +85°C	80	200	450	µA
FET Turn Off Current (DFET)	I_{DF}(OFF)	DFET voltage = FET2 to 1V	**100**	180		mA
DFET Resistance to VSS	R_{DF}(OFF)	VDFET < 1V (When turning off the FET)			**11**	Ω
SERIAL INTERFACE CHARACTERISTICS						
SCL Clock Frequency	f_{SCL}				**400**	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{IN}	Any pulse narrower than the max spec is suppressed			**50**	ns
SCL Falling Edge to SDA Output Data Valid	t_{AA}	From SCL falling crossing V_{IH}(min), until SDA exits the V_{IL}(max) to V_{IH}(min) window			**0.9**	µs

Electrical Specifications V_{CC} = 6V to 26.4V and -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Time the Bus Must Be Free Before Start of New Transmission	t_{BUF}	SDA crossing V_{IH}(min) during a STOP condition to SDA crossing V_{IH}(min) during the following START condition	**1.3**			µs
Clock Low Time	t_{LOW}	Measured at the V_{IL}(max) crossing	**1.3**			µs
Clock High Time	t_{HIGH}	Measured at the V_{IH}(min) crossing	**0.6**			µs
Start Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge. Both crossing the V_{IH}(min) level	**0.6**			µs
Start Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing V_{IL}(max) to SCL falling edge crossing V_{IH}(min)	**0.6**			µs
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the V_{IL}(max) to V_{IH}(min) window to SCL rising edge crossing V_{IL}(min)	**100**			ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL falling edge crossing V_{IH}(min) to SDA entering the V_{IL}(max) to V_{IH}(min) window	**0**		0.9	µs
Stop Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing V_{IH}(min) to SDA rising edge crossing V_{IL}(max)	**0.6**			µs
Stop Condition Hold Time	$t_{HD:STO}$	From SDA rising edge to SCL falling edge. Both crossing V_{IH}(min)	**0.6**			µs
Data Output Hold Time	t_{DH}	From SCL falling edge crossing V_{IL}(max) until SDA enters the V_{IL}(max) to V_{IH}(min) window. (Note 9)	**0**			ns
SDA and SCL Rise Time	t_R	From V_{IL}(max) to V_{IH}(min) (Notes 11, 12)	**20 + 0.1 x Cb**		**300**	ns
SDA and SCL Fall Time	t_F	From V_{IH}(min) to V_{IL}(max) (Notes 11, 12)	**20 + 0.1 x Cb**		**300**	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip (Notes 11, 12)	**10**		**400**	pF
SDA and SCL Bus Pull-up Resistor Off Chip	R_{OUT}	Maximum is determined by t_R and t_F. For C_B = 400pF, max is about 2kΩ ~ 2.5kΩ For C_B = 40pF, max is about 15kΩ to 20kΩ (Notes 11, 12)	**1**			kΩ
Input Leakage Current (SCL, SDA)	I_{LI}		**-10**		**10**	µA
Input Buffer Low Voltage (SCL, SDA)	V_{IL}	Voltage relative to V_{SS} of the device	**-0.3**		**V_{RGO} x 0.3**	V
Input Buffer High Voltage (SCL, SDA)	V_{IH}	Voltage relative to V_{SS} of the device	**V_{RGO} x 0.7**		**V_{RGO} + 0.1V**	V
Output Buffer Low Voltage (SDA)	V_{OL}	I_{OL} = 1mA			**0.4**	V
SDA and SCL Input Buffer Hysteresis	I^2CHYST	Sleep bit = 0	**0.05 * V_{RGO}**			V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
8. Power-up of the device requires V_{BACK} and VCC to be above the limits specified.
9. The device provides an internal hold time of at least 300ns for the SDA signal to bridge the unidentified region of the falling edge of SCL.
10. Maximum output capacitance = 15pF.
11. These are I^2C specific parameters and are not production tested. However, they are used to set conditions for testing to validate specification.
12. Limits should be considered typical and are not production tested.

Timing Diagrams

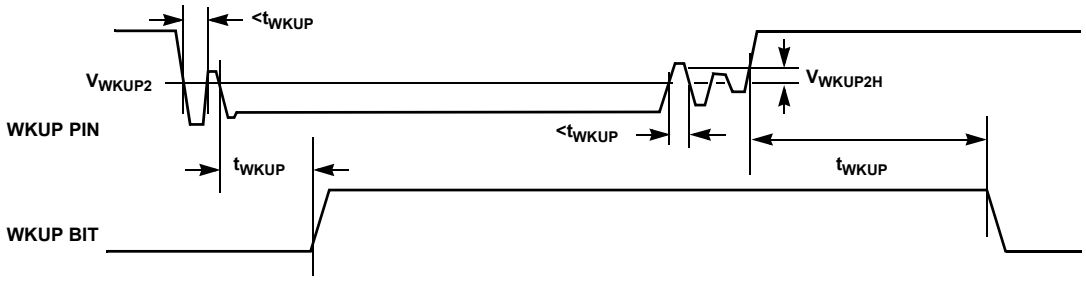


FIGURE 3. WAKE-UP TIMING (WKPOL = 0)

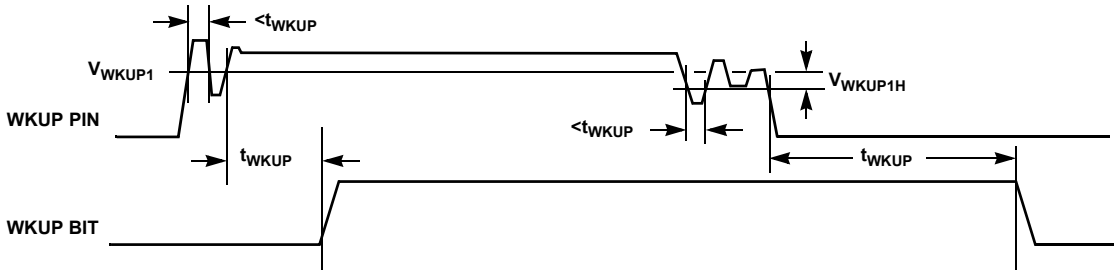


FIGURE 4. WAKE-UP TIMING (WKPOL = 1)

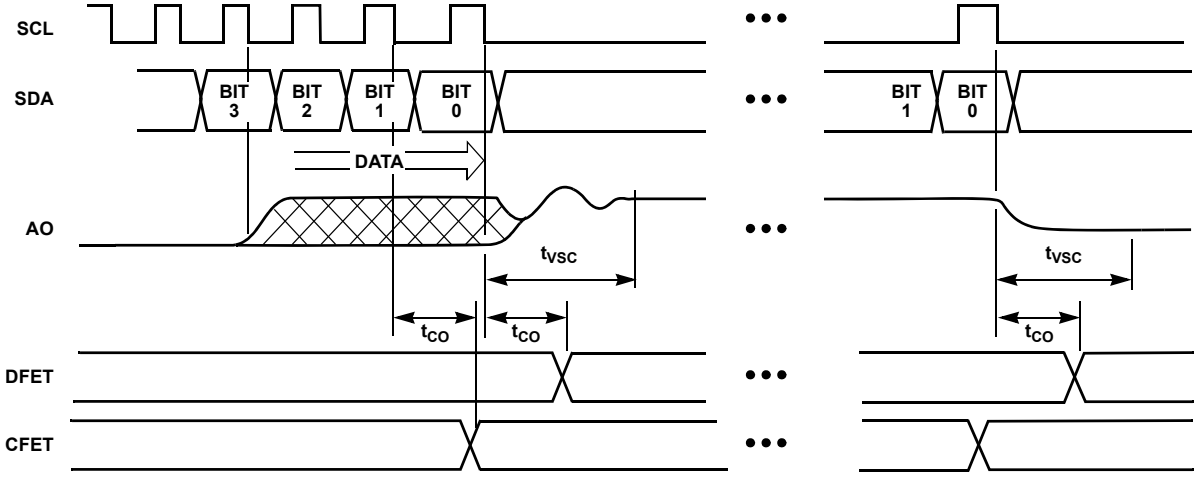


FIGURE 5. CHANGE IN VOLTAGE SOURCE, FET CONTROL

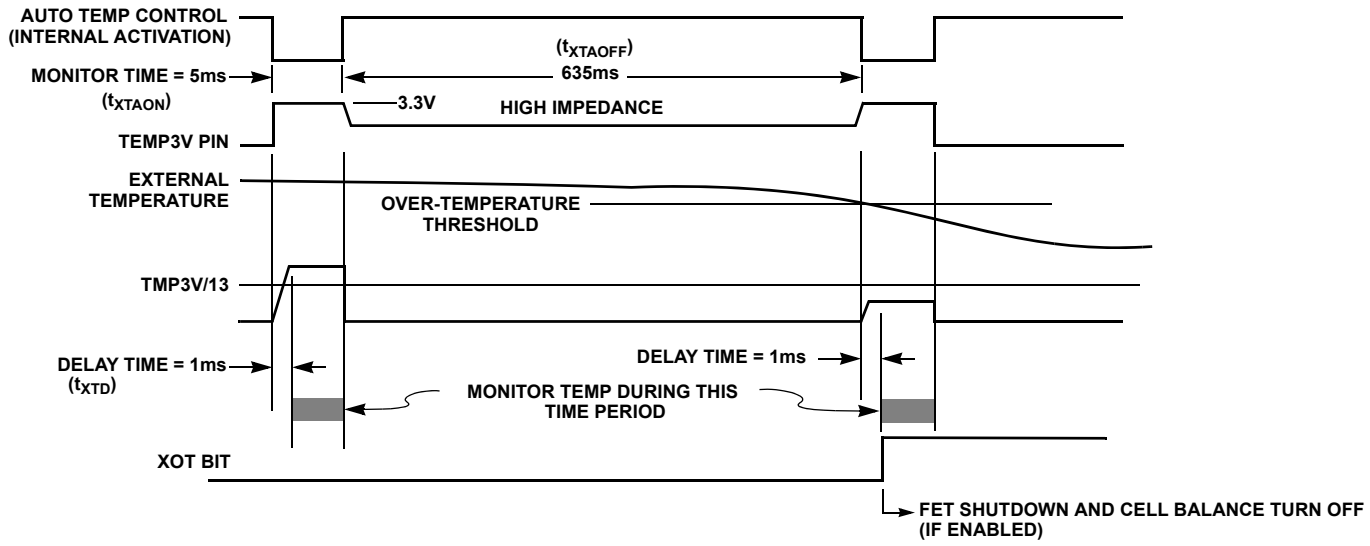


FIGURE 6. AUTOMATIC TEMPERATURE SCAN

(Assumes DENOCD and DENSCD bits are '0')

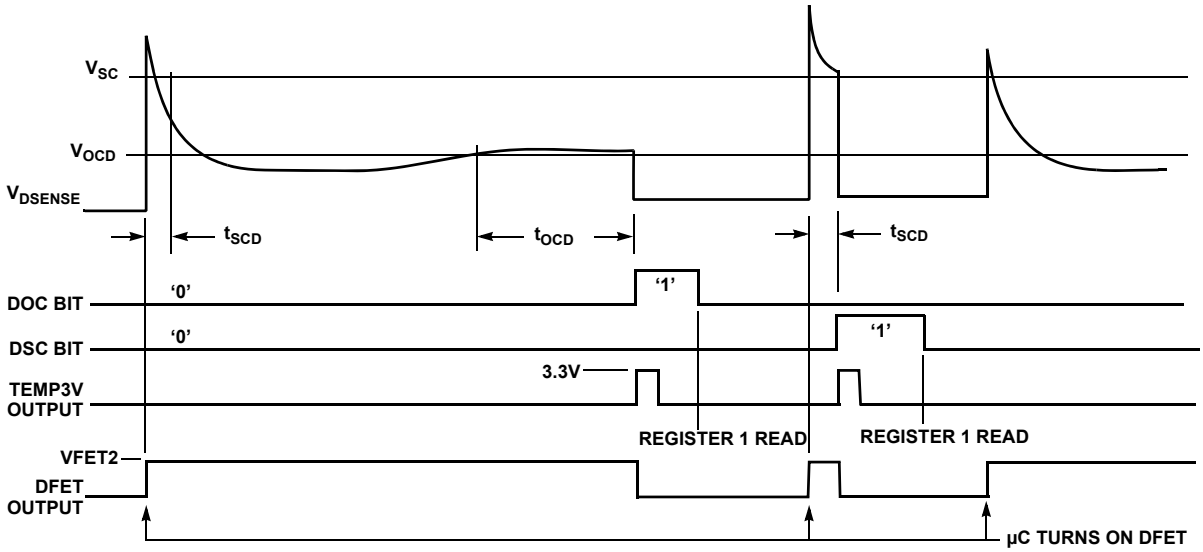


FIGURE 7. DISCHARGE OVERCURRENT/SHORT-CIRCUIT MONITOR

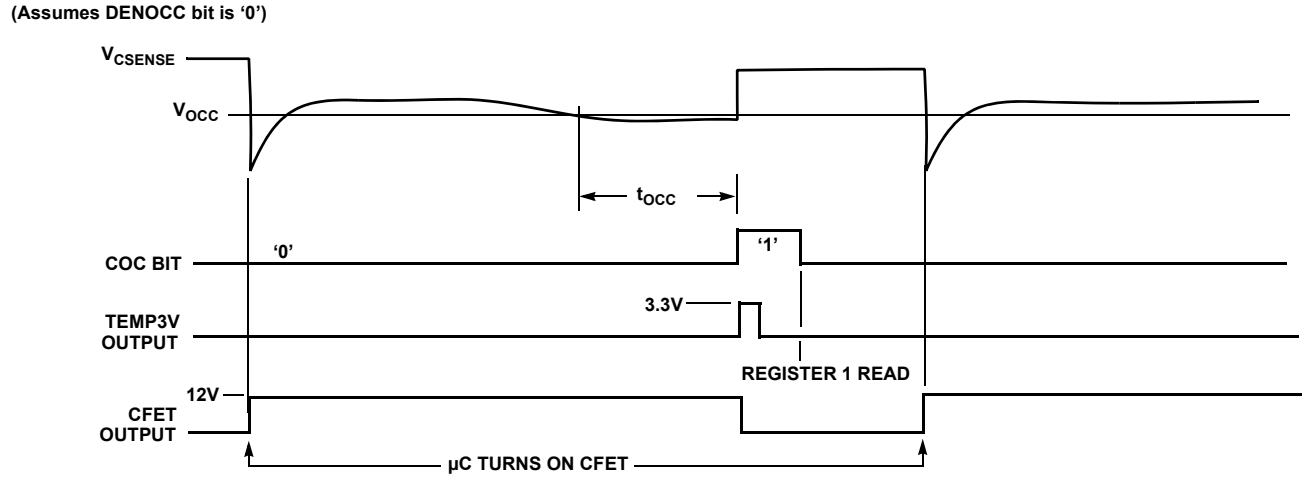


FIGURE 8. CHARGE OVERCURRENT MONITOR

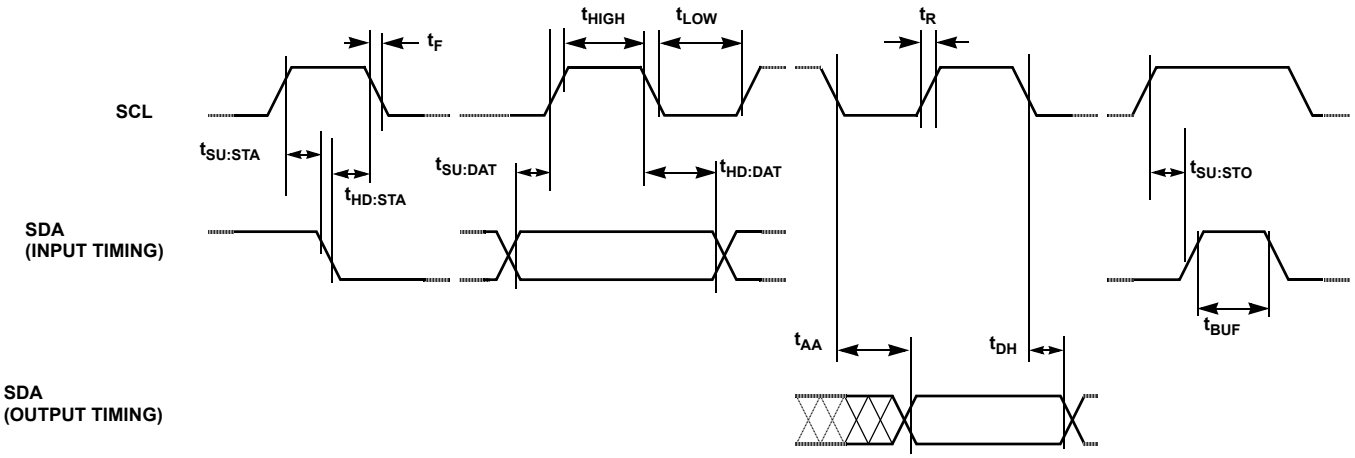


FIGURE 9. SERIAL INTERFACE BUS TIMING

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: CHANGES ALLOWED	CHANGING: STATE NOT KNOWN
	MAY CHANGE FROM LOW TO HIGH	WILL CHANGE FROM LOW TO HIGH		N/A	CENTER LINE IS HIGH IMPEDANCE
	MAY CHANGE FROM HIGH TO LOW	WILL CHANGE FROM HIGH TO LOW			

FIGURE 10. SYMBOL TABLE

Registers

TABLE 2. REGISTERS

ADDR	REGISTER	READ/ WRITE	7	6	5	4	3	2	1	0
00H	Config/Op Status	Read only	Reserved	Reserved	1	WKUP WKUP pin Status	Reserved	Reserved	Reserved	Reserved
01H	Operating Status (Note 15)	Read only	Reserved	Reserved	XOT Ext Over-Temp	IOT Int Over-Temp	LDFAIL Load Fail (VMON)	DSC Short-Circuit	DOC Discharge OC	COC Charge OC
02H	Cell Balance	Read/Write	Reserved	CB6ON	CB5ON	CB4ON	CB3ON	CB2ON	CB1ON	Reserved
				Cell Balance FET Control Bits						
03H	Analog Out	Read/Write	UFLG1 User Flag 1	UFLG0 User Flag 0	Reserved	Reserved	AO3	AO2	AO1	AO0
							Analog Output Select Bits			
04H	FET Control	Read/Write	SLEEP Force Sleep (Note 16)	LDMONEN Turn On VMON Connection	Reserved	Reserved	Reserved	Reserved	CFET Turn On Charge FET (Note 17)	DFET Turn On Discharge FET (Note 17)
05H	Discharge Set	Read/Write (Write only if DISSETEN bit set)	DENOCD	OCDV1	OCDV0	DENSCD	SCDV1	SCDV0	OCDT1	OCDT0
			Turn Off Automatic OCD control	Overcurrent Discharge Threshold Voltage		Turn Off Automatic SCD control	Short-Circuit Discharge Threshold Voltage		Overcurrent Discharge Time-out	
06H	Charge Set	Read/Write (Write only if CHSETEN bit set)	DENOCC	OCCV1	OCCV0	SCLONG Long Short-circuit Delay	CTDIV Divide Charge Time by 32	DTDIV Divide Discharge Time by 64	OCCT1	OCCT0
			Turn Off Automatic OCC control	Overcurrent Charge Threshold Voltage					Overcurrent Charge Time-out	
07H	Feature Set	Read/Write (Write Only if FSETEN Bit Set)	ATMPOFF Turn Off Automatic External Temp Scan	DIS3 Disable 3.3V Reg. (Device Requires External 3.3V)	TMP3ON Turn-On Temp3V	DISXTSD Disable External Thermal Shutdown	DISITSD Disable Internal Thermal Shutdown	POR Force POR	DISWKUP Disable WKUP pin	WKPOL Wake-Up Polarity
08H	Write Enable	Read/Write	FSETEN Enable Feature Set Writes	CHSETEN Enable Charge Set Writes	DISSETEN Enable Discharge Set Writes	UFLG3 User Flag 3	UFLG2 User Flag 2	Reserved	Reserved	Reserved
09H:FFH	Reserved	NA	Reserved							

NOTES:

13. A ‘1’ written to a control or configuration bit causes the action to be taken. A ‘1’ read from a status bit indicates that the condition exists.
14. “Reserved” indicates that the bit or register is reserved for future expansion. When writing to addresses 2, 3, 4, and 8: write a reserved bit with the value ‘0’. Do not write to reserved registers at addresses 09H through FFH. Ignore reserved bits that are returned in a read operation.
15. These status bits are automatically cleared when the register is read. All other status bits are cleared when the condition is cleared.
16. This SLEEP bit is cleared on initial power up by the WKUP pin going high (when WKPOL = ”1”), by the WKUP pin going low (when WKPOL = ”0”), or by writing a ‘0’ to the location with an I^2C command.
17. When the automatic responses are enabled, these bits are automatically reset by hardware when an overcurrent or short-circuit condition turns off the FETs. At all other times, an I^2C write operation controls the output to the respective FET and a read returns the current state of the FET drive output circuit (though not the actual voltage at the output pin).

Status Registers

TABLE 3. CONFIG/OP STATUS REGISTER (ADDR: 00H)

BIT	FUNCTION	DESCRIPTION
7, 6, 3, 2, 1, 0	Reserved	Reserved for future expansion.
5	1	This bit is always a '1'.
4	WKUP Wakeup pin status	This bit is set and reset by hardware. When 'WKPOL' is HIGH: • 'WKUP' bit HIGH = WKUP pin > Threshold voltage • 'WKUP' bit LOW = WKUP pin < Threshold voltage When 'WKPOL' is LOW: • 'WKUP' bit HIGH = WKUP pin < Threshold voltage • 'WKUP' bit LOW = WKUP pin > Threshold voltage

TABLE 4. OPERATING STATUS REGISTER (ADDR: 01H)

BIT	FUNCTION	DESCRIPTION
7, 6	Reserved	Reserved for future expansion.
5	XOT Ext Over-temp	This bit is set to '1' when the external temperature sensor input indicates an over-temperature condition. If the over-temperature condition has cleared, this bit is reset when the register is read.
4	IOT Int Over-temp	This bit is set to '1' when the internal temperature sensor input indicates an over-temperature condition. If the over-temperature condition has cleared, this bit is reset when the register is read.
3	LDFAIL Load Fail (VMON)	When the VMON function is enabled (LDMONEN = 1), this bit is set to '1' by hardware when a discharge overcurrent or short-circuit condition occurs. If the load fail condition is cleared or under a light load, the bit is reset when the register is read.
2	DSC Short-Circuit	This bit is set by hardware when a short-circuit condition occurs during discharge. If the discharge short-circuit condition is removed, the bit is reset when the register is read.
1	DOC Discharge OC	This bit is set by hardware when an overcurrent condition occurs during discharge. If the discharge overcurrent condition is removed, the bit is reset when the register is read.
0	COC Charge OC	This bit is set by hardware when an overcurrent condition occurs during charge. If the charge overcurrent condition is removed, the bit is reset when the register is read.

Control Registers

TABLE 5. CELL BALANCE CONTROL REGISTER (ADDR: 02H)

CONTROL REGISTER BITS						BALANCE
BIT 6 CB5ON	BIT 5 CB4ON	BIT 4 CB4ON	BIT 3 CB3ON	BIT 2 CB2ON	BIT 1 CB1ON	
x	x	x	x	x	1	Cell1 ON
x	x	x	x	x	0	Cell1 OFF
x	x	x	x	1	x	Cell2 ON
x	x	x	x	0	x	Cell2 OFF
x	x	x	1	x	x	Cell3 ON
x	x	x	0	x	x	Cell3 OFF
x	x	1	x	x	x	Cell4 ON
x	x	0	x	x	x	Cell4 OFF
x	1	x	x	x	x	Cell5 ON
x	0	x	x	x	x	Cell5 OFF
1	x	x	x	x	x	Cell6 ON
0	x	x	x	x	x	Cell6 OFF
Bit 7 and Bit 0	Reserved					

TABLE 6. ANALOG OUT CONTROL REGISTER (ADDR: 03H)

BITS	FUNCTION		DESCRIPTION	
7	UFLG1 User Flag 1		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
6	UFLG0 User Flag 0		General purpose flag usable by microcontroller software. This bit is battery backed up, even when RGO turns off.	
5:4	RESERVED		Reserved for future expansion.	
BIT 3 AO3	BIT 2 AO2	BIT 1 AO1	BIT 0 AO0	OUTPUT VOLTAGE
0	0	0	0	High Impedance Output (Low Power State) *Remember to reset the AO3:AO0 bits to '0000' after measurements to minimize unnecessary current draw from the cells.*
0	0	0	1	$V(V_{CELL1}) - V(V_{CELL0})$
0	0	1	0	$V(V_{CELL2}) - V(V_{CELL1})$
0	0	1	1	$V(V_{CELL3}) - V(V_{CELL2})$
0	1	0	0	$V(V_{CELL4}) - V(V_{CELL3})$
0	1	0	1	$V(V_{CELL5}) - V(V_{CELL4})$
0	1	1	0	$V(V_{CELL6}) - V(V_{CELL5})$
1	0	0	0	External Temperature
1	0	0	1	Internal Temperature Sensor Voltage V(TEMPI)
Other cases				Reserved

Configuration Registers

The device is configured for specific application requirements using the Configuration Registers. The configuration registers consist of SRAM memory. In the wake-up state, this memory is powered by the RGO output. In a sleep state, this memory is powered by VBACK.

TABLE 7. FET CONTROL REGISTER (ADDR: 04H)

BIT	FUNCTION	DESCRIPTION
7	SLEEP Force Sleep	Setting this bit to '1' forces the device to go into a sleep condition. This turns off both FET outputs, the cell balance outputs, and the voltage regulator. This also resets the CFET, DFET, and CB6ON:CB1ON bits. The SLEEP bit is automatically reset to '0' when the device wakes up. This bit does not reset the AO3:AO0 bits (if the WKUP pin is Active, when attempting to put the device into the Sleep mode, then the SLEEP bit needs to be reset from '1' to '0' before setting it to '1' to initiate sleep).
6	LDMONEN Turn on VMON connection	Writing a '1' to this bit turns on the VMON circuit. Writing a '0' to this bit turns off the VMON circuit. As such, the microcontroller has full control of the operation of this circuit.
5:2	RESERVED	Reserved for future expansion.
1	CFET	Setting this bit to '1' turns on the charge FET. Setting this bit to '0' turns off the charge FET. This bit is automatically reset in the event of a charge overcurrent condition, unless the automatic response is disabled by the DENOCC bit. This bit is automatically reset in the event of an external over-temperature condition, unless the response is disabled by the DISXTSD bit. This bit is automatically reset in the event of an internal over-temperature condition, unless the response is disabled by the DISITSD bit.
0	DFET	Setting this bit to '1' turns on the discharge FET. Setting this bit to '0' turns off the discharge FET. This bit is automatically reset in the event of a discharge overcurrent or discharge short-circuit condition, unless the automatic response is disabled by the DENOCD or DENSCD bits. This bit is automatically reset in the event of an external over-temperature condition, unless the response is disabled by the DISXTSD bit. This bit is automatically reset in the event of an internal over-temperature condition, unless the response is disabled by the DISITSD bit.

TABLE 8. DISCHARGE SET CONFIG REGISTER (ADDR: 05H)

SETTING	FUNCTION	DESCRIPTION
Bit 7	DENOCD Turn off automatic OC discharge control	When set to '0', a discharge overcurrent condition automatically turns off the FETs. When set to '1', a discharge overcurrent condition will not automatically turn off the FETs. In either case, this condition sets the DOC bit, which also turns on the TEMP3V output.
BIT 6 OCDV1	**BIT 5 OCDV0**	**OVERCURRENT DISCHARGE VOLTAGE THRESHOLD**
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V
Bit 4	DENSCD Turn off automatic SC discharge control	When set to '0', a discharge short-circuit condition turns off the FETs. When set to '1', a discharge short-circuit condition does not automatically turn off the FETs. In either case, the condition sets the SCD bit, which also turns on the TEMP3V output.
BIT 3 SCDV1	**BIT 2 SCDV0**	**SHORT-CIRCUIT DISCHARGE VOLTAGE THRESHOLD**
0	0	V_{SCD} = 0.20V
0	1	V_{SCD} = 0.35V
1	0	V_{SCD} = 0.65V
1	1	V_{SCD} = 1.20V
BIT 1 OCDT1	**BIT 0 OCDT0**	**OVERCURRENT DISCHARGE TIME-OUT**
0	0	t_{OCD} = 160ms (2.5ms if DTDIV = 1)
0	1	t_{OCD} = 320ms (5ms if DTDIV = 1)
1	0	t_{OCD} = 640ms (10ms if DTDIV = 1)
1	1	t_{OCD} = 1280ms (20ms if DTDIV = 1)

TABLE 9. CHARGE/TIME SCALE CONFIG REGISTER (ADDR: 06H)

SETTING	FUNCTION	DESCRIPTION
Bit 7	DENOCC Turn off automatic OC charge control	When set to '0', a charge overcurrent condition automatically turns off the FETs. When set to '1', a charge overcurrent condition does not automatically turn off the FETs. In either case, this condition sets the COC bit, which also turns on the TEMP3V output.
BIT 6 OCCV1	**BIT 5 OCCV0**	**OVERCURRENT CHARGE VOLTAGE THRESHOLD**
0	0	V_{OCD} = 0.10V
0	1	V_{OCD} = 0.12V
1	0	V_{OCD} = 0.14V
1	1	V_{OCD} = 0.16V
Bit 4	SCLONG Short-circuit long delay	When this bit is set to '0', a short-circuit needs to be in effect for 190µs before a shutdown begins. When this bit is set to '1', a short-circuit needs to be in effect for 10ms before a shutdown begins.
Bit 3	CTDIV Divide charge time by 32	When set to '1', the charge overcurrent delay time is divided by 32. When set to '0', the charge overcurrent delay time is divided by 1.
Bit 2	DTDIV Divide discharge time by 64	When set to '1', the discharge overcurrent delay time is divided by 64. When set to '0', the discharge overcurrent delay time is divided by 1.
BIT 1 OCCT1	**BIT 0 OCCT0**	**OVERCURRENT CHARGE TIME-OUT**
0	0	t_{OCC} = 80ms (2.5ms if CTDIV=1)
0	1	t_{OCC} = 160ms (5ms if CTDIV=1)
1	0	t_{OCC} = 320ms (10ms if CTDIV=1)
1	1	t_{OCC} = 640ms (20ms if CTDIV=1)

TABLE 10. FEATURE SET CONFIGURATION REGISTER (ADDR: 07H)

BIT	FUNCTION	DESCRIPTION
7	ATMPOFF Turn off automatic external temp scan	When set to '1', this bit disables the automatic temperature scan. When set to '0', the temperature is turned on for 5ms in every 640ms.
6	DIS3 Disable 3.3V reg	Setting this bit to '1' disables the internal 3.3V regulator. Setting this bit to '1' requires that there be an external 3.3V regulator connected to the RGO pin.
5	TMP3ON Turn on Temp 3.3V	Setting this bit to '1' turns ON the TEMP3V output to the external temperature sensor. The output will remain on as long as this bit remains '1'.
4	DISXTSD Disable external thermal shutdown	Setting this bit to '1' disables the automatic shutdown of the cell balance and power FETs in response to an external over-temperature condition. While the automatic response is disabled, the XOT flag is set so the microcontroller can initiate a shutdown based on the XOT flag.
3	DISITSD Disable internal thermal shutdown	Setting this bit to '1' disables the automatic shutdown of the cell balance and power FETs in response to an internal over-temperature condition. While the automatic response is disabled, the IOT flag is set so the microcontroller can initiate a shutdown based on the IOT flag.
2	POR Force POR	Setting this bit to '1' forces a Power On Reset (POR) condition. This resets all internal registers to zero.
1	DISWKUP Disable WKUP pin	Setting this bit to '1' disables the WKUP pin function. CAUTION: Setting this pin to '1' disables hardware wake-up functionality. If the device then goes to sleep, it cannot be awakened without an I^2C command that resets this bit, or by power cycling the device.
0	WKPOL Wake-up polarity	Setting this bit to '1' sets the device to wake up on a rising edge at the WKUP pin. Setting this bit to '0' sets the device to wake up on a falling edge at the WKUP pin. When WKPOL= 0, limit the maximum voltage on the WKUP pin to no more than the voltage on VBACK.

TABLE 11. WRITE ENABLE REGISTER (ADDR: 08H)

BIT	FUNCTION	DESCRIPTION
7	FSETEN Enable discharge set writes	When set to '1', allows writes to the Feature Set register. When set to '0', prevents writes to the Feature Set register (Addr: 07H). Default on initial power-up is '0'.
6	CHSETEN Enable charge set writes	When set to '1', allows writes to the Charge Set register. When set to '0', prevents writes to the Feature Set register (Addr: 06H). Default on initial power-up is '0'.
5	DISSETEN Enable discharge set writes	When set to '1', allows writes to the Discharge Set register (Addr: 05H). When set to '0', prevents writes to the Feature Set register. Default on initial power-up is '0'.
4	UFLG3 User Flag 3	General purpose flag usable by microcontroller software. This bit is powered by the voltage on VBACK when RGO turns off.
3	UFLG2 User Flag 3	General purpose flag usable by microcontroller software. This bit is powered by the voltage on VBACK when RGO turns off.
2, 1, 0	RESERVED	Reserved for future expansion.

Device Description

Instructed by the microcontroller, the ISL94208 performs cell voltage monitoring and cell balancing operations, overcurrent and short-circuit monitoring with automatic pack shutdown using built-in selectable time delays, and automatic turn off of the power FETs and cell balancing FETs in an over-temperature condition. All automatic functions of the ISL94208 can be turned off and the microcontroller can manage the operations through software.

Battery Connection

The ISL94208 supports packs of four to six series-connected Li-ion cells. One connection, with input filtering components, for six cells is shown in Figure 11. Input capacitors are not normally needed and are not recommended. These capacitors rapidly charge when the batteries connect. This surge current is limited only by the input resistors and may be high enough to damage elements in the IC. If capacitors are needed, use the largest possible series input resistor.

When using input filters, the time constants on all inputs should be the same.

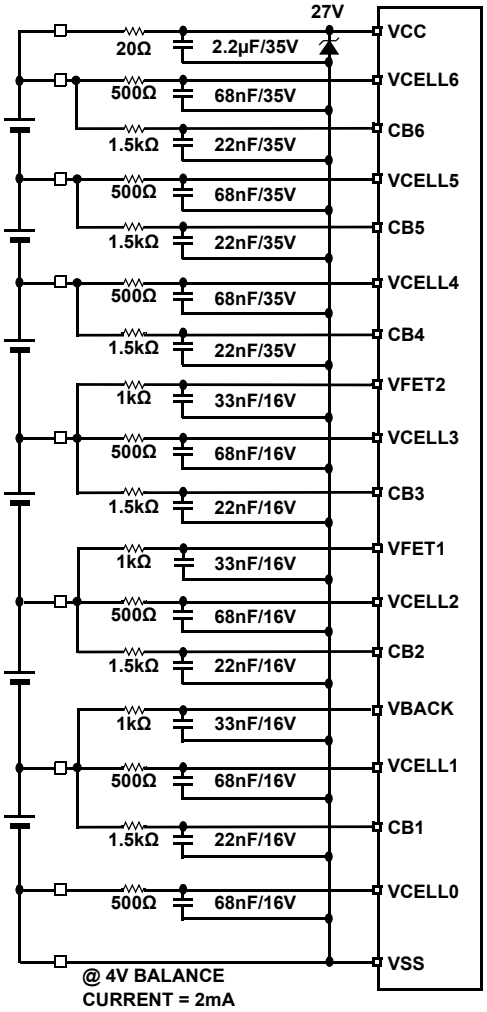
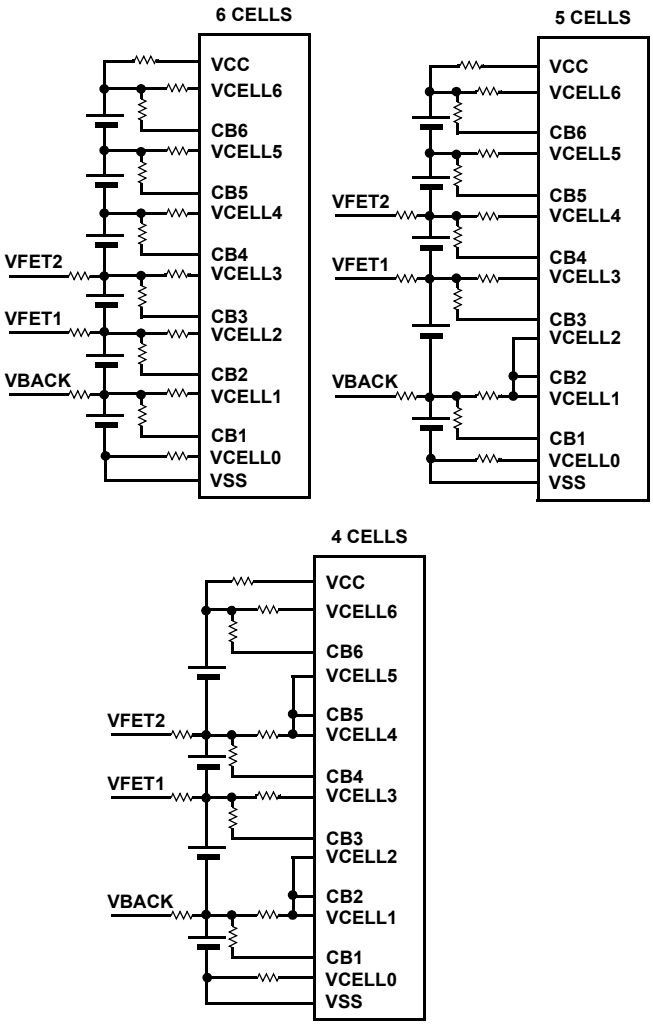


FIGURE 11. ISL94208 INPUT FILTERS

Connection guidelines for systems using 4, 5, or 6 cells are shown in Figure 12 (minus the input filters and diodes).



Note: Multiple cells can be connected in parallel.

FIGURE 12. BATTERY CONNECTION OPTIONS

System Power-Up/Power-Down

The ISL94208 powers up when the voltage on V_{BACK} and V_{CC} both exceed their POR threshold. At this time, the ISL94208 wakes up and turns on the RGO output.

RGO provides a regulated 3.3VDC ±10% voltage at pin RGO. It does this by using a control voltage on the RGC pin to drive an external NPN transistor (see Figure 13). The transistor should have a beta of at least 70 to provide ample current to the device and external circuits and should have a breakdown voltage greater than 30V (preferably 50V). The voltage at the emitter of the NPN transistor is monitored and regulated to 3.3V by the control signal RGC. RGO also powers most of the ISL94208 internal circuits. A 500Ω resistor is recommended in the collector of the NPN transistor to minimize initial current surge when the regulator turns on.

When the device is powered up, it remains in a wake-up state until it is put to sleep by the microcontroller (typically when the cells drop too low in voltage) or until the V_{BACK} or V_{CC} voltages drop below their POR threshold.

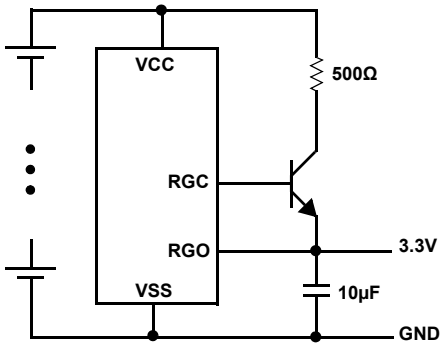


FIGURE 13. VOLTAGE REGULATOR CIRCUITS

WKUP Pin Operation

There are two ways to design a wake-up of the ISL94208: WKPOL = 0 and WKPOL = 1. These are described in the following sections.

WKPOL = 0

In an active Low connection (WKPOL = '0' - default), the device wakes up when the WKUP pin goes Low when compared to a reference based on the V_{BACK} voltage. This normally happens in a pack when a charger connects to the battery terminals.

To put the device to sleep, when configured as an active Low WKUP, if the WKUP pin is High, then a single rising edge on the SLEEP bit puts the device to sleep. However, if the WKUP pin is Low, the device needs to see a falling edge of the SLEEP bit (or the WKUP pin needs to be pulled High), before the rising edge of the SLEEP bit can force the device into the Sleep mode. A WKUP/Sleep Timing timing diagram for WKPOL = 0 is shown in Figure 16.

When using the falling edge option, the voltage on the WKUP pin should not exceed the voltage on VBACK for extended periods of time. Also, if WKUP is pulled up to the VBACK pin (or CELL1) then the connection of the charger or load should only maintain the WKUP connection for a short time to minimize the drain of CELL 1. Also, for the falling edge option, maintaining the WKUP voltage low results in higher VBACK current. See the electrical table. For an example wake-up circuit, see Figure 15.

WKPOL = 1

In an active High connection (WKPOL = '1'), the device wakes up when the WKUP pin is pulled high, normally by a connection through an external switch.

To put the device to sleep, when configured as an active High WKUP, if the WKUP pin is Low, then a single rising edge on the SLEEP bit puts the device to sleep. However, if the WKUP pin is High, the device needs to see a falling edge of the SLEEP bit, (or the WKUP pin needs to be pulled Low), before the rising edge of the SLEEP bit can force the device into the Sleep mode. A WKUP/Sleep Timing timing diagram for WKPOL = 1 is shown in Figure 15. See an example wake-up circuit, using the microcontroller to control wake-up, in Figure 15. This microcontroller would need to be powered by a separate supply.

In either active Low or active High wake-up, there is a filter that ignores WKUP pulses that are shorter than a t_{WKUP} period. If the device is in SLEEP mode when the WKUP signal goes active, then the regulator turns on to power the wake-up circuits. However, the device is not fully awake, it is in a pseudo sleep mode, until the wake-up condition is latched, after which the device is fully active.

When using the active High wake-up option, it is not recommended that the WKUP voltage remain high while the device is in sleep mode. Doing so results in excessive current on the VBACK pin.

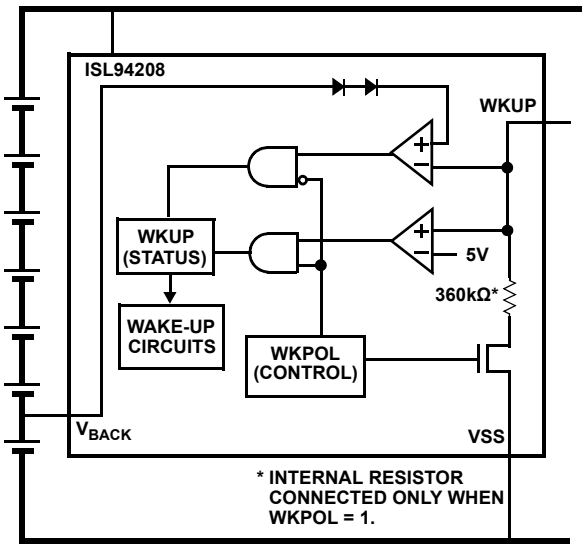
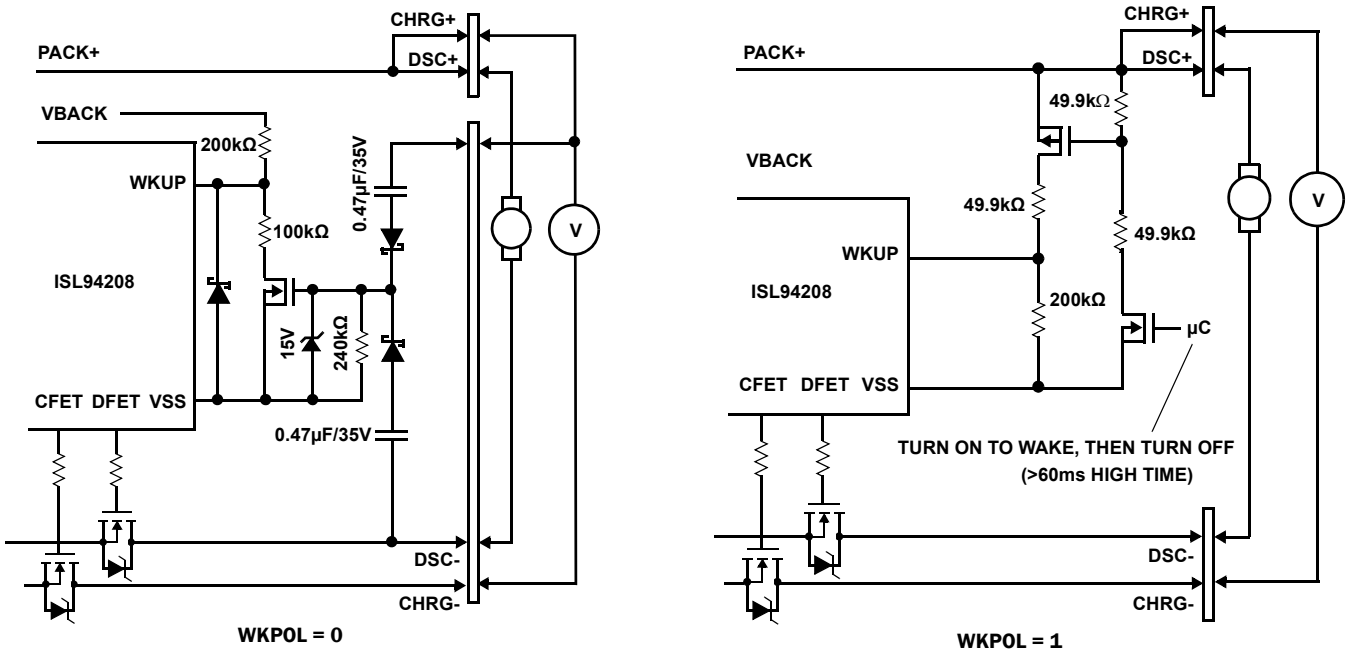


FIGURE 14. SIMPLIFIED WAKE-UP CONTROL CIRCUITS



NOTES:

18. WKPOL = 0 - The DSC- connection wakes the ISL94208 when the load connects.
19. WKPOL = 0 - The charger connection has three terminals. One terminal indicates that the charger is connected.
20. WKPOL = 1 - This connection wakes the pack under control of a microcontroller. This microcontroller needs to be powered by a separate regulator.

FIGURE 15. EXAMPLE EXTERNAL WAKE-UP CIRCUITS

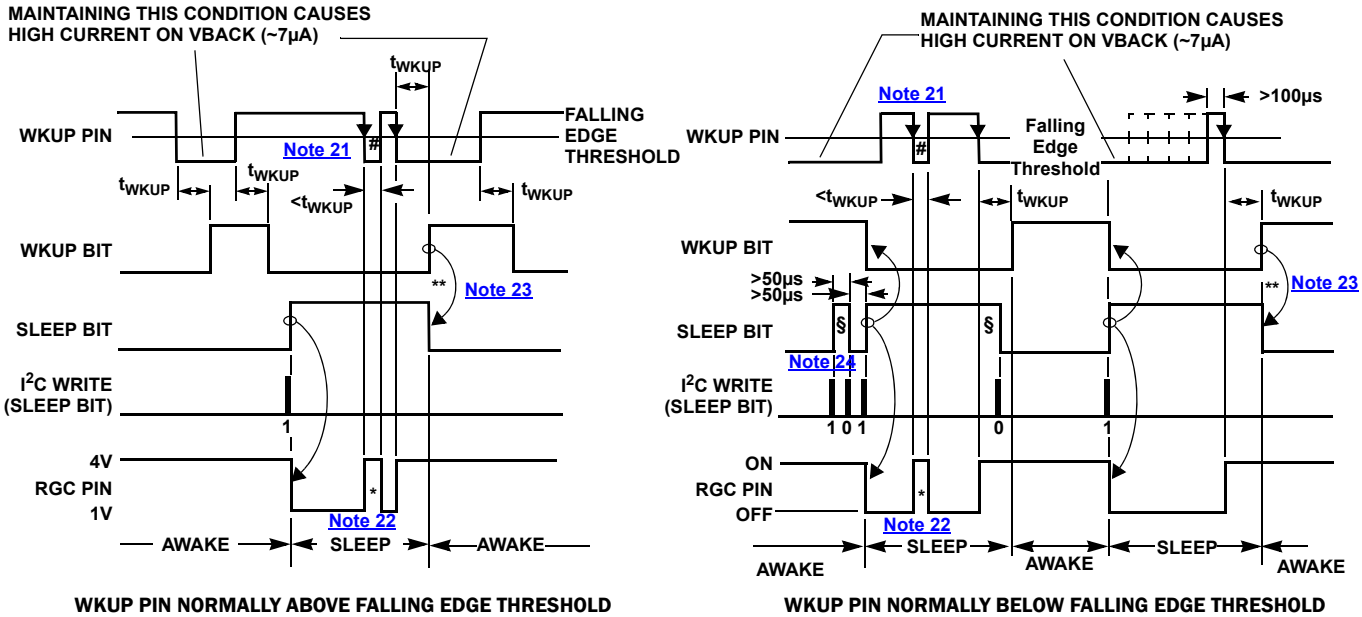
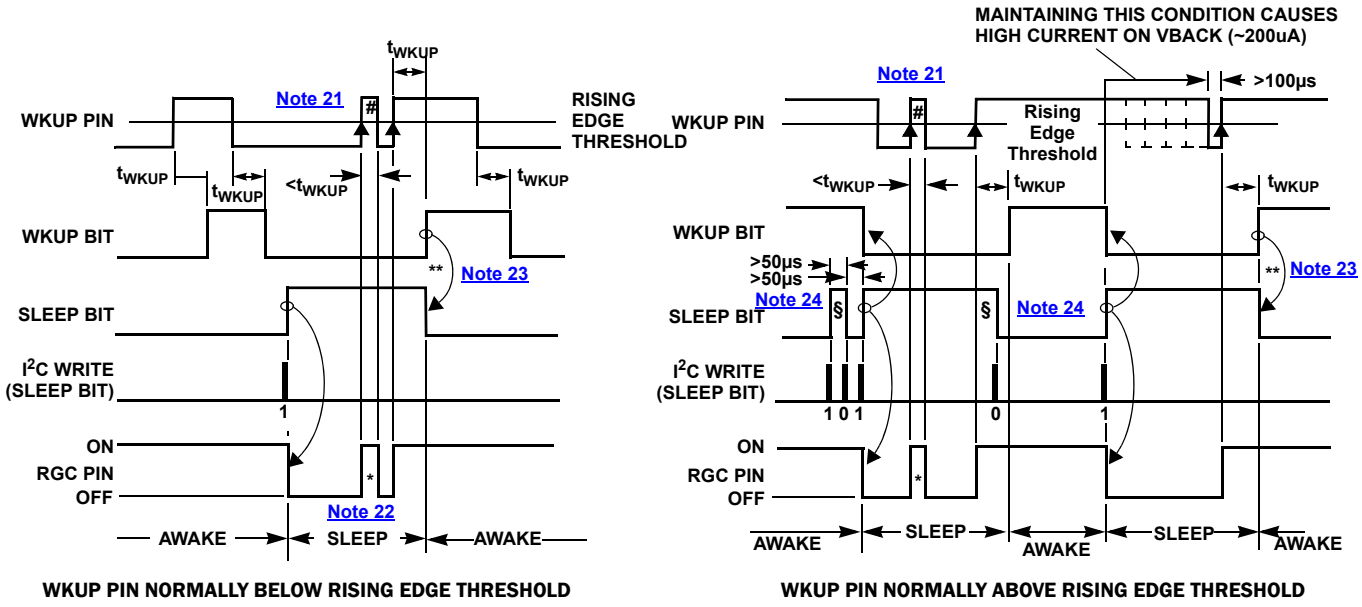


FIGURE 16. SLEEP/WAKE-UP TIMING (WKPOL BIT = 0)



NOTES:

21. # These are Glitches on the WKUP pin that are not long enough to exceed the internal filter and are not detected as valid signals.
22. * These periods are pseudo-sleep. The regulator turns on to power the wake-up circuits, but Wake-up is not complete until the WKUP bit is latched.
23. ** The rising edge of the WKUP bit resets the SLEEP bit, if not already reset.
24. § When the WKUP pin is Active during Awake periods, the device needs a falling edge on the SLEEP bit (while the WKUP pin is above the threshold) before the SLEEP bit can force sleep. The diagram shows two methods of doing this.

FIGURE 17. SLEEP/WAKEUP TIMING (WKPOL BIT = 1)

Protection Functions

In the default recommended condition, the ISL94208 automatically responds to discharge overcurrent, discharge short-circuit, charge overcurrent, internal over-temperature, and external over-temperature conditions. The designer can set optional over-ride conditions that allow the response to be dictated by the microcontroller. These are discussed in the following sections.

Overcurrent Safety Functions

The ISL94208 continually monitors the discharge current by monitoring the voltage at the CSENSE and DSENSE pins. If that voltage exceeds a selected value for a time exceeding a selected delay, then the device enters an overcurrent or short-circuit protection mode. In these modes, the ISL94208 automatically turns off both power FETs and hence prevents current from flowing through the terminals P+ and P-. See Figure 29 on page 32.

The voltage thresholds and the response times of the overcurrent protection circuits are selectable for discharge overcurrent, charge overcurrent, and discharge short-circuit conditions. The specific settings are determined by bits in the Discharge Set Configuration Register (ADDR:05H) on page 18, and the Charge/Time Scale Configuration Scale Register (ADDR:06H) on page 19. In addition, refer to "Registers" on page 15.

In an overcurrent condition, the ISL94208 automatically turns off the voltage on CFET and DFET pins. The DFET output drives the discharge FET gate low, turning off the FET quickly. The CFET output turns off and allows the gate of the charge FET to be pulled low through a resistor.

By turning off the FETs the ISL94208 prevents damage to the battery pack caused by excessive current into or out of the cells (as in the case of a faulty charger or short-circuit condition).

When the ISL94208 detects a discharge overcurrent condition, both power FETs are turned off and the DOC bit is set. When the FETs are turned off, the DFET and CFET bits are also reset. The automatic response to overcurrent during discharge is prevented by setting the DENOCD bit to '1'. The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually turn on the load monitor function first (by setting the LDMONEN bit) and monitor the LDFAIL bit to detect that the overcurrent condition has been removed.

When the ISL94208 detects a discharge short-circuit condition, both power FETs are turned off and DSC bit is set. When the FETs are turned off, the DFET and CFET bits are also reset. The automatic response to short-circuit during discharge is prevented by setting the DENSCD bit to '1'. The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually turn on the load monitor function first (by setting the LDMONEN bit) and monitor the LDFAIL bit to detect that the overcurrent condition has been removed.

When the ISL94208 detects a charge overcurrent condition, both power FETs are turned off and COC bit is set. When the FETs are turned off, the DFET and CFET bits are also reset. The automatic response to overcurrent during discharge is prevented by setting the DENOCC bit to '1'. The external microcontroller can turn on the FETs at any time to recover from this condition, but it would usually wait to do this until the cell voltages are not overcharged and that the overcurrent condition has been removed (or the microcontroller could wait until the pack is removed from the charger and then re-attached).

An alternative method of providing the protection function, if desired by the designer, is to turn off the automatic safety response. In this case, the ISL94208 devices still monitor the conditions and set the status bits, but take no action in overcurrent or short-circuit conditions. Safety of the pack depends, instead, on the microcontroller sending commands to the ISL94208 to turn off the FETs.

To facilitate a microcontroller response to an overcurrent condition, especially if the microcontroller is in a low power state, a charge overcurrent flag (COC), a discharge overcurrent flag (DOC), or the short-circuit flag (DSC) being set causes the ISL94208 TEMP3V output to turn on and pull high (see Figure 19). This output can be used as an external interrupt by the microcontroller to wake-up quickly to handle the overcurrent condition.

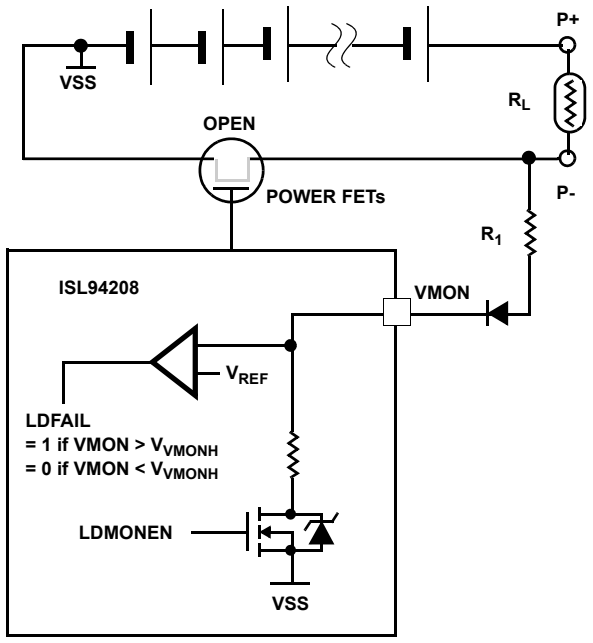


FIGURE 18. LOAD MONITOR CIRCUIT

Load Monitoring

The load monitor function in the ISL94208 (see Figure 18) is used primarily to detect that the load has been removed following an overcurrent or short-circuit condition during discharge. This can be used in a control algorithm to prevent the FETs from turning on while the overload or short-circuit condition remains.

The load monitor can also be used by the microcontroller algorithms after an undervoltage condition on any cells causes the FETs to turn off. Use of the load monitor prevents the FETs from turning on while the load is still present. This minimizes the possible "on-off-on cycles" that can occur when a load is applied in a low capacity pack. It can also be part of a system protection mechanism to prevent the load from turning on automatically. That is, some action must be taken before the pack is again turned on.

The load monitor circuit can be turned on or off by the microcontroller. It is normally turned off to minimize current consumption. It must be activated by the external microcontroller for it to operate. The circuit works by internally connecting the VMON pin to VSS through a resistor. The circuit operates as shown in Figure 18.

In a typical pack operation, when an overcurrent or short-circuit event happens, the DFET turns off, opening the battery circuit to the load. At this time, the R_L is small and the load monitor is initially off. In this condition, the voltage at VMON rises to nearly the pack voltage.

When the power FETs turn off, the microcontroller activates the load monitor by setting the LDMONEN bit. This turns on an internal FET that adds a pull down resistor to the load monitor circuit. While still in the overload condition the combination of the load resistor, an external adjustment resistor (R_1), and the internal load monitor resistor form a voltage divider. R_1 is chosen so that when the load is released to a sufficient level, the LDFAIL condition is reset.

The diode in the VMON circuit is necessary to prevent the VMON voltage from going negative with respect to VSS when a charger connects between P+ and P- and the charger voltage is significantly larger than the battery stack voltage.

Over-Temperature Safety Functions

EXTERNAL TEMPERATURE MONITORING

The external temperature is monitored by using a voltage divider consisting of a fixed resistor and a thermistor. This divider is powered by the ISL94208 TEMP3V output. This output is normally controlled so it is on for only short periods to minimize current consumption.

Without microcontroller intervention, and in the default state, the ISL94208 provides an automatic temperature scan. This scan circuit repeatedly turns on TEMP3V output (and the external temperature monitor) for 5ms out of every 640ms. In this way, the external temperature is monitored even if the microcontroller is asleep.

When the TEMP3V output turns on, the ISL94208 waits 1ms for the temperature reading to stabilize, then compares the external temperature voltage with an internal voltage divider that is set to TEMP3V/13. If the thermistor voltage is below the reference threshold after the delay, an external temperature fail condition exists. To set the external over-temperature limit, set the value of R_X resistor to 12 times the resistance of the thermistor at the desired over-temp threshold.

The TEMP3V output pin also turns on when the microcontroller sets the A03:A00 bits to select that the external temperature voltage. This causes the TEMPI voltage to be placed on A0 and activates (after 1ms) the over-temperature detection. As long as the A03:A00 bits point to the external temperature, the TEMP3V

output remains on. Because of the manual scan of the temperature, it may be desired to turn off the automatic scan, although they can be used at the same time without interference. To turn off the automatic scan, set the ATMPOFF bit.

The microcontroller can override both the automatic temperature scan and the microcontroller controlled temperature scan by setting the TEMP3ON configuration bit. This turns on the TEMP3V output to keep the temperature control voltage on all the time for a continuous monitoring of an over-temperature condition. This likely will consume a significant amount of current, so this feature is usually used for special or test purposes.

PROTECTION

By default, when the ISL94208 detects an internal or external over-temperature condition, the FETs are turned off, the cell balancing function is disabled, and the IOT bit or XOT bit (respectively) is set.

Turning off the FETs in the event of an over-temperature condition prevents continued discharge or charge of the cells when they are overheated. Turning off cell balancing in the event of an over-temperature condition prevents damage to the IC if too many cells are being balanced, which would cause too much power dissipation in the ISL94208.

In the event of an automatic over-temperature condition, cell balancing is prevented and the FETs are held off until the temperature drops below the temperature recovery threshold. During this temperature shutdown period, the microcontroller can monitor the internal temperature through the analog output pin (AO), but any writes to the CFET bit, DFET bit, or cell balancing bits are ignored

The automatic response to an internal over-temperature is prevented by setting the DISITSD bit to '1'. The automatic response to an external over-temperature is prevented by setting the DISXTSD bit to '1'. In either case, it is important for the microcontroller to monitor the internal and external temperature to protect the pack and the electronics in an over-temperature condition.

Analog Multiplexer Selection

The ISL94208 devices can be used to externally monitor individual battery cell voltages and temperatures. Each quantity can be monitored at the analog output pin (AO). The desired voltage is selected using the I^2C interface and the AO3:AO0 bits. See Figure 20 and Table 6 on page 17. Remember to reset the AO3:AO0 bits to '0000' after measurements to minimize unnecessary current draw from the cells.

Voltage Monitoring

Because the voltage on each of the Li-ion Cells is normally higher than the regulated supply voltage, and because the voltages on the upper cells are much higher than is tolerated by a microcontroller, it is necessary to both level shift and divide the voltage before it can be monitored by the microcontroller or an external A/D converter. To get into the voltage range required by the external circuits, the voltage level shifter divides the cell voltage by 2 and references it to VSS. Therefore, a Li-ion cell with a voltage of 4.2V becomes a voltage of 2.1V on the AO pin.

Temperature Monitoring

The voltage representing the external temperature applied at the TEMPI terminal is directed to the AO terminal through a MUX, as selected by the AO control bits (see Figures 19 and 20). The external temperature voltage is not divided by 2 as are the cell voltages. Instead it is a direct reflection of the voltage at the TEMPI pin.

A similar operation occurs when monitoring the internal temperature through the AO output, except there is no external "calibration" of the voltage associated with the internal temperature. For the internal temperature monitoring, the voltage at the output is linear with respect to temperature. See "Electrical Specifications" on page 6 for information about the output voltage at +25°C and the output slope relative to temperature.

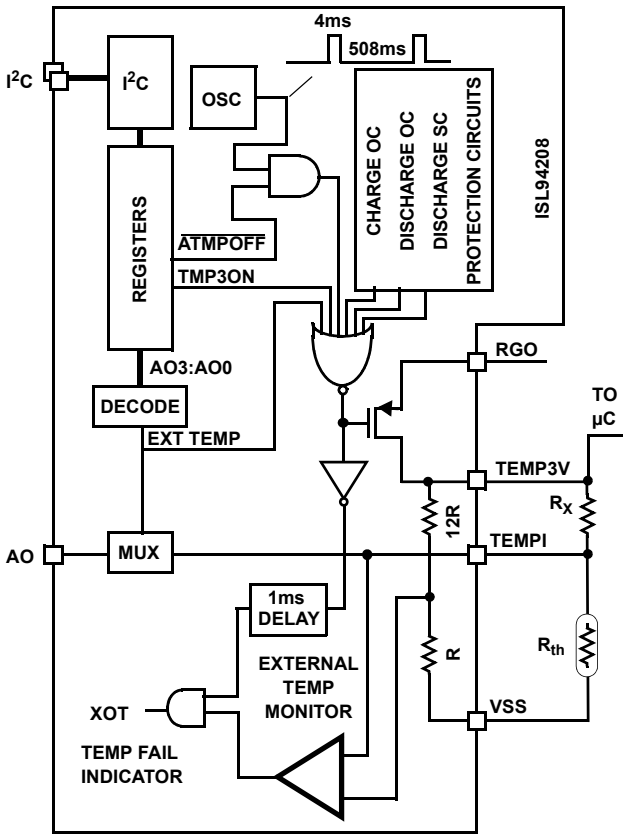


FIGURE 19. EXTERNAL TEMPERATURE MONITORING AND CONTROL

Cell Balancing

Overview

A typical ISL94208 Li-ion battery pack consists of four to six cells in series, with one or more cells in parallel. This combination gives both the voltage and power necessary for many battery powered applications. While the series/parallel combination of Li-ion cells is common, the configuration is not as efficient as it could be, because any capacity mismatch between series-connected cells reduces the overall pack capacity. This mismatch is greater as the number of series cells and the load current increase. Cell balancing techniques increase the capacity, and the operating time, of Li-ion battery packs.

Definition of Cell Balancing

Cell balancing is defined as the application of differential currents to individual cells (or combinations of cells) in a series string. Without cell balancing, cells in a series string receive nominally identical currents. A battery pack requires additional components and circuitry to achieve cell balancing. For the ISL94208 devices, balancing resistors are the only external components required.

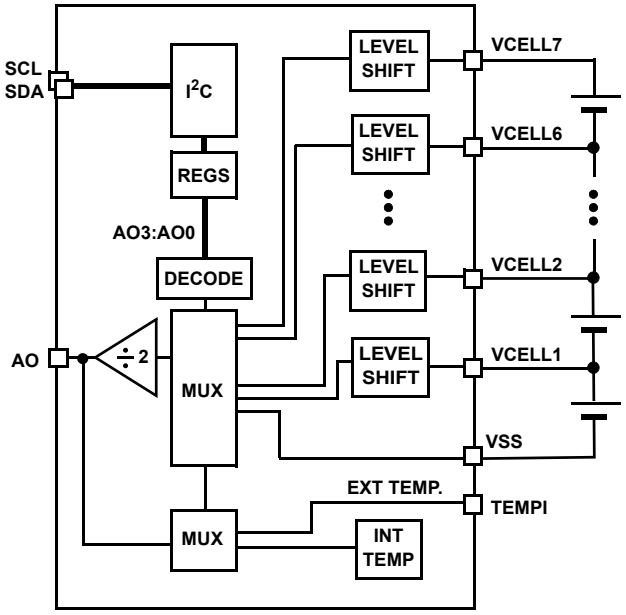


FIGURE 20. ANALOG OUTPUT MONITORING DIAGRAM

Cell Balance Operation

Cell balancing is accomplished through a microcontroller algorithm. This algorithm compares the cell voltages (a representation of the pack capacity) and turns on balancing for the cells that have the higher voltages. There are many parameters that should be considered when writing this algorithm. An example cell balancing algorithm is available in the ISL94208EVAL1Z evaluation kit.

The microcontroller turns on a specific cell balancing switch by setting a bit in the Cell Balance Register. Each bit in the register corresponds to one cell's balancing control. When the bit is set, an internal cell balancing FET turns on. This connects an external resistor across the specified cell. The maximum current that can be drawn from (or bypassed around) the cell is 200mA. This current is set by selecting the value of the external resistor. Figure 21 shows an example with a 200mA (maximum) balancing current.

With lower balancing current, more balancing FETs can be turned on at once, without exceeding the device power dissipation limits or generating excessive balancing current that will heat the external resistor.

External VMON/CFET Protection Mechanisms

When there is a single charge/discharge path, a blocking diode is recommended in the VMON to Pack- (discharge) path in ISL94208 solution. See D1 in Figure 22. This diode is to protect against a negative voltage on the VMON pin that can occur when the FETs are off and the charger connects to the pack. This diode is not needed when there is a separate charge and discharge path, because the voltages on Pack- (discharge) are always positive.

When the pack is designed with a single set of charge/discharge FETs, the ISL94208 CFET pin should be protected in the event of an overcurrent or short-circuit shutdown. When this happens, the FET opens suddenly. The flyback voltage from the motor windings could exceed the maximum input voltage on the CFET pin. Therefore, it is recommended that an additional external series diode be placed between the CFET pin of the ISL94208 and the gate of the Charge FET. See Diode D_3 in Figure 22. This reduces the CFET gate voltage, but not significantly.

Finally, to protect the Charge FET itself in the event of a large negative voltage on the Pack- pin, zener diode D_4 is added. A large negative voltage can occur when the Pack- (discharge) pin goes significantly negative, while the CFET pin is being internally clamped. The zener voltage of D_4 should be less than the V_{GS}(max) specification of the FET.

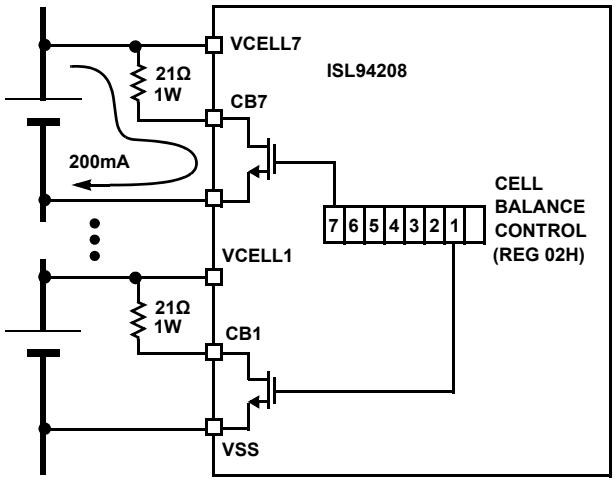


FIGURE 21. CELL BALANCING CONTROL EXAMPLE WITH 200mA BALANCING CURRENT

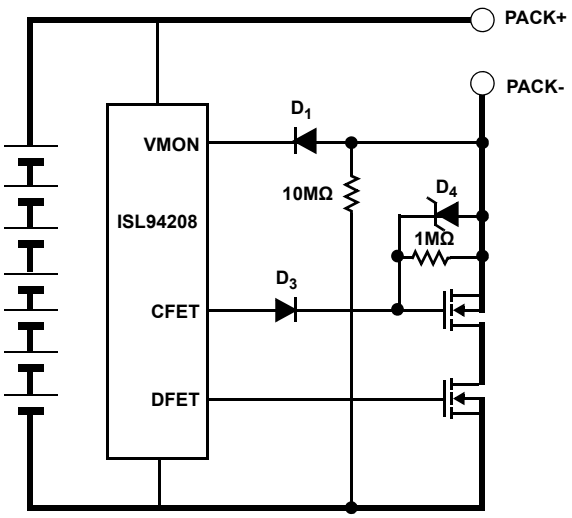


FIGURE 22. USE OF DIODES FOR PROTECTING THE CFET AND VMON PINS

User Flags

The ISL94208 contains four flags in the register area that the microcontroller can use for general purpose indicators. These bits are designated UFLG3, UFLG2, UFLG1, and UFLG0. The microcontroller can set or reset these bits by writing into the appropriate register.

The user flag bits are battery backed up (by the VBACK pin voltage), so the contents remain even after exiting Sleep mode. However, if the microcontroller sets the POR bit to force a power on reset, all of the user flags are also reset. In addition, if the voltage on VBACK ever drops below the POR voltage, the contents of the user flags (as well as all other register values) would be lost.

I^2C Interface

Interface Conventions

The device provides an I^2C communications interface. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the Master and the device being controlled is called the Slave. The Master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the ISL94208 devices operate as slaves in all applications.

When sending or receiving data, the convention is that the Most Significant Bit (MSB) is sent first. Therefore, the first address bit sent is bit 7.

Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes while SCL HIGH are reserved for indicating START and STOP conditions. See Figure 23.

Start Condition

All commands are preceded by the START condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met. See Figure 24.

Stop Condition

All communications must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a Read sequence. A STOP condition is only issued after the transmitting device has released the bus. See Figure 24.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either Master or Slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge that it received the eight bits of data. See Figure 25.

The device responds with an Acknowledge after recognition of a START condition and the correct Slave byte. If a Write operation is selected, the device responds with an Acknowledge after the receipt of each subsequent eight bits. The device acknowledges all incoming data and Address bytes, except for the Slave byte when the contents do not match the device's address.

In the Read mode, the device transmits eight bits of data, releases the SDA line, then monitors the line for an Acknowledge. If an acknowledge is detected and no STOP condition is generated by the Master, the device continues transmitting data. The device terminates further data transmissions if an acknowledge is not detected. The Master must then issue a STOP condition to return the device to Standby mode and place the device into a known state.

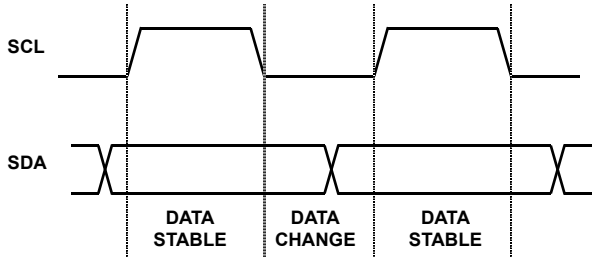


FIGURE 23. VALID DATA CHANGES ON I^2C BUS

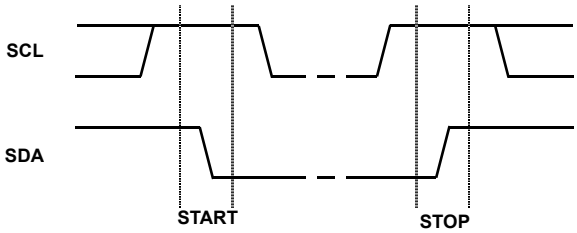


FIGURE 24. I^2C START AND STOP BITS

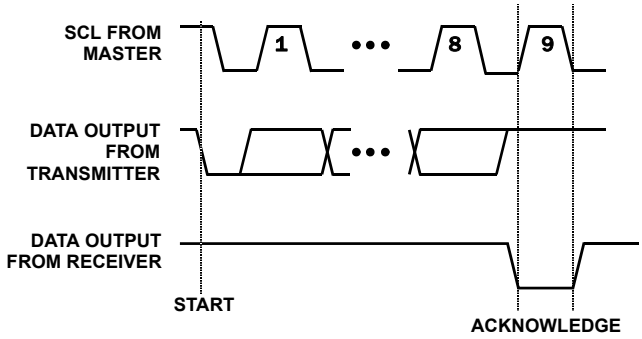


FIGURE 25. ACKNOWLEDGE RESPONSE FROM RECEIVER

Write Operations

For a Write operation, the device requires a Slave byte and a Register Address byte. The Slave byte specifies the particular device on the I^2C bus that the Master is writing to. The Register Address specifies one of the registers in that device. After receipt of each byte, the device responds with an Acknowledge, and awaits the next eight bits from the Master. After the Acknowledge, following the transfer of data, the Master terminates the transfer by generating a STOP condition (see Figure 26).

When receiving data from the Master, the value in the Data byte is transferred into the register specified by the Register address byte on the falling edge of the clock following the eighth data bit.

After receiving the Acknowledge after the Data byte, the device automatically increments the address. So, before sending the STOP bit, the Master may send additional data to the device without re-sending the Slave and Register Address bytes. After writing to address 0AH, the address "wraps around" to address 0. Do not continue to write to addresses higher than address 08H, because these addresses access registers that are reserved. Writing to these locations can result in unexpected device operation.

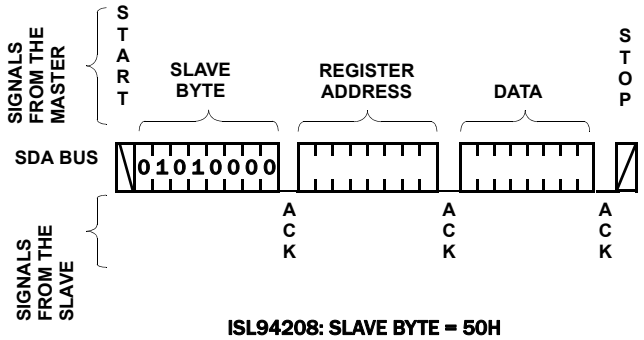
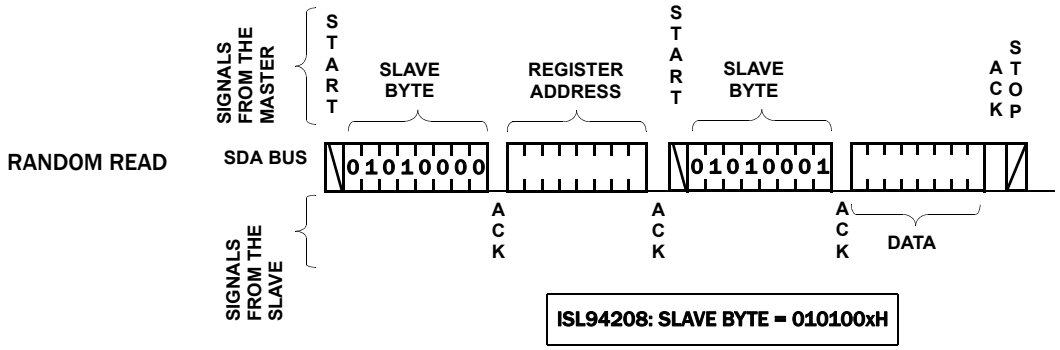


FIGURE 26. WRITE SEQUENCE

Read Sequence



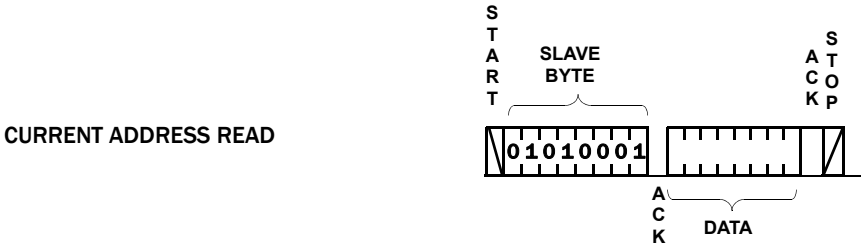


FIGURE 27. READ SEQUENCE

Register Protection

The Discharge Set, Charge Set, and Feature Set configuration registers are write protected on initial power up. To write to these registers it is necessary to set a bit to enable each one. These write enable bits are in the Write Enable register (Address 08H).

1. Write the FSETEN bit (Addr 8:bit 7) to '1' to enable changes to the data in the Feature Set register (Address 7).
2. Write the CHSETEN bit (Addr 8:bit 6) to '1' to enable changes to the data in the Feature Set register (Address 6).
3. Write the DISSETEN bit (Addr 8:bit 5) to '1' to enable changes to the data in the Feature Set register (Address 5).

The microcontroller can reset these bits back to zero to prevent inadvertent writes that change the operation of the pack.

Operation State Machine

Figure 28 shows a device state machine, which illustrates how the ISL94208 responds to various conditions.

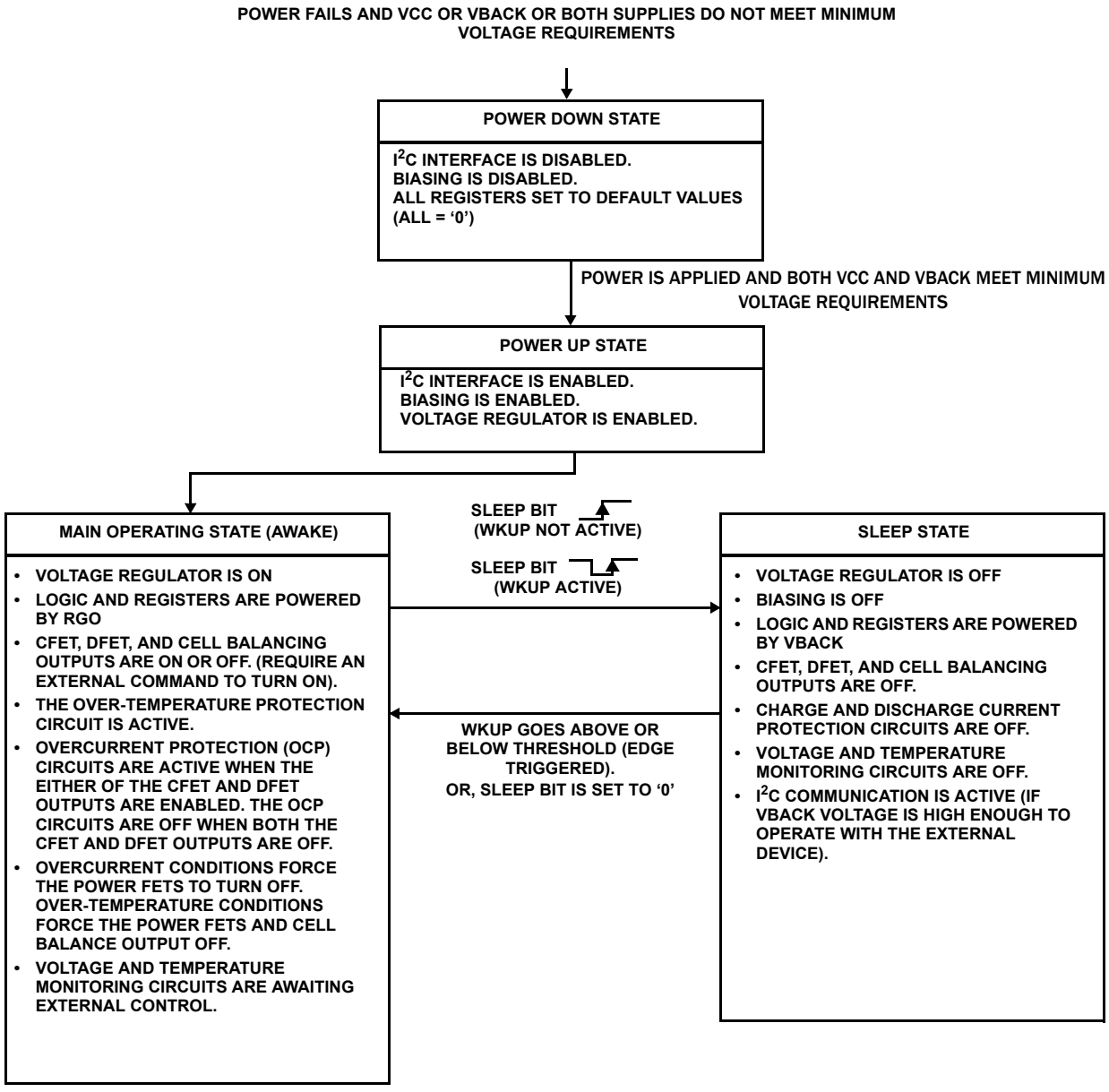


FIGURE 28. DEVICE OPERATION STATE MACHINE

Application Circuits

The following application circuits are ideas to consider when developing a battery pack implementation. There are many more ways that the pack can be designed.

Integrated Charge/Discharge Path

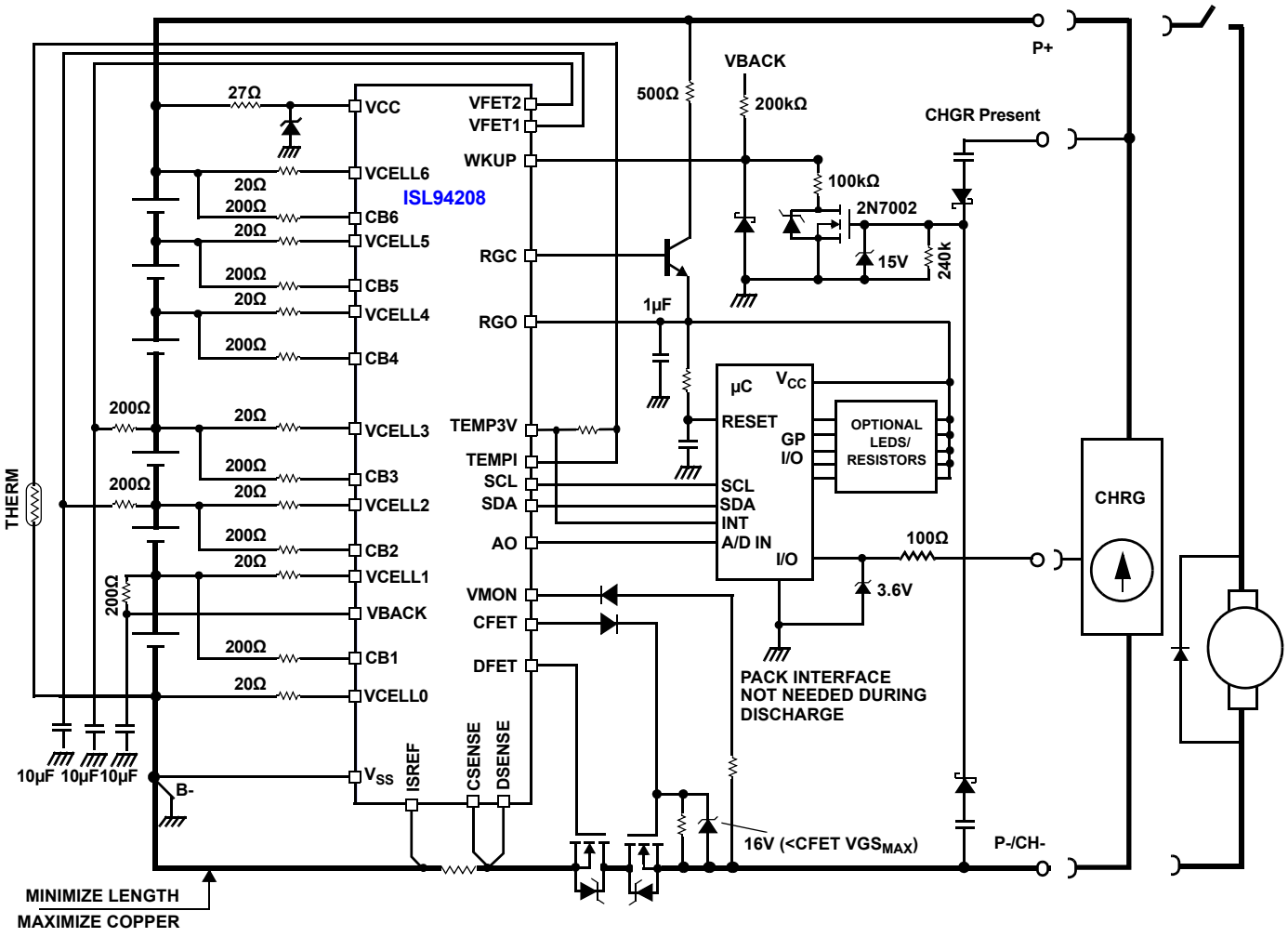


FIGURE 29. 6-CELL APPLICATION CIRCUIT INTEGRATED CHARGE/DISCHARGE PATH

Separate Charge/Discharge Path

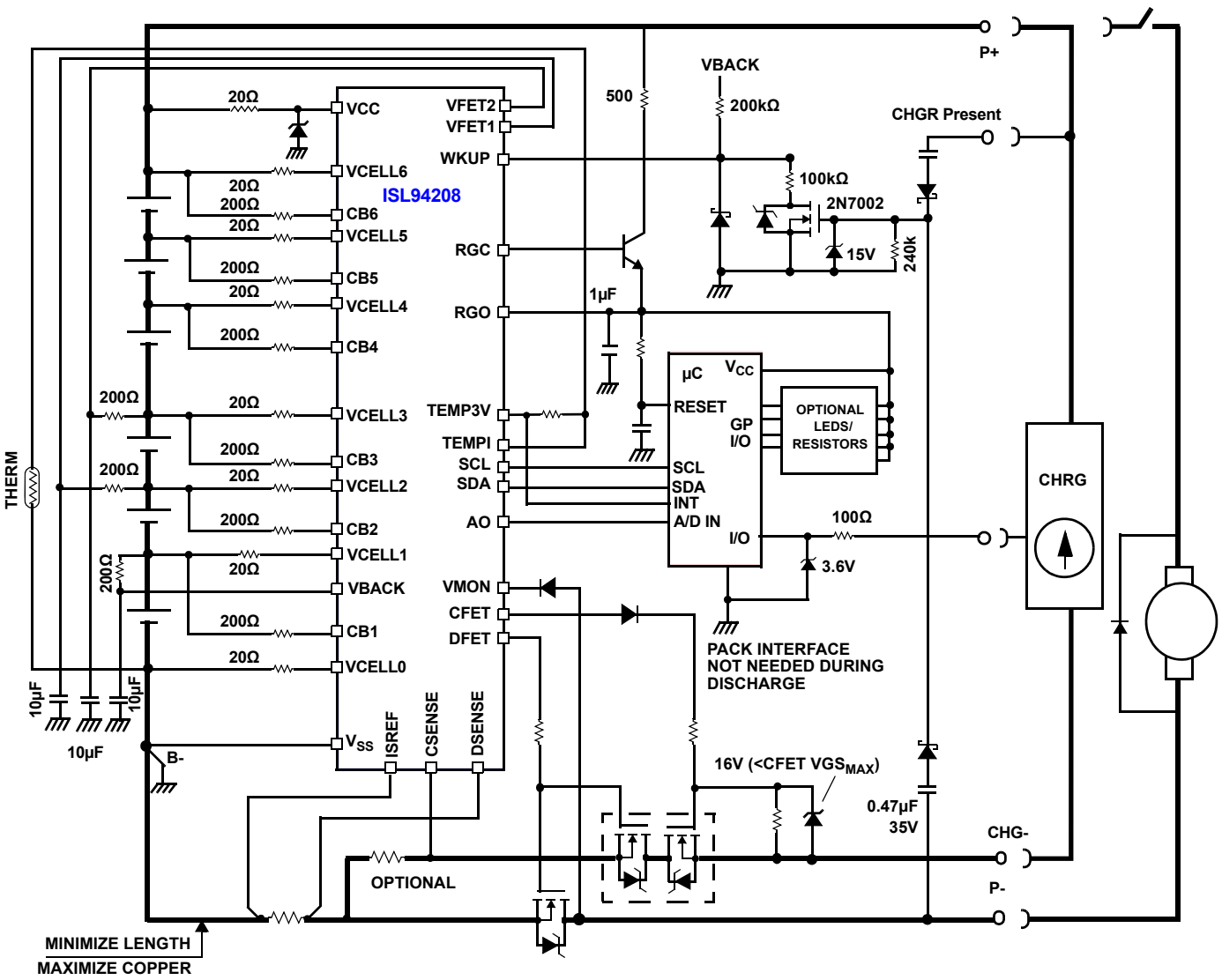


FIGURE 30. 6-CELL APPLICATION CIRCUIT SEPARATE CHARGE/DISCHARGE PATH

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. This is especially true for the CSENSE, DSENSE, and VCELL0-VCELL6 inputs. Trace inductance and capacitance can easily affect circuit performance.
- Match channel-channel analog I/O trace lengths and layout symmetry. This is especially true for the DSENSE, CSENSE, and ISREF lines, because their inputs are normally very low voltage.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes. That is, no split planes or PCB gaps under these lines. Avoid vias in the signal I/O lines. Placing signal lines on internal layers with ground planes on top and bottom of the board provides best immunity to electromagnetic interference.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.

QFN Package

The QFN package requires additional PCB layout rules or the Thermal Pad. The thermal pad is electrically connected to VSS supply through the high resistance IC substrate. The thermal pad provides heat sinking for the IC. If the design uses the RGO pin to supply power to external components or if the device is balancing significant current through the internal balance FETs, then the IC can experience significant internal power dissipation. To deal with this, careful layout of the thermal pad and the use of thermal vias to direct the heat away from the IC is an important consideration. Besides heat dissipation, the thermal pad also provides noise reduction by providing a ground plane under the IC.

Alternate VFET Power Supply

The circuit in Figure 31 shows an alternate connection for powering the Charge and Discharge FETs. If the designer is concerned that the cells become unbalanced by supplying the FET reference from only one or two cells, then a regulator can be used that is powered by the full stack. In this case, the VFET 1 pin needs a supply that is less than VFET2, but not zero. In the circuit below, a 4.3V zener provides the desired reference.

This circuit provides another benefit. In the normal connection, as the cells discharge, the voltages on VFET2 and VFET3 also drop. When the difference between VFET2 nd VFET1 goes below about 2.8V, the FET driver has a difficult time providing the current to control the FETs. This limits the cell voltage to 2.8V. However, by using the external regulator, the pack voltage can drop to 8.6V (or a little below) and still provide adequate FET drive. For a 6-cell pack, the minimum cell voltage is 1.4V per cell. For a 4-cell pack, it is 2.15V per cell.

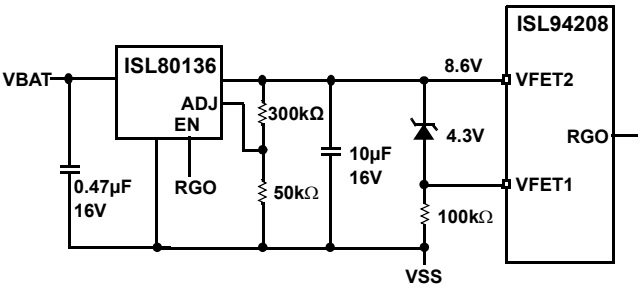


FIGURE 31. ISL94208 EXAMPLE ALTERNATIVE VFET POWER SUPPLY

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 1, 2017	FN8306.2	Updated Note 1 on page 3. Added Table 1 on page 3. Page 6: Added ESD Ratings and Latch-up ratings to “Absolute Maximum Ratings”.
Jun 11, 2013	FN8306.1	Figure 1: Updated application diagram. Page 7: Changed Recommended Operating Conditions for WKUP voltage. Page 8: Reduced Max Limit for VFET1 and VFET2 current. Page 8: Added several operating conditions for VBACK current Specifications adjusted Max Limit to comply with the new conditions. Page 8: Reduced the Limits for VCELL Input Current (Non-Monitoring). Page 21: On the description of the WKPOL bit, added the comment, “When WKPOL=0, limit the maximum voltage on the WKUP pin to no more than the voltage on VBACK.” Page 23: Changed the circuit in Figure 2 on the use of input filters and changed the related text. Page 23: Changed the circuits in Figure 3 regarding the recommended connection of fewer than 6 cells. Page 24: Added text describing the WKPOL=0 and WKPOL=1 operation and changed the example Wake up circuit in Figure 6. Page 25: Changed the comments in Figure 7 to clarify operation of external microcontroller control of wake up. Page 25 and 26: Added comments to Figure 8 and Figure 9. Pages 34 and 35: Updated the example applications circuits in Figure 20 and 21.
Nov 26, 2012	FN8306.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

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Package Outline Drawing

For the most recent package outline drawing, see L32.5x5B.

L32.5x5B

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

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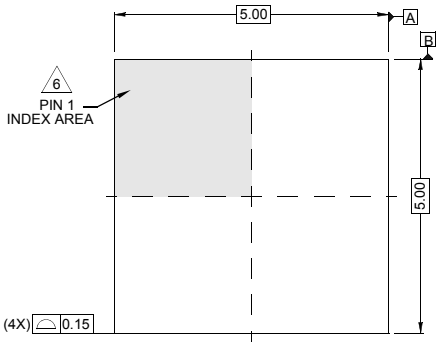
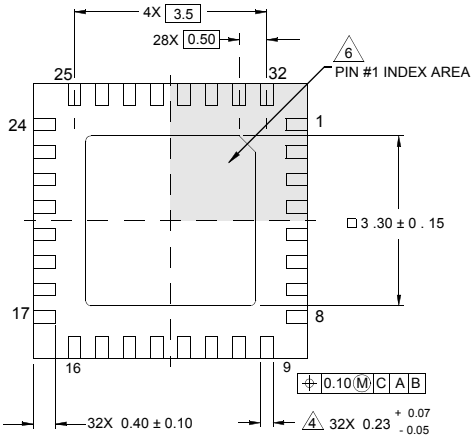
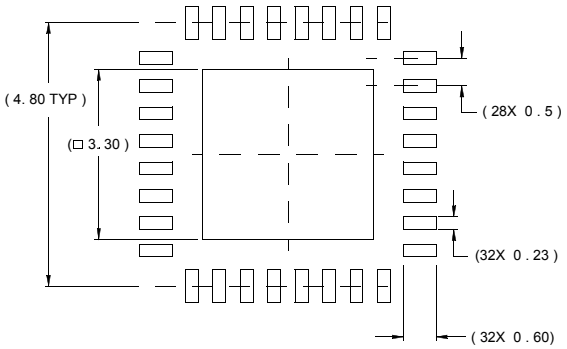


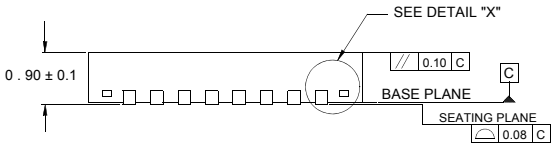
TOP VIEW



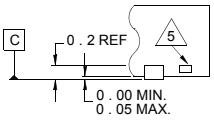
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.