ISL8843

Industry Standard Single-Ended Current Mode PWM Controller

FN9238
Rev 2.00
September 14, 2015

The ISL8843 is an industry standard drop-in replacement for the popular 28C43 and 18C43 PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Its fast signal propagation and output switching characteristics make this an ideal product for existing and new designs.

Features include 30V operation, low operating current, 90µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

PART NUMBER	RISING UVLO	MAX. DUTY CYCLE
ISL8843	8.4V	100%

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8843ABZ (See Note)	8843 ABZ	-40 to 105	8 Ld SOIC (Pb-free)	M8.15
ISL8843AUZ (See Note) **(No longer available, recommended replacement: ISL8843AAUZ)**	8843Z	-40 to 105	8 Ld MSOP (Pb-free)	M8.118
ISL8843MBZ (See Note)	8843 MBZ	-55 to 125	8 Ld SOIC (Pb-free)	M8.15
ISL8843MUZ (See Note) **(No longer available, recommended replacement: ISL8843AMUZ)**	843MZ	-55 to 125	8 Ld MSOP (Pb-free)	M8.118

Add -T to part number for Tape and Reel packaging.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

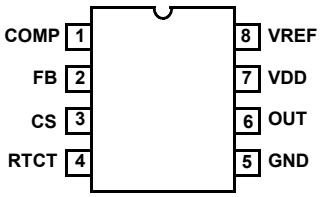
- 1A MOSFET gate driver
- 90µA start-up current, 125µA maximum
- 35ns propagation delay current sense to output
- Fast transient response with peak current mode control
- 30V operation
- Adjustable switching frequency to 2MHz
- 20ns rise and fall times with 1nF output load
- Trimmed timing capacitor discharge current for accurate deadtime/maximum duty cycle control
- 1.5MHz bandwidth error amplifier
- Tight tolerance voltage reference over line, load, and temperature
- ±3% current limit threshold
- Pb-free plus anneal available and ELV, WEEE, RoHS Compliant

Applications

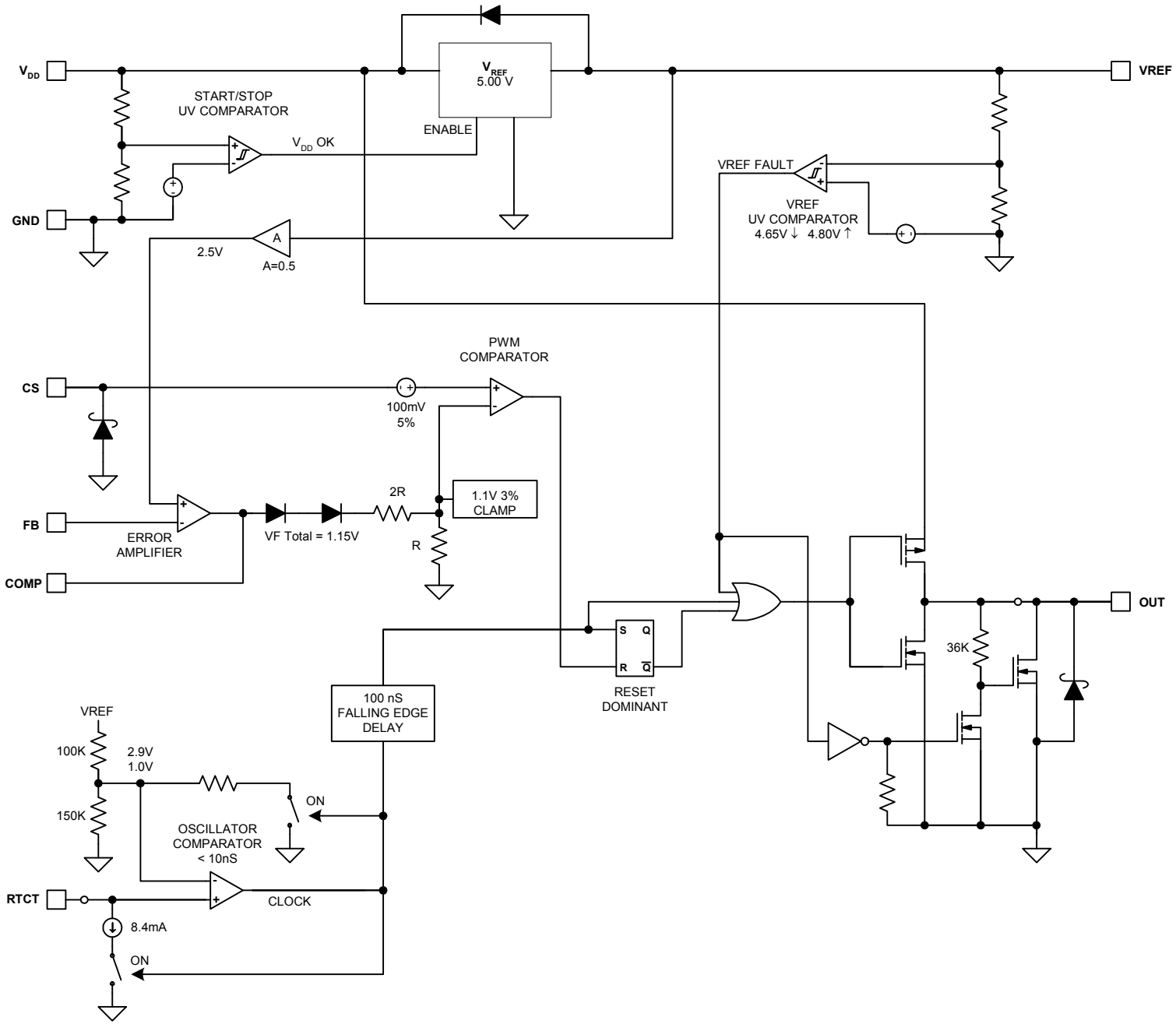
- Telecom and datacom power
- Wireless base station power
- File server power
- Industrial power systems
- PC power supplies
- Isolated buck and flyback regulators
- Boost regulators

Pinout

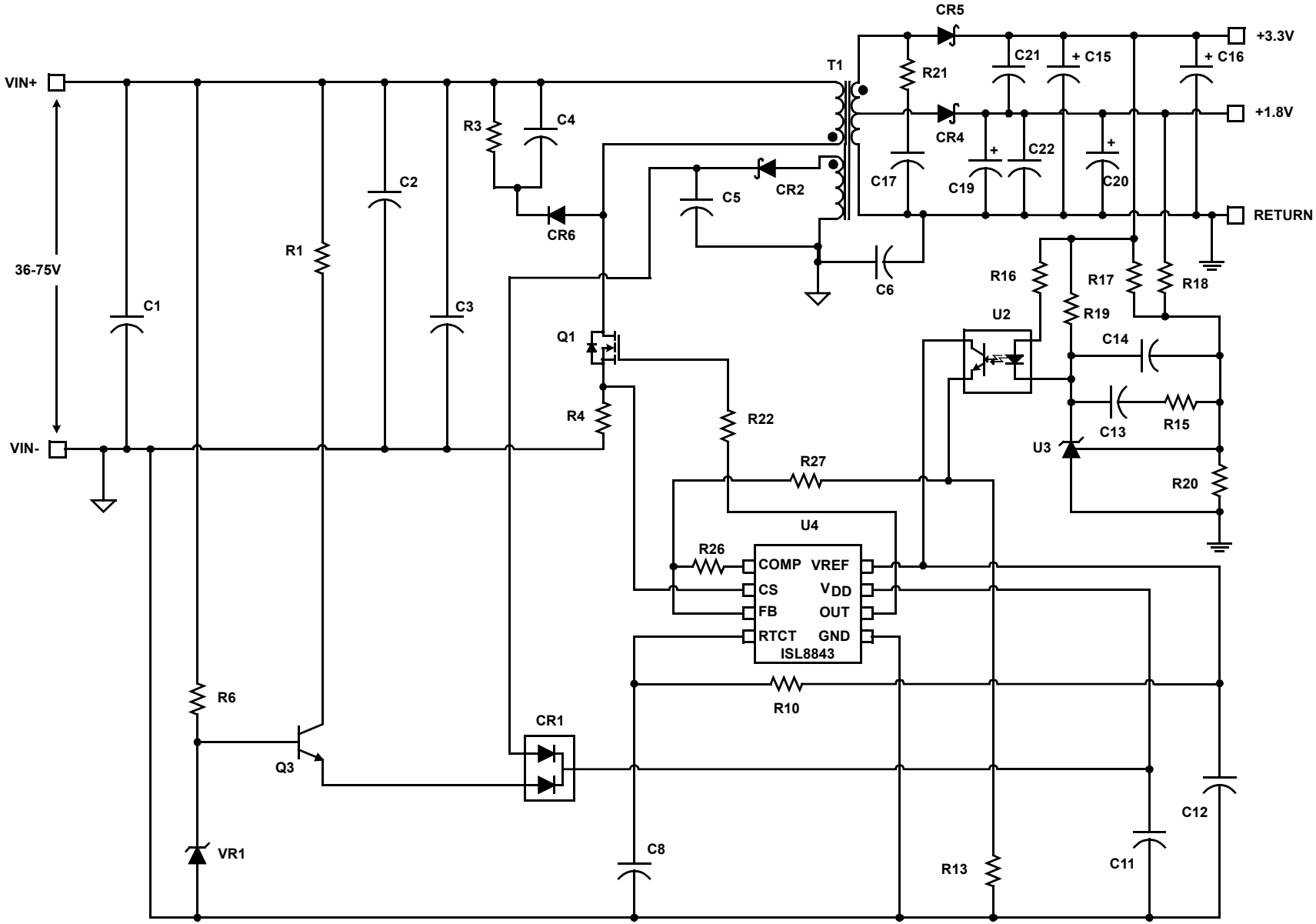
ISL8843
(8 LD SOIC, MSOP)
TOP VIEW



Functional Block Diagram



Typical Application - 48V Input Dual Output Flyback



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +30.0V
OUT . . . . . GND - 0.3V to V_{DD} + 0.3V
Signal Pins . . . . . GND - 0.3V to 6.0V
Peak GATE Current 1A
ESD Classification
Human Body Model (Per JESD22-A114C.01) 2000V
Machine Model (Per EIA/JESD22-A115-A) 200V
Charged Device Model (Per JESD22-C191-A) 1000V

Operating Conditions

Temperature Range
ISL8843AxZ . . . . . -40°C to 105°C
ISL8843MxZ . . . . . -55°C to 125°C
Supply Voltage Range (Typical)
ISL8843 . . . . . 9V - 30V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	100
MSOP Package	130

Maximum Junction Temperature . . . . . -55°C to 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC, MSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are with respect to GND.

Electrical Specifications

ISL8843A - Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. V_{DD} = 15V, RT = 10kΩ, CT = 3.3nF, T_A = -40 to 105°C (Note 3) Typical values are at T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold		8.0	8.4	9.0	V
STOP Threshold		7.3	7.6	8.0	V
Hysteresis		-	0.8	-	V
Startup Current, I_{DD}	V_{DD} < START Threshold	-	90	125	µA
Operating Current, I_{DD}	(Note 4)	-	2.9	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.75	5.5	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	4.925	5.000	5.050	V
Long Term Stability	T_A = 125°C, 1000 hours (Note 5)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1.0	µA
CS Offset Voltage	V_{CS} = 0V (Note 5)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 5)	0.80	1.15	1.30	V
Input Signal, Maximum		0.97	1.00	1.03	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V	2.5	3.0	3.5	V/V
CS to OUT Delay		-	35	55	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 5)	60	90	-	dB
Unity Gain Bandwidth	(Note 5)	1.0	1.5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.475	2.500	2.530	V

Electrical Specifications **ISL8843A -** Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. V_{DD} = 15V, RT = 10kΩ, CT = 3.3nF, T_A = -40 to 105°C (Note 3) Typical values are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FB Input Bias Current	V_{FB} = 0V	-1.0	-0.2	1.0	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	1.0	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	-0.4	-	-	mA
COMP VOH	V_{FB} = 2.3V	4.80	-	VREF	V
COMP VOL	V_{FB} = 2.7V	0.4	-	1.0	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 5)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_A = 25°C	48	51	53	kHz
Frequency Variation with V_{DD}	T_A= 25°C, (F_{30V} - F_{9V})/F_{30V}	-	0.2	1.0	%
Temperature Stability	(Note 5)	-	-	5	%
Amplitude, Peak to Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.5	7.8	8.5	mA
OUTPUT					
Gate VOH	V_{DD} - OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate VOL	OUT - GND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 5)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 5)	-	20	40	ns
Fall Time	C_{OUT} = 1nF (Note 5)	-	20	40	ns
GATE VOL UVLO Clamp Voltage	VDD = 5V, I_{LOAD} = 1mA	-	-	1.2	V
PWM					
Maximum Duty Cycle	COMP = VREF	93.5	95	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

NOTES:

3. Specifications at -40°C and 105°C are guaranteed by 25°C test with margin limits.
4. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
5. Guaranteed by design, not 100% tested in production.

Electrical Specifications **ISL8843M -** Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. V_{DD} = 15V, RT = 10kΩ, CT = 3.3nF, T_A = -55 to 125°C (Note 6), Typical values are at T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold		8.0	8.4	9.0	V
STOP Threshold		7.3	7.6	8.0	V
Hysteresis		-	0.8	-	V
Startup Current, I_{DD}	V_{DD} < START Threshold	-	90	125	µA
Operating Current, I_{DD}	(Note 7)	-	2.9	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.75	5.5	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	4.900	5.000	5.050	V

Electrical Specifications **ISL8843M** - Recommended operating conditions unless otherwise noted. Refer to Block Diagram and Typical Application schematic. V_{DD} = 15V, RT = 10kΩ, CT = 3.3nF, T_A = -55 to 125°C (Note 6), Typical values are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Long Term Stability	T_A = 125°C, 1000 hours (Note 8)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	-1.0	-	1.0	µA
CS Offset Voltage	V_{CS} = 0V (Note 8)	95	100	105	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 8)	0.80	1.15	1.30	V
Input Signal, Maximum		0.97	1.00	1.03	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V	2.5	3.0	3.5	V/V
CS to OUT Delay		-	35	60	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 8)	60	90	-	dB
Unity Gain Bandwidth	(Note 8)	1.0	1.5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	2.460	2.500	2.535	V
FB Input Bias Current	V_{FB} = 0V	-1.0	-0.2	1.0	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	1.0	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	-0.4	-	-	mA
COMP VOH	V_{FB} = 2.3V	4.80	-	VREF	V
COMP VOL	V_{FB} = 2.7V	0.4	-	1.0	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 8)	60	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_A = 25°C	48	51	53	kHz
Frequency Variation with V_{DD}	T_A = 25°C, $(F_{30V} - F_{9V})/F_{30V}$	-	0.2	1.0	%
Temperature Stability	(Note 8)	-	-	5	%
Amplitude, Peak to Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.2	8.0	8.5	mA
OUTPUT					
Gate VOH	V_{DD} - OUT, I_{OUT} = -200mA	-	1.0	2.0	V
Gate VOL	OUT - GND, I_{OUT} = 200mA	-	1.0	2.0	V
Peak Output Current	C_{OUT} = 1nF (Note 8)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 8)	-	20	40	ns
Fall Time	C_{OUT} = 1nF (Note 8)	-	20	40	ns
GATE VOL UVLO Clamp Voltage	VDD = 5V, I_{LOAD} = 1mA	-	-	1.2	V
PWM					
Maximum Duty Cycle	COMP = VREF	93.5	95	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

NOTES:

6. Specifications at -55°C and 125°C are guaranteed by 25°C test with margin limits.
7. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
8. Guaranteed by design, not 100% tested in production.

Typical Performance Curves

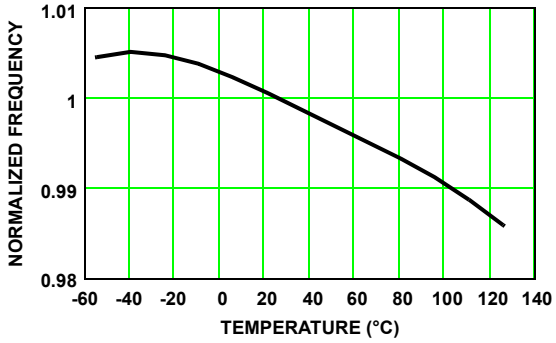


FIGURE 1. FREQUENCY vs TEMPERATURE

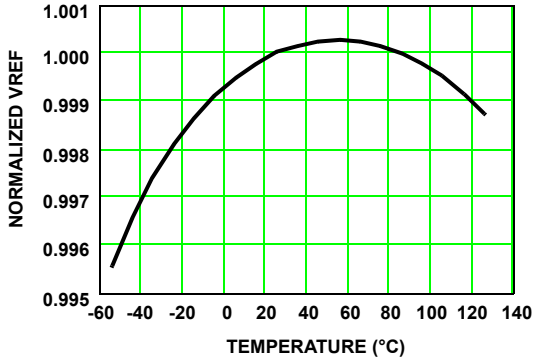


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

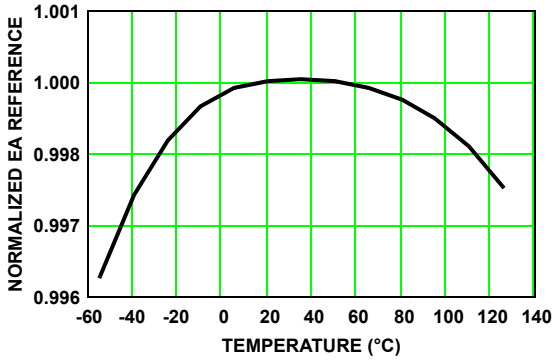


FIGURE 3. EA REFERENCE vs TEMPERATURE

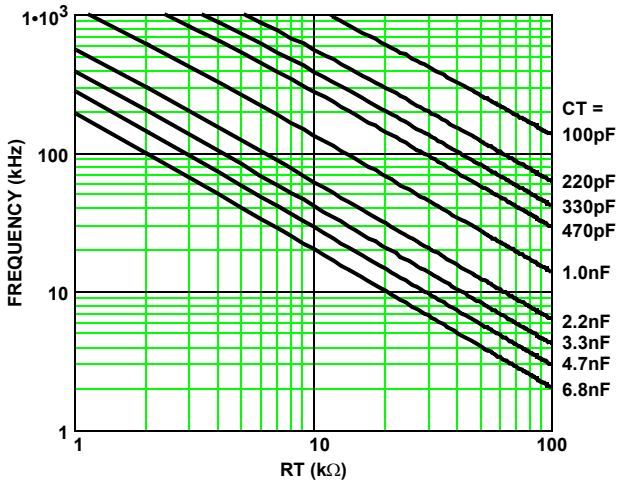


FIGURE 4. RTCT vs FREQUENCY

Pin Descriptions

RTCT - This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, T_C, the discharge time, T_D, the switching frequency, f, and the maximum duty cycle, Dmax, can be approximated from the following equations:

$$T_C \approx 0.533 \bullet RT \bullet CT \quad \text{(EQ. 1)}$$

$$T_D \approx -RT \bullet CT \bullet \ln\left(\frac{0.008 \bullet RT - 3.83}{0.008 \bullet RT - 1.71}\right) \quad \text{(EQ. 2)}$$

$$f = 1/(T_C + T_D) \quad \text{(EQ. 3)}$$

$$D = T_C \bullet f \quad \text{(EQ. 4)}$$

The formulae have increased error at higher frequencies due to propagation delays. Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.

COMP - COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.

FB - The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.

CS - This is the current sense input to the PWM comparator. The range of the input signal is nominally 0 to 1.0V and has an internal offset of 100mV.

GND - GND is the power and small signal reference ground for all functions.

OUT - This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when V_{DD} is below the UVLO threshold.

V_{DD} - V_{DD} is the power connection for the device. The total supply current will depend on the load applied to OUT. Total I_{DD} current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated from:

$$I_{OUT} = Qg \times f \quad \text{(EQ. 5)}$$

To optimize noise immunity, bypass V_{DD} to GND with a ceramic capacitor as close to the V_{DD} and GND pins as possible.

VREF - The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

Functional Description

Features

The ISL8843 current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL8843 has a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

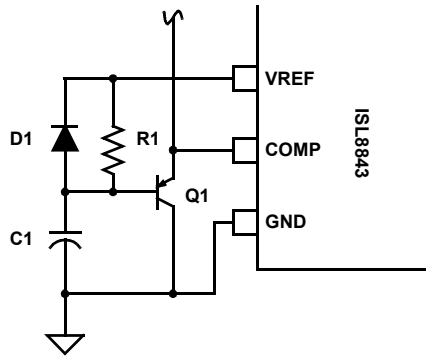


FIGURE 5. SOFT-START

The COMP pin is clamped to the voltage on capacitor C1 plus a base-emitter junction by transistor Q1. C1 is charged from VREF through resistor R1 and the base current of Q1. At power-up C1 is fully discharged, COMP is at ~0.7V, and the duty cycle is zero. As C1 charges, the voltage on COMP increases, and the duty cycle increases in proportion to the voltage on C1. When COMP reaches the steady state operating point, the control loop takes over and soft start is complete. C1 continues to charge up to VREF and no longer affects COMP. During power down, diode D1 quickly discharges C1 so that the soft start circuit is properly initialized prior to the next power on sequence.

Gate Drive

The ISL8843 is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, Fm, without slope compensation, is

$$Fm = \frac{1}{SnTsw} \quad \text{(EQ. 6)}$$

where Sn is the slope of the sawtooth signal and Tsw is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes

$$Fm = \frac{1}{(Sn+Se)Tsw} = \frac{1}{m_c SnTsw} \quad \text{(EQ. 7)}$$

where Se is slope of the external ramp and

$$m_c = 1 + \frac{Se}{Sn} \quad \text{(EQ. 8)}$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching

frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for Q < 1, and under-damped for Q > 1. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D)-0.5)} \quad \text{(EQ. 9)}$$

where D is the percent of on time during a switching cycle. Setting Q = 1 and solving for Se yields

$$S_e = S_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 10)}$$

Since Sn and Se are the on time slopes of the current ramp and the external ramp, respectively, they can be multiplied by Ton to obtain the voltage change that occurs during Ton.

$$V_e = V_n\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad \text{(EQ. 11)}$$

where Vn is the change in the current feedback signal (ΔI) during the on time and Ve is the voltage that must be added by the external ramp.

For a flyback converter, Vn can be solved for in terms of input voltage, current transducer components, and primary inductance, yielding

$$V_e = \frac{D \cdot T_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p}\left(\left(\frac{1}{\pi}+0.5\right)\frac{1}{1-D}-1\right) \quad V \quad \text{(EQ. 12)}$$

where R_{CS} is the current sense resistor, T_{SW} is the switching frequency, L_p is the primary inductance, V_{IN} is the minimum input voltage, and D is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is:

$$V_{CS} = \frac{N_S \cdot R_{CS}}{N_P}\left(I_O + \frac{(1-D)\cdot V_O \cdot T_{sw}}{2L_s}\right) \quad V \quad \text{(EQ. 13)}$$

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance, and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Since the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold.

$$V_e + V_{CS} = 1 \quad \text{(EQ. 14)}$$

Substituting Equations 12 and 13 into Equation 14 and solving for R_{CS} yields

$$R_{CS} = \frac{1}{\frac{D \cdot T_{sw} \cdot V_{IN}}{L_p}\cdot\left(\frac{\frac{1}{\pi}+0.5}{1-D}-1\right)+\frac{N_s}{N_p}\cdot\left(I_O+\frac{(1-D)\cdot V_O \cdot T_{sw}}{2L_s}\right)} \quad \text{(EQ. 15)}$$

Adding slope compensation is accomplished in the ISL8843 using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in Figure 6.

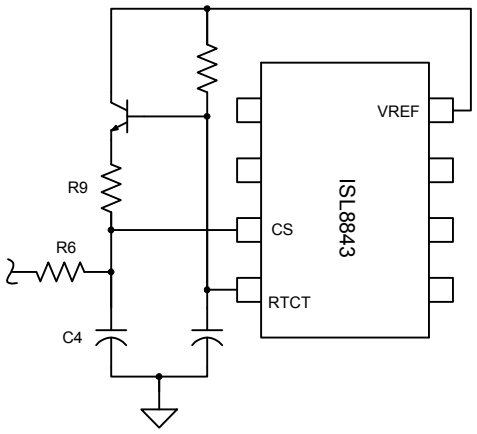


FIGURE 6. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R6 and C4) placed on the CS pin, the value of R9 required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05D \cdot R6}{R6+R9} \quad V \quad \text{(EQ. 16)}$$

The factor of 2.05 in Equation 16 arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R9 yields:

$$R9 = \frac{(2.05D - V_e)\cdot R6}{V_e} \quad \Omega \quad \text{(EQ. 17)}$$

The value of R_{CS} determined in Equation 15 must be rescaled so that the current sense signal presented at the CS pin is that predicted by Equation 13. The divider created by R6 and R9 makes this necessary.

$$R'_{CS} = \frac{R6+R9}{R9}\cdot R_{CS} \quad \text{(EQ. 18)}$$

Example:

V_{IN} = 12V

V_O = 48V

L_s = 800µH

Ns/Np = 10

Lp = 8.0µH

I_O = 200mA

Switching Frequency, Fsw = 200kHz

Duty Cycle, D = 28.6%

R6 = 499Ω

Solve for the current sense resistor, R_{CS}, using Equation 15.

R_{CS} = 295mΩ

Determine the amount of voltage, Ve, that must be added to the current feedback signal using Equation 12.

Ve = 92.4mV

Using Equation 17, solve for the summing resistor, R9, from CT to CS.

R9 = 2.67kΩ

Determine the new value of R_{CS}, R'_{CS}, using Equation 18.

R'_{CS} = 350mΩ

Additional slope compensation may be considered for design margin. The above discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from RTCT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and will reduce the oscillator frequency.

Fault Conditions

A Fault condition occurs if VREF falls below 4.65V. When a Fault is detected OUT is disabled. When VREF exceeds 4.80V, the Fault condition clears, and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

References

[1] Ridley, R., “A New Continuous-Time Model for Current Mode Control”, IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
September 14, 2015	FN9238.2	- Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. - Updated POD M8.15 to latest revision changes are as follow: -Revision 1 to Revision 2 Changes: Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern. -Revision 2 to Revision 3 Changes: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) -Revision 3 to Revision 4 Changes: Changed Note 1 "1982" to "1994"

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

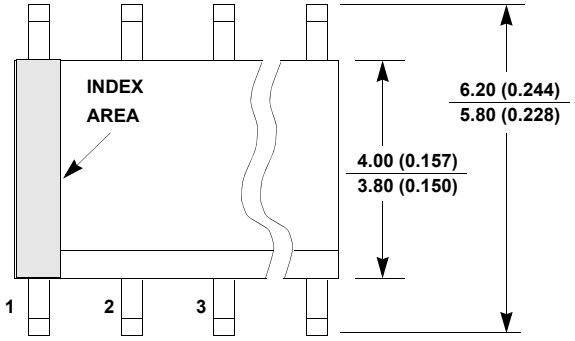
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

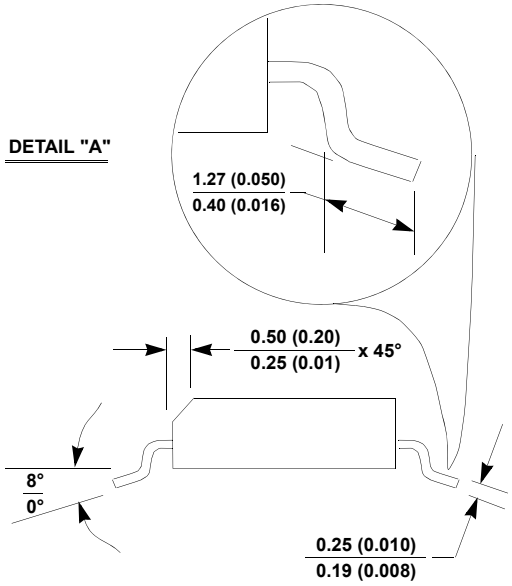
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

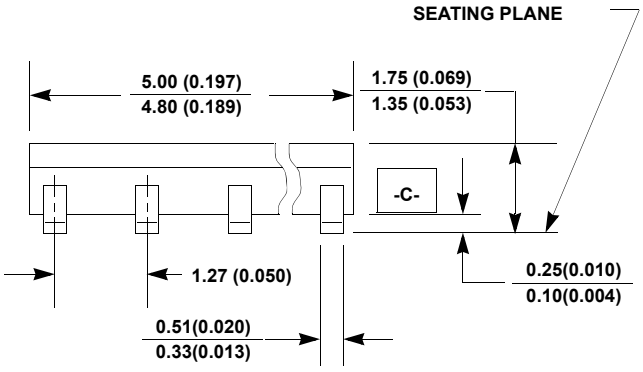
Rev 4, 1/12



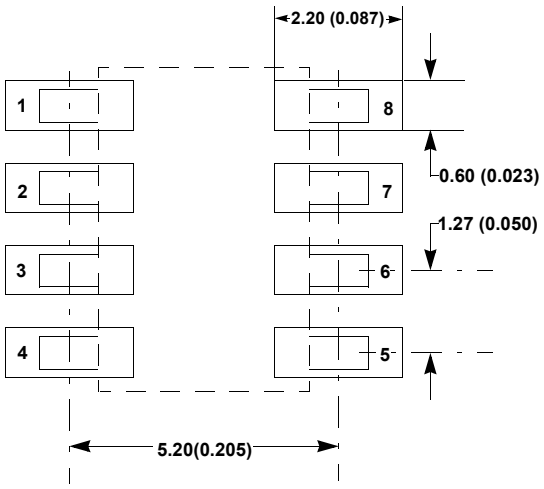
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"

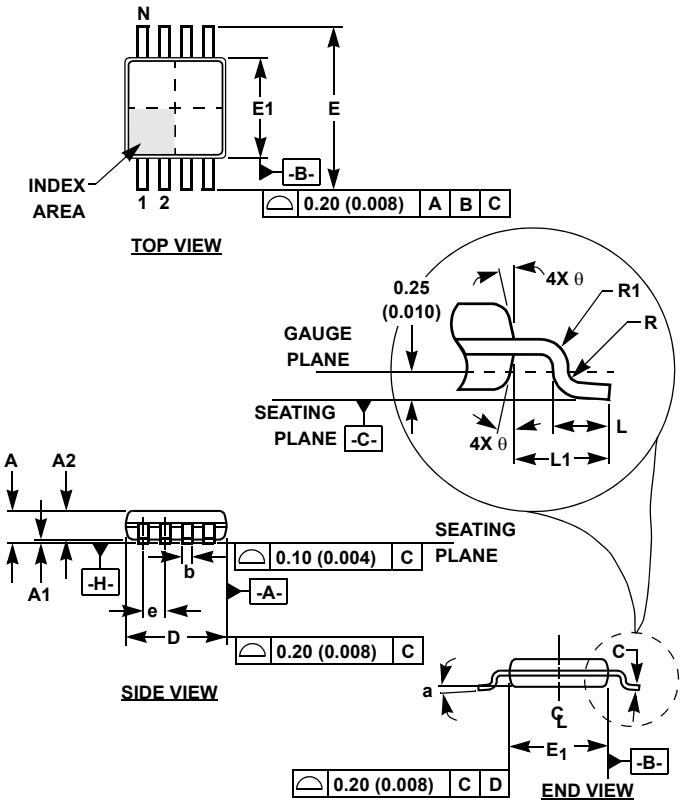


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
0	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.