ISL8484

Ultra Low ON-Resistance, +1.65V to +4.5V, Single Supply, Dual SPDT Analog Switch

FN6128
Rev 5.00
May 12, 2008

The Intersil ISL8484 device is a low ON-resistance, low voltage, bidirectional, dual single-pole/double-throw (SPDT) analog switch designed to operate from a single +1.65V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low r_{ON} (0.29Ω) and fast switching speeds (t_{ON} = 40ns, t_{OFF} = 20ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply.

With a supply voltage of 4.2V and logic high voltage of 2.85V at both logic inputs, the part draws only 12µA max of I+ current.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to “mux-in” additional functionality while reducing ASIC design risk. The ISL8484 is offered in small form factor packages, alleviating board space limitations.

The ISL8484 is a committed dual single-pole/double-throw (SPDT) that consist of two normally open (NO) and two normally closed (NC) switches. This configuration can be used as a dual 2-to-1 multi-plexer. The ISL8484 is pin compatible with the MAX4684 and MAX4685.

TABLE 1. FEATURES AT A GLANCE

	ISL8484
NUMBER OF SWITCHES	2
SW	SPDT or 2-1 MUX
4.3V r_{ON}	0.29Ω
4.3V t_{ON}/t_{OFF}	40ns/20ns
3V r_{ON}	0.33Ω
3V t_{ON}/t_{OFF}	50ns/27ns
1.8V r_{ON}	0.55Ω
1.8V t_{ON}/t_{OFF}	70ns/54ns
Packages	10 Ld 3x3 Thin DFN, 10 Ld MSOP

Features

- Pin Compatible Replacement for the MAX4684 and MAX4685
- ON-Resistance (r_{ON})
  - V+ = +4.3V 0.29Ω
  - V+ = +3.0V 0.33Ω
  - V+ = +1.8V 0.55Ω
- r_{ON} Matching Between Channels 0.06Ω
- r_{ON} Flatness Across Signal Range 0.03Ω
- Single Supply Operation. . . . . +1.65V to +4.5V
- Low Power Consumption (P_D) . . . . . .<0.45µW
- Fast Switching Action (V+ = +4.3V)
  - t_{ON} 40ns
  - t_{OFF} 20ns
- ESD HBM Rating . . . . . >8kV
- Guaranteed Break-Before-Make
- 1.8V Logic Compatible (+3V supply)
- Low I+ Current when V_{IN}H is not at the V+ Rail
- Available in 10 Ld 3x3 TDFN and 10 Ld MSOP
- Pb-Free Available (RoHS Compliant)

Applications

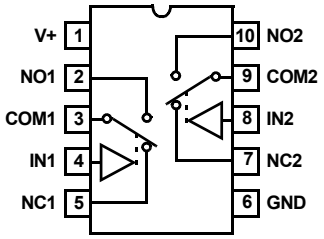
- Battery-powered, Handheld, and Portable Equipment
  - Cellular/mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Pinout (Note 1)

ISL8484
(10 LD TDFN, MSOP)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Input.

Truth Table

LOGIC	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V with a 3V supply.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (+1.65V to +4.5V)
GND	Ground Connection
INx	Digital Control Input
COMx	Analog Switch Common Pin
NOx	Analog Switch Normally Open Pin
NCx	Analog Switch Normally Closed Pin

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8484IR*	484	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL8484IU*	8484	-40 to +85	10 Ld MSOP	M10.118
ISL8484IRZ* (Note)	484Z	-40 to +85	10 Ld 3x3 TDFN (Pb-free)	L10.3x3A
ISL8484IUZ* (Note)	8484Z	-40 to +85	10 Ld MSOP (Pb-free)	M10.118

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.5 to 5.5V
Input Voltages
NO, NC, IN (Note 2). . . . . -0.5 to ((V+) + 0.5V)
Output Voltages
COM (Note 2). . . . . -0.5 to ((V+) + 0.5V)
Continuous Current NO, NC, or COM . . . . . ±300mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating:
Human Body Model . . . . . >8kV
Machine Model. . . . . >500V
Charged Device Model. . . . . >1.4kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 TDFN Package (Notes 3, 4)	52	11
10 Ld MSOP Package (Note 5)	140	N/A

Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
4. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 6), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 11)	TYP	MAX (Notes 7, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Figure 5, Note 9)	25	-	0.30	0.5	Ω
		Full	-	0.35	0.7	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max R_{ON} (Note 9, 10)	25	-	0.06	0.07	Ω
		Full	-	0.08	0.08	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Note 8, 9)	25	-	0.03	0.15	Ω
		Full	-	0.04	0.15	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-100	-	100	nA
		Full	-195	-	195	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-100	-	100	nA
		Full	-195	-	195	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	40	-	ns
		Full	-	50	-	ns
Turn-OFF Time, t_{OFF}	V+ = 3.9V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	20	-	ns
		Full	-	30	-	ns
Break-Before-Make Time Delay, t_D	V+ = 4.5V, V_{NO} or V_{NC} = 3.0V, R_L = 50Ω, C_L = 35pF (Figure 3)	Full	-	8	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	170	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (Figure 4)	25	-	62	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (Figure 6)	25	-	-85	-	dB

Electrical Specifications - 4.3V Supply

Test Conditions: V+ = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 6), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 11)	TYP	MAX (Notes 7, 11)	UNITS
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.005	-	%
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	62	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	176	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.65	-	4.5	V
Positive Supply Current, I+	V+ = +4.5V, V_{IN} = 0V or V+	25	-	-	0.1	µA
		Full	-	-	1	µA
Positive Supply Current, I+	V+ = +4.2V, V_{IN} = 2.85V	25	-	-	12	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		Full	-	-	0.5	V
Input Voltage High, V_{INH}		Full	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 4.5V, V_{IN} = 0V or V+ (Note 9)	Full	-0.5	-	0.5	µA

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 6), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 11)	TYP	MAX (Notes 7, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Figure 5)	25	-	0.35	0.5	Ω
		Full	-	-	0.7	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = Voltage at max R_{ON} (Note 10)	25	-	0.06	0.07	Ω
		Full	-	-	0.08	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Note 8)	25	-	0.03	0.15	Ω
		Full	-	-	0.15	Ω
NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{NO} or V_{NC} = 3V, 0.3V	25	-	0.9	-	nA
		Full	-	30	-	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, or V_{NO} or V_{NC} = 0.3V, 3V, or Floating	25	-	0.8	-	nA
		Full	-	30	-	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	50	-	ns
		Full	-	60	-	ns
Turn-OFF Time, t_{OFF}	V+ = 2.7V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	27	-	ns
		Full	-	35	-	ns
Break-Before-Make Time Delay, t_D	V+ = 3.3V, V_{NO} or V_{NC} = 1.5V, R_L = 50Ω, C_L = 35pF (Figure 3)	Full	-	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	94	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$ (Figure 4)	25	-	62	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 100kHz, V_{COM} = $1V_{RMS}$, (Figure 6)	25	-	-85	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{COM} = $2V_{P-P}$, R_L = 600Ω	25	-	0.005	-	%

Electrical Specifications - 3V Supply

Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 6), Unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 11)	TYP	MAX (Notes 7, 11)	UNITS
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	65	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	181	-	pF
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = +3.6V, V_{IN} = 0V or V+	25	-	0.01	-	µA
		Full	-	0.52	-	µA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.5	V
Input Voltage High, V_{INH}		25	1.4	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 3.3V, V_{IN} = 0V or V+ (Note 9)	Full	-0.5	-	0.5	µA

Electrical Specifications - 1.8V Supply

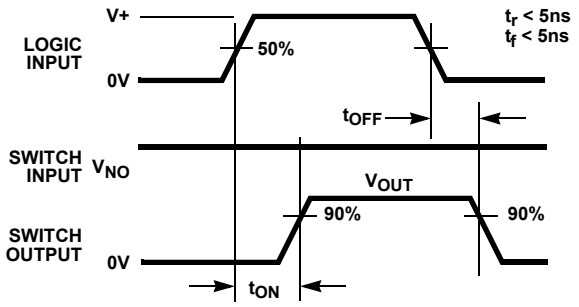
Test Conditions: V+ = +1.65V to +2V, GND = 0V, VINH = 1.0V, VINL = 0.4V (Note 6), Unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 7, 11)	TYP	MAX (Notes 7, 11)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON-Resistance, r_{ON}	V+ = 1.65V, I_{COM} = 100mA, V_{NO} or V_{NC} = 0V to V+ (Figure 5)	25	-	0.7	0.8	Ω
		Full	-	-	0.85	Ω
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	70	-	ns
		Full	-	80	-	ns
Turn-OFF Time, t_{OFF}	V+ = 1.65V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (Figure 1)	25	-	54	-	ns
		Full	-	65	-	ns
Break-Before-Make Time Delay, t_D	V+ = 2.0V, V_{NO} or V_{NC} = 1.0V, R_L = 50Ω, C_L = 35pF (Figure 3)	Full	-	10	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω (Figure 2)	25	-	42	-	pC
NO or NC OFF Capacitance, C_{OFF}	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	70	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{NO} or V_{NC} = V_{COM} = 0V (Figure 7)	25	-	186	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}		25	-	-	0.4	V
Input Voltage High, V_{INH}		25	1.0	-	-	V
Input Current, I_{INH}, I_{INL}	V+ = 2.0V, V_{IN} = 0V or V+ (Note 9)	Full	-0.5	-	0.5	µA

NOTES:

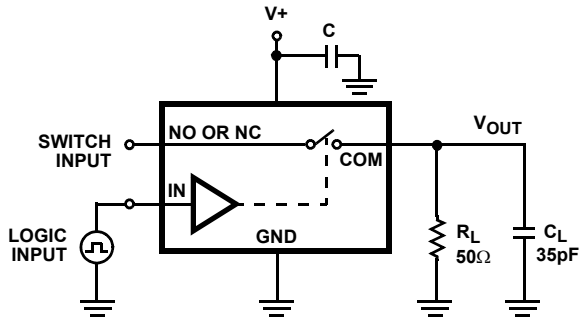
6. V_{IN} = input voltage to perform proper function.
7. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
8. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
9. Limits established by characterization and are not production tested.
10. R_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between NC1 and NC2 or between NO1 and NO2.
11. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS

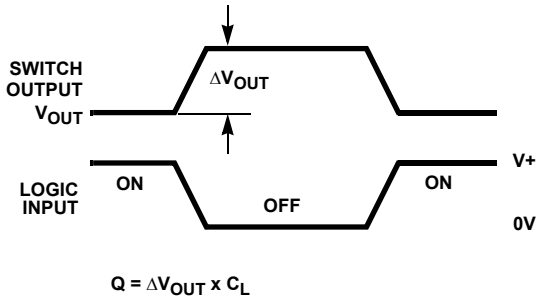


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{r_L}{r_L + r_{(ON)}}$$

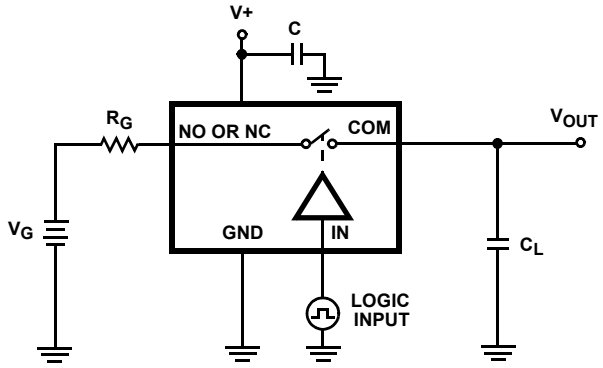
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



$Q = \Delta V_{OUT} \times C_L$

FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches.

FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

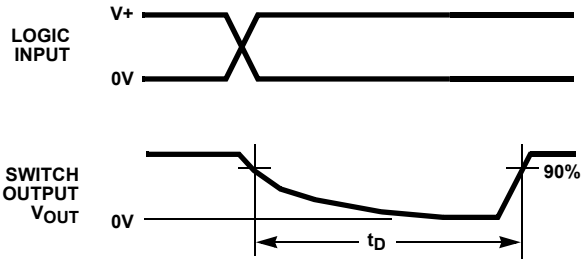
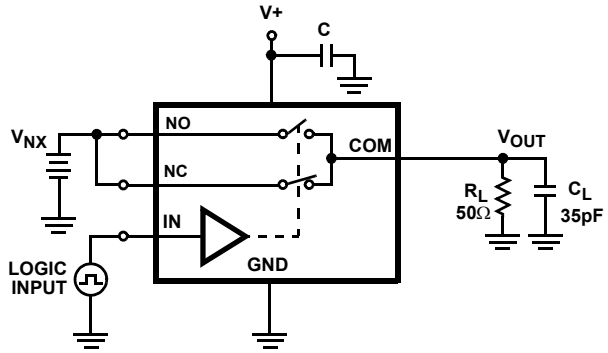


FIGURE 3A. MEASUREMENT POINTS

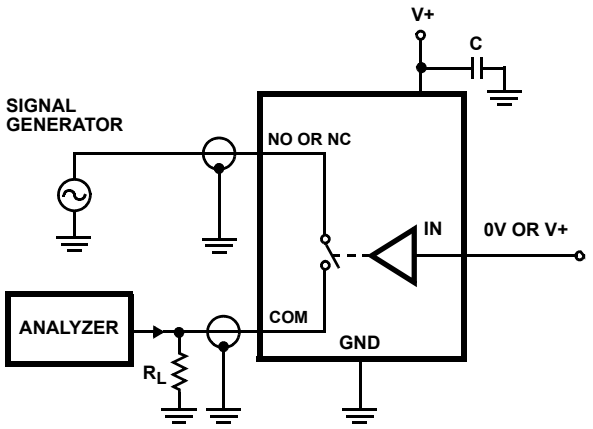


Repeat test for all switches. C_L includes fixture and stray capacitance.

FIGURE 3B. TEST CIRCUIT

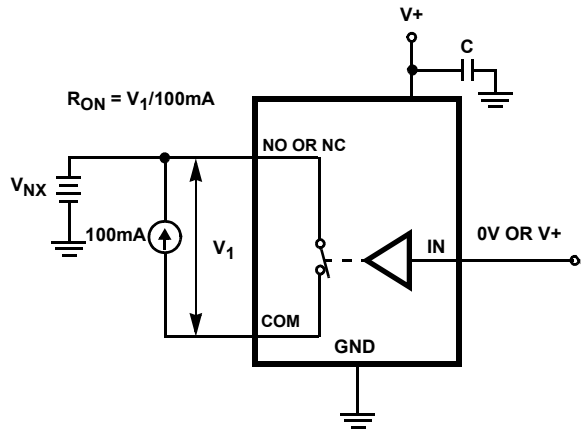
FIGURE 3. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)



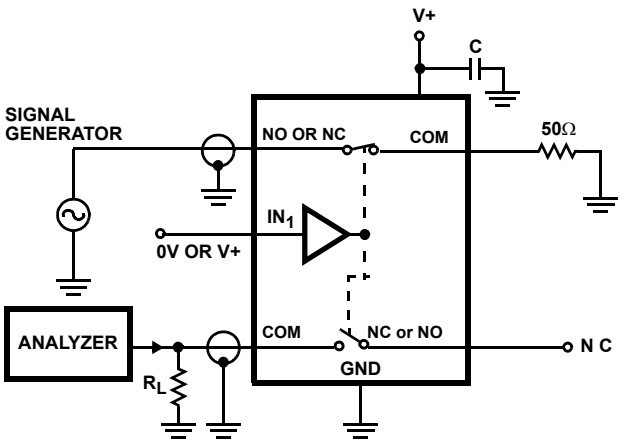
Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 4. OFF-ISOLATION TEST CIRCUIT



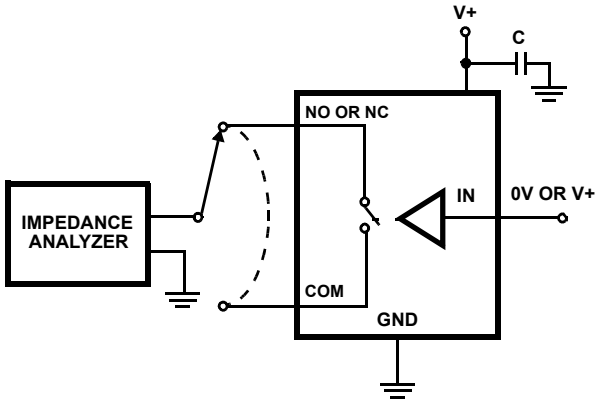
Repeat test for all switches.

FIGURE 5. r_{ON} TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. CROSSTALK TEST CIRCUIT



Repeat test for all switches.

FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL8484 is a bidirectional, dual single pole/double throw (SPDT) analog switch that offers precise switching capability from a single 1.65V to 4.5V supply with low on-resistance (0.29Ω) and high speed operation (t_{ON} = 40ns, t_{OFF} = 20ns). The device is especially well suited for portable battery-powered equipment due to its low operating supply voltage (1.65V), low power consumption (4.5µW max), low leakage currents (195nA max), and the tiny DFN and MSOP packages. The ultra low on-resistance and r_{ON} flatness provide very low insertion loss and distortion to applications that require signal reproduction.

External V+ Series Resistor

For improved ESD and latch-up immunity Intersil recommends adding a 100Ω resistor in series with the V+ power supply pin of the ISL8484 IC (see Figure 8).

During an overvoltage transient event, such as occurs during system level IEC 61000 ESD testing, substrate currents can be generated in the IC that can trigger parasitic SCR structures to turn ON, creating a low impedance path from the V+ power supply to ground. This will result in a significant amount of current flow in the IC which can potentially create a latch-up state or permanently damage the IC. The external V+ resistor limits the current during this over-stress situation and has been found to prevent latch-up or destructive damage for many overvoltage transient events.

Under normal operation the sub-microamp I_{DD} current of the IC produces an insignificant voltage drop across the 100Ω series resistor resulting in no impact to switch operation or performance.

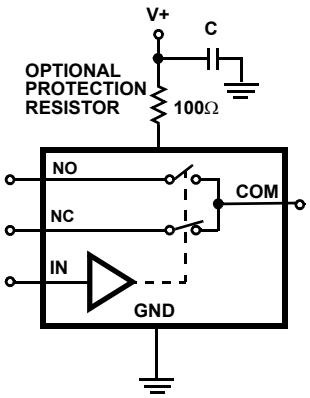


FIGURE 8. V+ SERIES RESISTOR FOR ENHANCED ESD AND LATCH-UP IMMUNITY

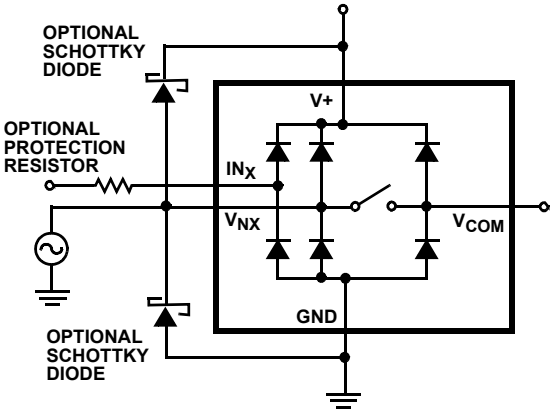


FIGURE 9. OVERVOLTAGE PROTECTION

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 9). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 9). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch. Connecting Schottky diodes to the signal pins as shown in Figure 8 will shunt the fault current to the supply or to ground thereby protecting the switch. These Schottky diodes must be sized to handle the expected fault current.

Power-Supply Considerations

The ISL8484 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL8484 5.5V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the “Electrical Specifications” tables, beginning on page 3, and “Typical Performance Curves”, beginning on page 9, for details.

V+ and GND also power the internal logic and level shiftiers. The level shiftiers convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.7V to 4.5V (see Figure18). At 2.7V the V_{IL} level is about 0.53V. This is still above the 1.8V CMOS guaranteed low output maximum level of 0.5V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

The ISL8484 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply the device draws only 12µA of current
(see Figure17 for VIN = 2.85V).

High-Frequency Performance

In 50Ω systems, the signal response is reasonably flat even past 30MHz with a -3dB bandwidth of 120MHz (see Figure 22). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch’s input to its output. Off Isolation is

the resistance to this feedthrough, while crosstalk indicates the amount of feedthrough from one switch to another. Figure 23 details the high off isolation and crosstalk rejection provided by this part. At 100kHz, off isolation is about 62dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified.

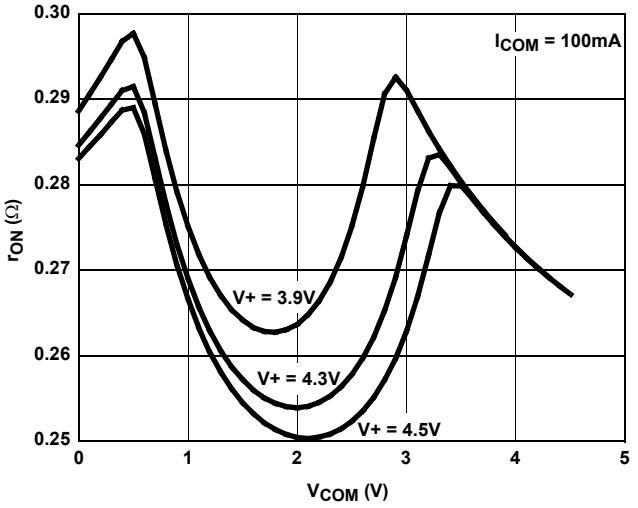


FIGURE 10. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

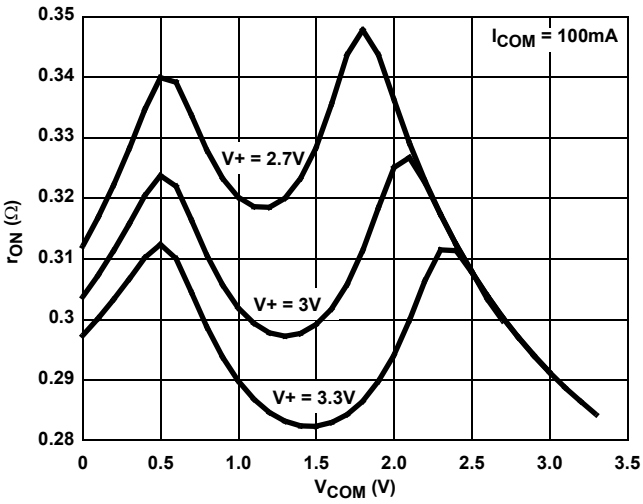


FIGURE 11. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

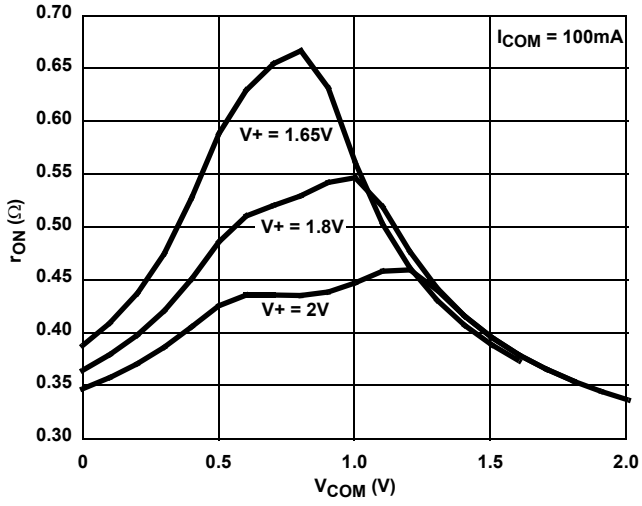


FIGURE 12. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

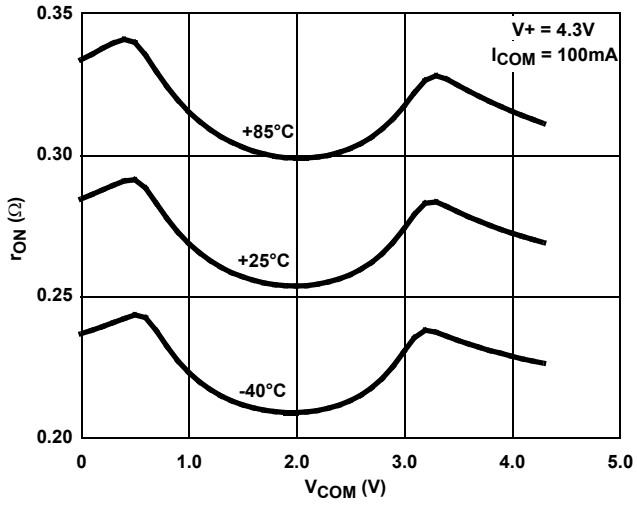


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

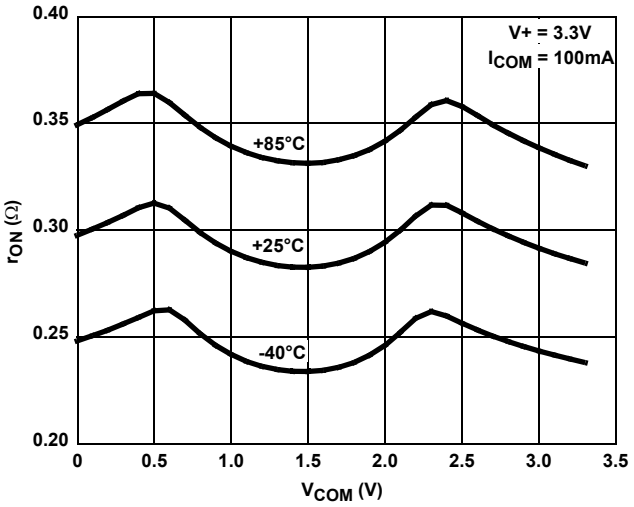


FIGURE 14. ON RESISTANCE vs SWITCH VOLTAGE

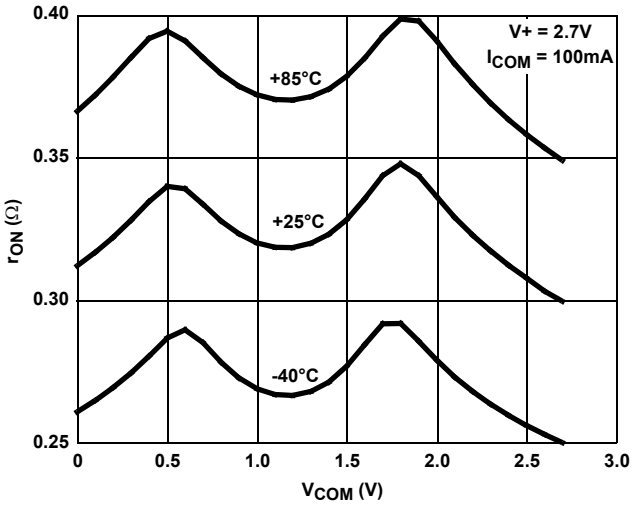


FIGURE 15. ON-RESISTANCE vs SWITCH VOLTAGE

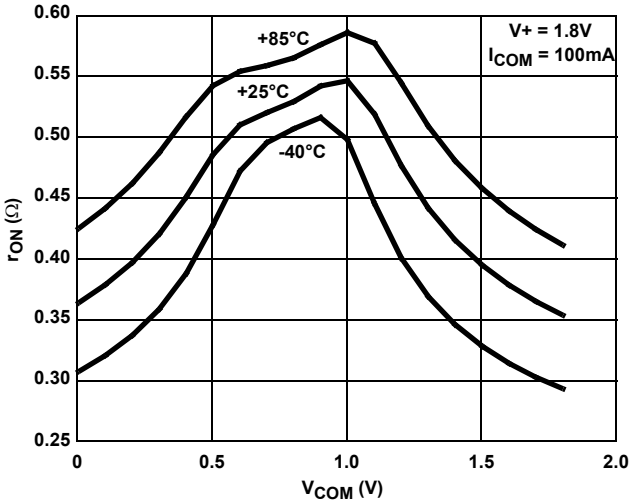


FIGURE 16. ON-RESISTANCE vs SWITCH VOLTAGE

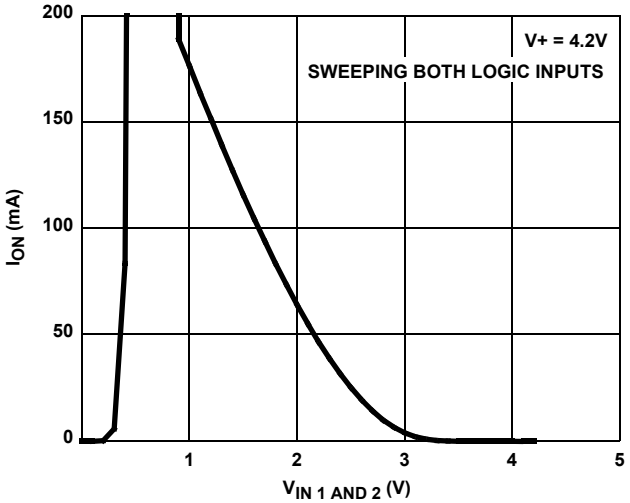


FIGURE 17. SUPPLY CURRENT vs VLOGIC VOLTAGE

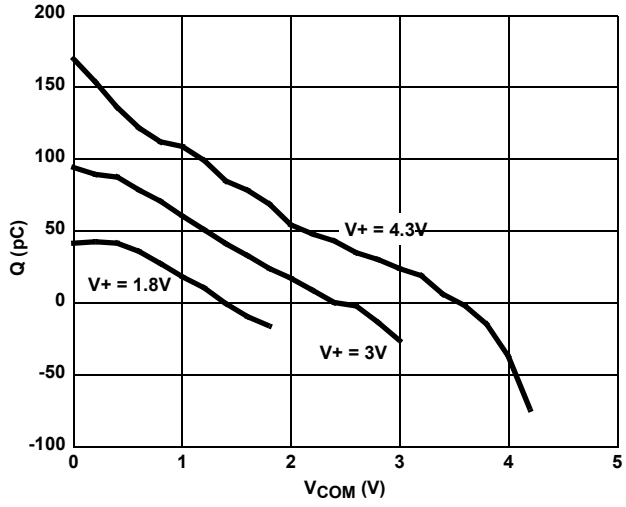


FIGURE 18. CHARGE INJECTION vs SWITCH VOLTAGE

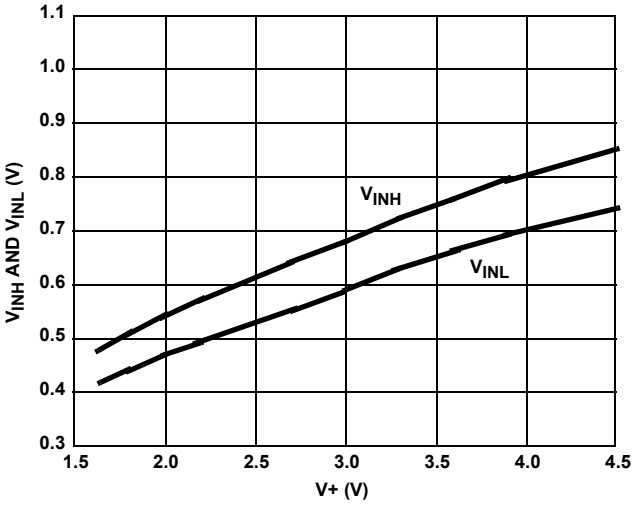


FIGURE 19. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified. **(Continued)**

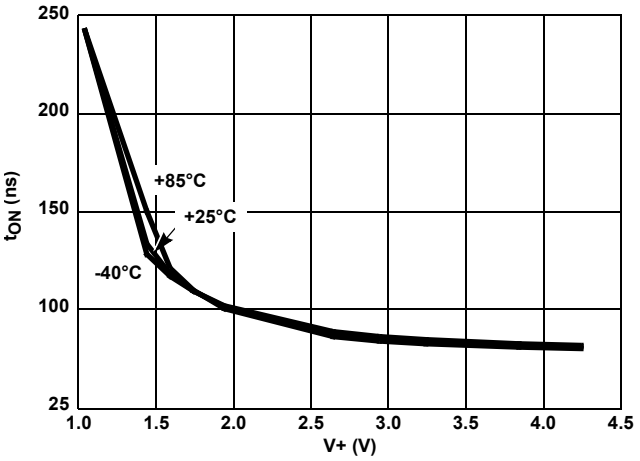


FIGURE 20. TURN-ON TIME vs SUPPLY VOLTAGE

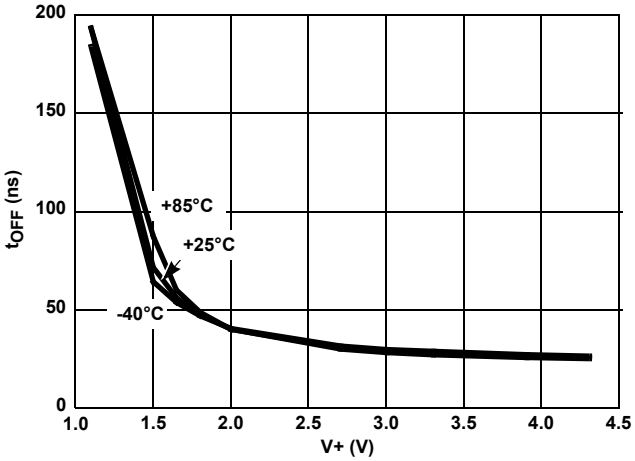


FIGURE 21. TURN-OFF TIME vs SUPPLY VOLTAGE

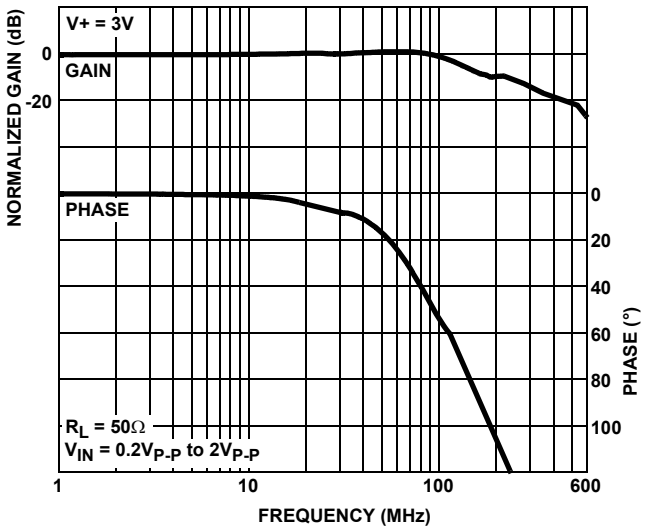


FIGURE 22. FREQUENCY RESPONSE

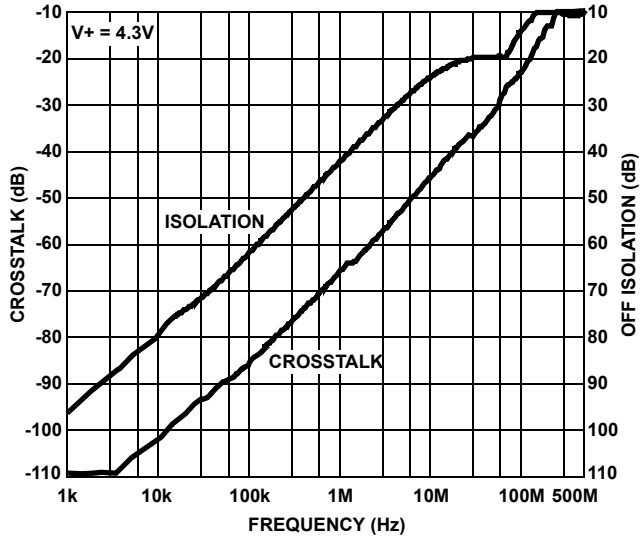


FIGURE 23. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (DFN Paddle Connection: Tie to GND or Float)

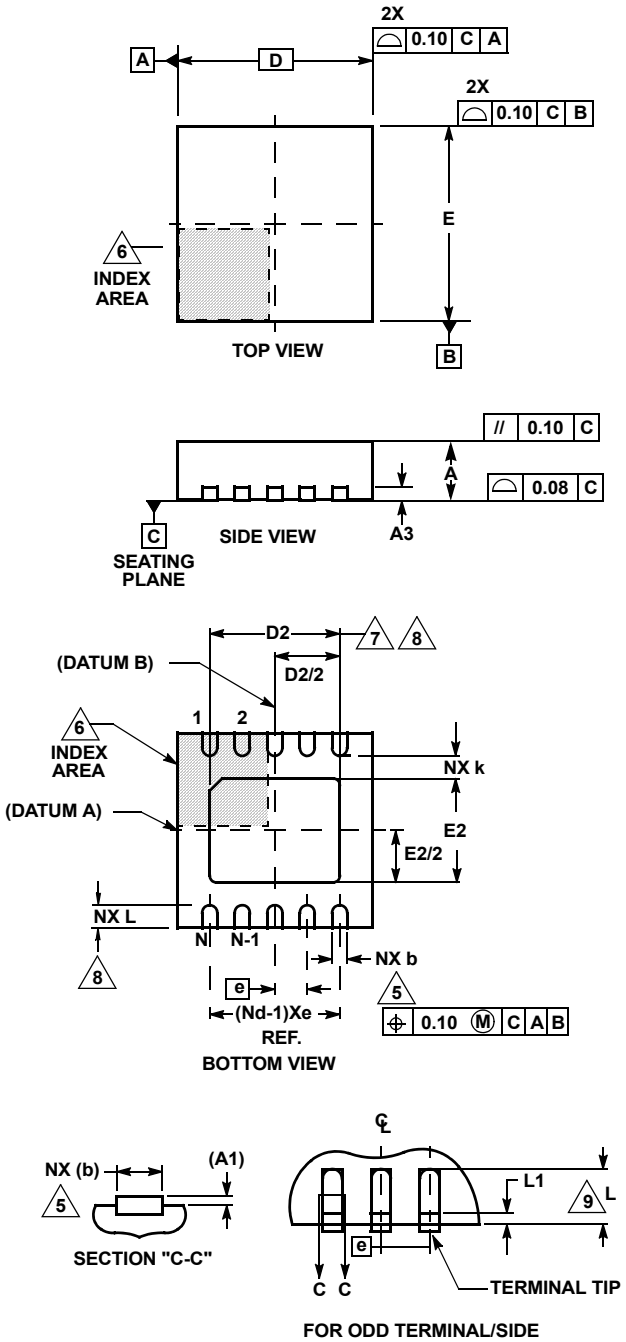
TRANSISTOR COUNT:

114

PROCESS:

Submicron CMOS

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

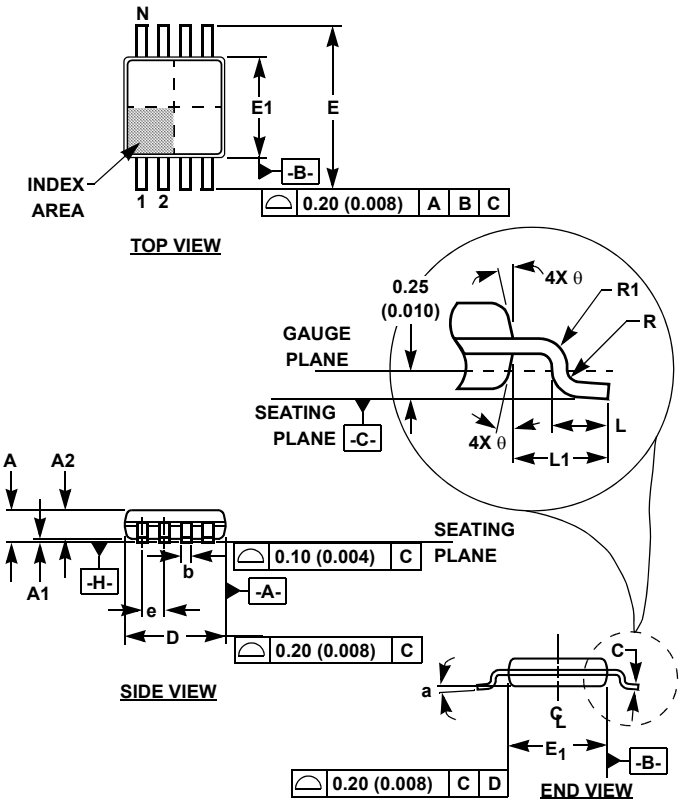
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

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