NOT RECOMMENDED FOR NEW DESIGNS
RECOMMENDED REPLACEMENT PART
ICL3222EIVZ

ISL83385E

±15kV ESD Protected, +3V to +5.5V, 1 Microamp, 250kbps, RS-232 Transmitters/Receivers

FN6001
Rev 4.00
January 16, 2005

The Intersil ISL83385E contains 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Targeted applications are PDAs, Palmtops, and notebook and laptop computers where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with a manual powerdown function reduces the standby supply current to a 1µA trickle. Small footprint packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions. This device is fully compatible with 3.3V only systems, mixed 3.3V and 5.0V systems, and 5.0V only systems.

The single pin powerdown function ($\overline{SHDN}$ = 0) disables all the transmitters, while shutting down the charge pump to minimize supply current drain.

Table 1 summarizes the features of the ISL83385E, while Application Note AN9863 summarizes the features of each device comprising the 3V RS-232 family.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL83385ECA	83385ECA	0 to 70	20 Ld SSOP	M20.209
ISL83385ECAZ (See Note)	83385ECAZ	0 to 70	20 Ld SSOP (Pb-free)	M20.209
ISL83385EIA	83385EIA	-40 to 85	20 Ld SSOP	M20.209
ISL83385EIAZ (See Note)	83385EIAZ	-40 to 85	20 Ld SSOP (Pb-free)	M20.209
ISL83385EIB	83385EIB	-40 to 85	18 Ld SOIC	M18.3
ISL83385EIBZ (See Note)	83385EIBZ	-40 to 85	18 Ld SOIC (Pb-free)	M18.3

Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Low Power, Pin Compatible Upgrade for MAX3385E
- Single $\overline{SHDN}$ Pin Disables Transmitters
- RS-232 Compatible Outputs at 2.7V
- Receivers Active in Powerdown
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- Latch-Up Free
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Receiver Hysteresis For Improved Noise Immunity
- Very Low Supply Current 0.3mA
- Guaranteed Minimum Data Rate 250kbps
- Guaranteed Minimum Slew Rate 6V/µs
- Wide Power Supply Range . . . . . Single +3V to +5.5V
- Low Supply Current in Powerdown State . . . . . <1µA
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

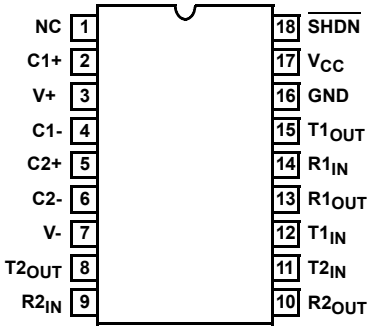
- Any System Requiring RS-232 Communication Ports
  - Battery Powered, Hand-Held, and Portable Equipment
  - Laptop Computers, Notebooks, Palmtops
  - Modems, Printers and other Peripherals
  - Digital Cameras
  - Cellular/Mobile Phones

TABLE 1. SUMMARY OF FEATURES

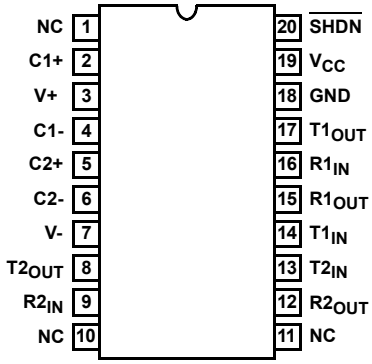
PART NUMBER	NO. OF Tx.	NO. OF Rx.	NO. OF MONITOR Rx. (R_{OUTB})	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	READY OUTPUT?	MANUAL POWER-DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ISL83385E	2	2	0	250	No	No	Yes	No

Pinouts

ISL83385E (SOIC)
TOP VIEW



ISL83385E (SSOP)
TOP VIEW

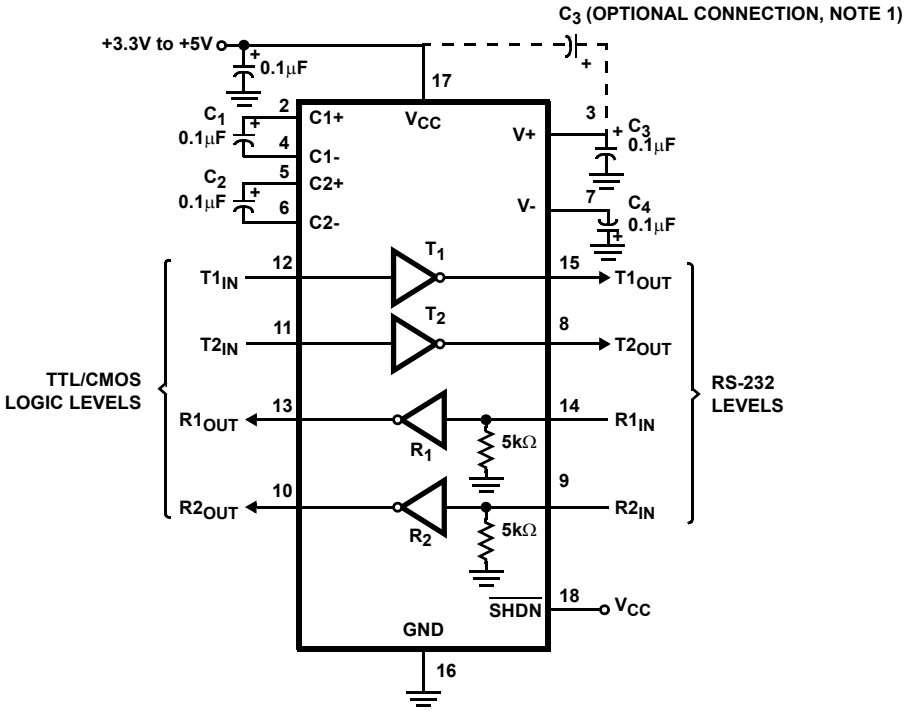


Pin Descriptions

PIN	FUNCTION
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs.
T_{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs.
$\overline{SHDN}$	Active low input to shut down transmitters and on-board power supply, to place device in low power mode.

Typical Operating Circuit

ISL83385E (Note 2)



NOTES:

1. The negative terminal of C_3 can be connected to either V_{CC} or Gnd.
2. Pin numbers refer to SOIC package.

Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground. . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
  T_{IN}, $\overline{SHDN}$ . . . . . -0.3V to 6V
  R_{IN} . . . . . ±25V
Output Voltages
  T_{OUT} . . . . . ±13.2V
  R_{OUT} . . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
  T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
18 Ld SOIC Package	75
20 Ld SSOP Package	125

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Temperature Range
  ISL83385ECX . . . . . 0°C to 70°C
  ISL83385EIX . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = 25°C

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Current, Enabled	All Outputs Unloaded, $\overline{SHDN}$ = V_{CC}, V_{CC} = 3.15V		25	-	0.3	1	mA
Supply Current, Powerdown	$\overline{SHDN}$ = GND		25	-	1	10	µA
LOGIC AND TRANSMITTER INPUTS							
Input Logic Threshold Low	T_{IN}, $\overline{SHDN}$		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, $\overline{SHDN}$	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Transmitter Input Hysteresis			25	-	0.5	-	V
Input Leakage Current	T_{IN}, $\overline{SHDN}$		Full	-	±0.01	±1.0	µA
RECEIVER OUTPUTS							
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} -0.6	V_{CC} -0.1	-	V
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, $\overline{SHDN}$ = GND		Full	-	-	±25	µA

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	250	500	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Transmitter Output Enable Time	From $\overline{SHDN}$ Rising Edge to T_{OUT} = ±3.7V		25	-	100	-	µs
Transmitter Skew	t_{PHL} - t_{PLH} (Note 4)		25	-	100	-	ns
Receiver Skew	t_{PHL} - t_{PLH}		25	-	50	-	ns
Transition Region Slew Rate	R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V, V_{CC} = 3.3V	C_L = 150pF to 1000pF	25	6	-	30	V/µs
		C_L = 150pF to 2500pF	25	4	-	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model		25	-	±15	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
All Other Pins	Human Body Model		25	-	±3	-	kV

NOTE:

4. Transmitter skew is measured at the transmitter zero crossing points.

Detailed Description

The ISL83385E operates from a single +3V to +5.5V supply, guarantees a 250kbps minimum data rate, requires only four small external 0.1µF capacitors, features low power consumption, and meets all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge-Pump

Intersil's new ISL83385E utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions over the full V_{CC} range; other capacitor combinations can be used as shown in Table 3. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (see Table 2). These outputs may be driven to ±12V when disabled.

All devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq$ 3.0V, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq$ 3.3V, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected (there are no pull-up resistors), and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

TABLE 2. POWERDOWN TRUTH TABLE

$\overline{SHDN}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	MODE OF OPERATION
H	Active	Active	Normal Operation
L	High-Z	Active	Manual Powerdown

Receivers

The ISL83385E contains standard inverting receivers that convert RS-232 signals to CMOS output levels and accept inputs up to ±30V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 1) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses

hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

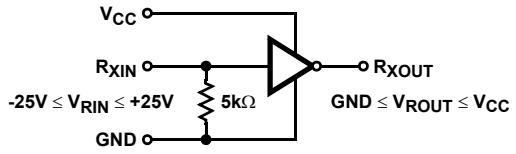


FIGURE 1. INVERTING RECEIVER CONNECTIONS

Low Power Operation

This 3V device requires a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in powerdown mode). This is considerably less than the 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by replacing the old style device with the ISL83385E in new designs.

Powerdown Functionality

The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to 1µA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter outputs three-state. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Powerdown

The ISL83385E may be forced into its low power, standby state via a simple shutdown ($\overline{SHDN}$) pin (see Figure 2). Driving this pin high enables normal operation, while driving it low forces the IC into it's powerdown state. The time required to exit powerdown, and resume transmission is less than 100µs. Connect $\overline{SHDN}$ to V_{CC} if the powerdown function isn't needed.

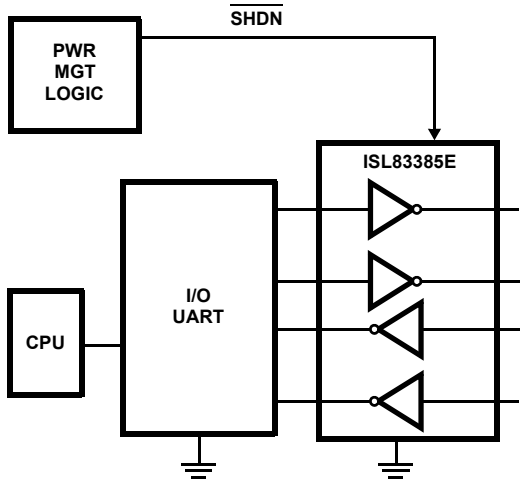


FIGURE 2. CONNECTIONS FOR MANUAL POWERDOWN

Capacitor Selection

These charge pumps only require 0.1µF capacitors for the full operational voltage range. Table 3 lists other acceptable capacitor values for various supply voltage ranges. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Operation Down to 2.7V

ISL83385E transmitter outputs meet RS-562 levels (±3.7V), at the full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure inter operability with RS-232 devices.

Transmitter Outputs when Exiting Powerdown

Figure 3 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

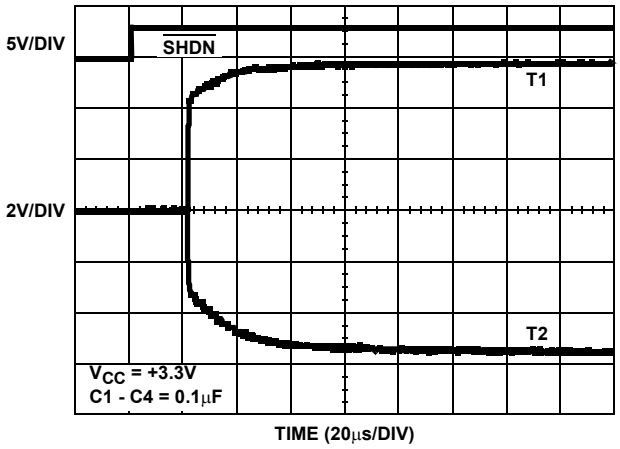


FIGURE 3. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

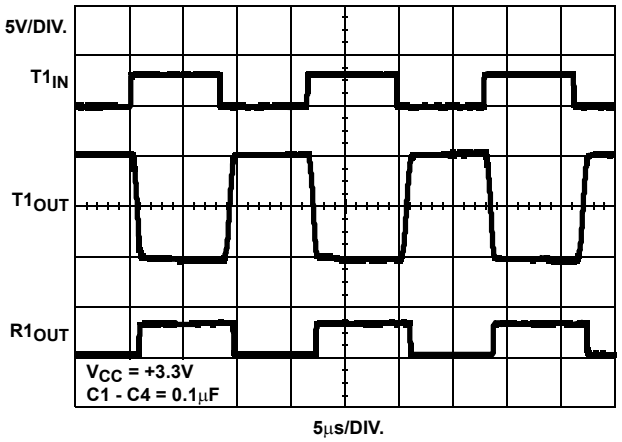


FIGURE 5. LOOPBACK TEST AT 120kbps

High Data Rates

The ISL83385E maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 4 details a transmitter loopback test circuit, and Figure 5 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 6 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitter was also loaded with an RS-232 receiver.

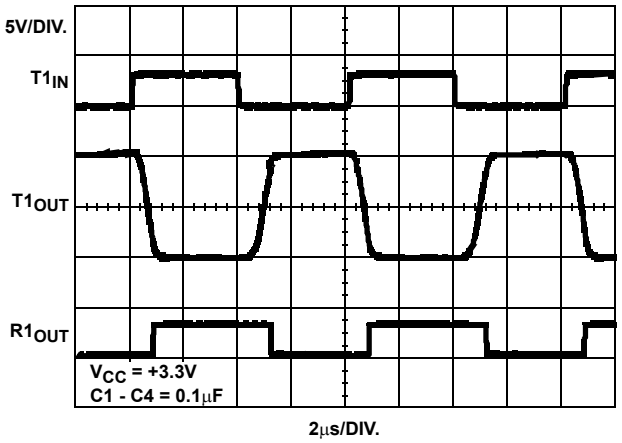


FIGURE 6. LOOPBACK TEST AT 250kbps

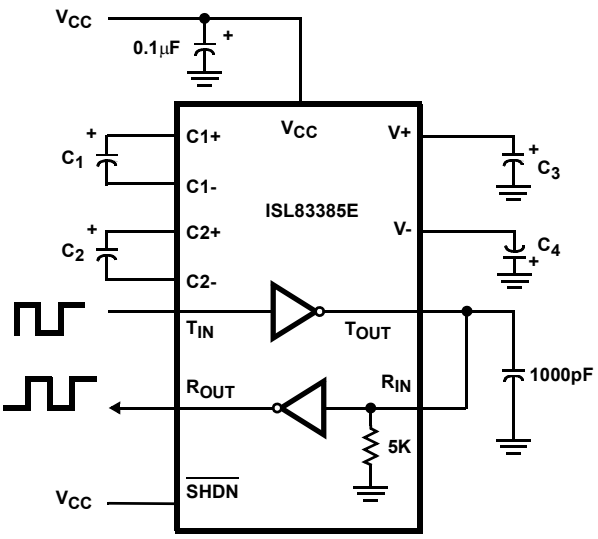


FIGURE 4. TRANSMITTER LOOPBACK TEST CIRCUIT

Interconnection with 3V and 5V Logic

The ISL83385E directly interfaces with 5V CMOS and TTL logic families. Nevertheless, with the device at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can drive ISL83385E inputs, but ISL83385E outputs do not reach the minimum V_{IH} for these logic families. See Table 4 for more information.

TABLE 4. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ISL83385E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on the 3V interface devices include ESD protection structures, but the ISL83385E incorporates advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C

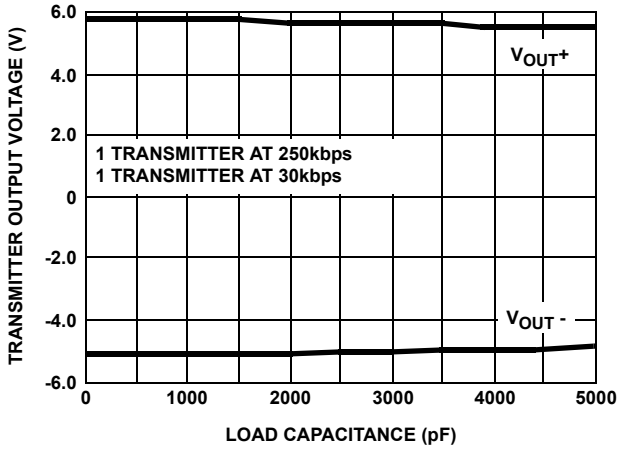


FIGURE 7. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

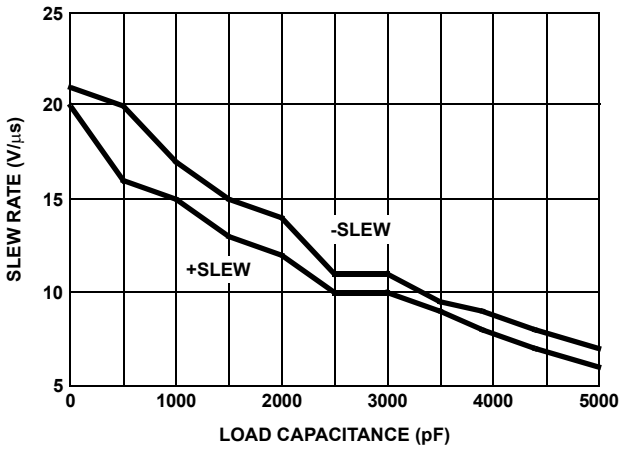


FIGURE 8. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C **(Continued)**

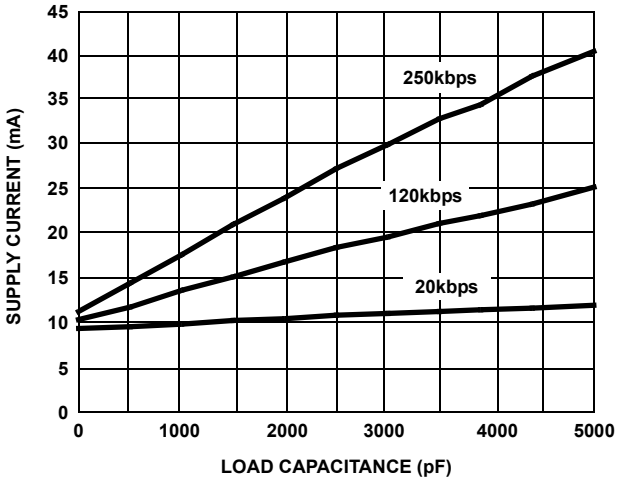


FIGURE 9. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

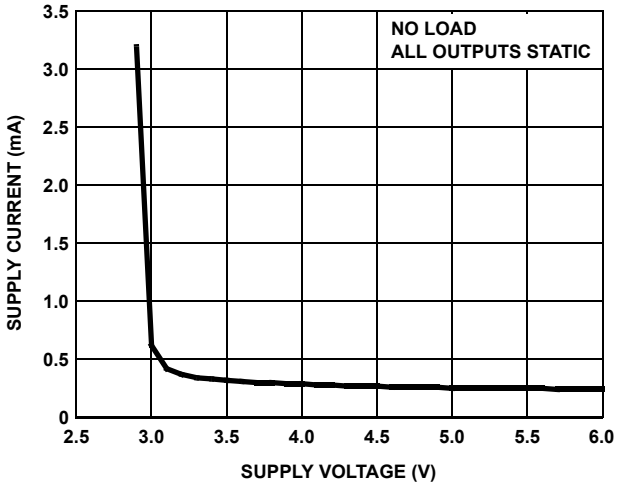


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP)

GND

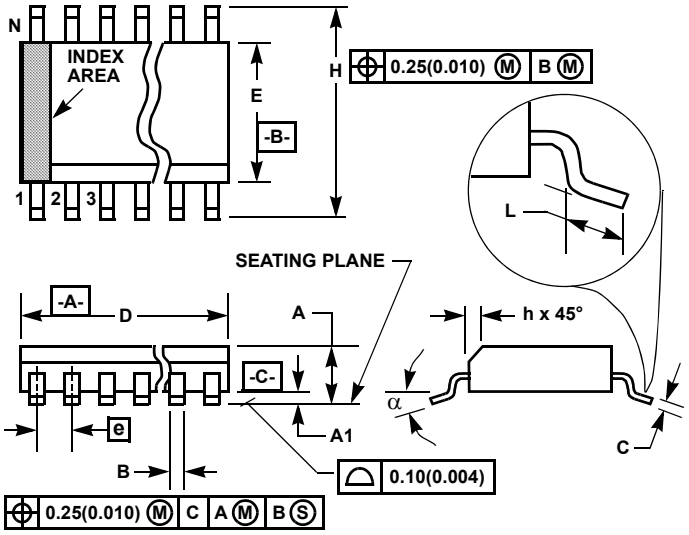
TRANSISTOR COUNT

338

PROCESS

Si Gate CMOS

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

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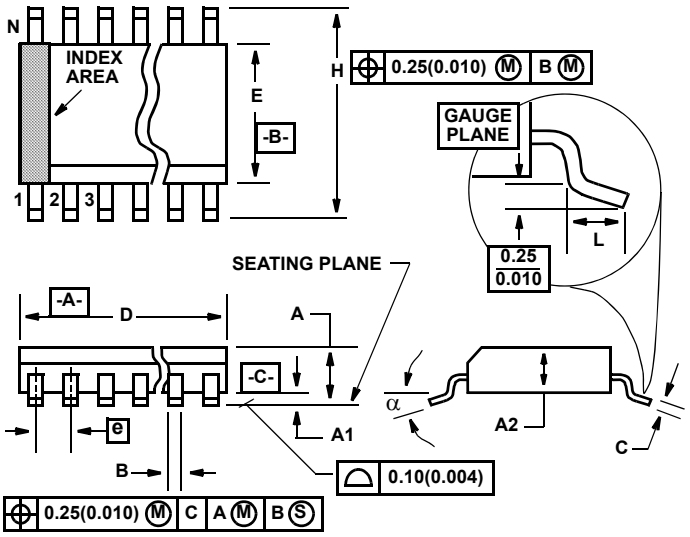
Shrink Small Outline Plastic Packages (SSOP)



M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.068	0.078	1.73	1.99	
A1	0.002	0.008’	0.05	0.21	
A2	0.066	0.070’	1.68	1.78	
B	0.010’	0.015	0.25	0.38	9
C	0.004	0.008	0.09	0.20’	
D	0.278	0.289	7.07	7.33	3
E	0.205	0.212	5.20’	5.38	4
e	0.026 BSC		0.65 BSC		
H	0.301	0.311	7.65	7.90’	
L	0.025	0.037	0.63	0.95	6
N	20		20		7
α	0 deg.	8 deg.	0 deg.	8 deg.	

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “B” does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of “B” dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.