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ISL55036

400MHz Slew Rate Enhanced Rail-to-Rail Output Gain Block

FN6640
Rev 1.00
September 11, 2008

The ISL55036 is a hex, rail-to-rail output, fixed gain amplifier (G = 4) with a -3dB bandwidth of 400MHz and slew rate of 2500V/µs into a 150Ω load. The ISL55036 features single supply operation over a voltage range of 3VDC to 5.5VDC. The inputs are capable of sensing ground with an output swing of VCC - 0.3V into a 150Ω load tied to V+/2. The part includes a fast-acting global disable/power-down circuit. The ISL55036 is available in a 24 Ld TQFN package. Operation is specified over the -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL55036IRTZ	55036 IRTZ	24 Ld TQFN	L24.4x5C
ISL55036IRTZ-T13*	55036 IRTZ	24 Ld TQFN	L24.4x5C

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

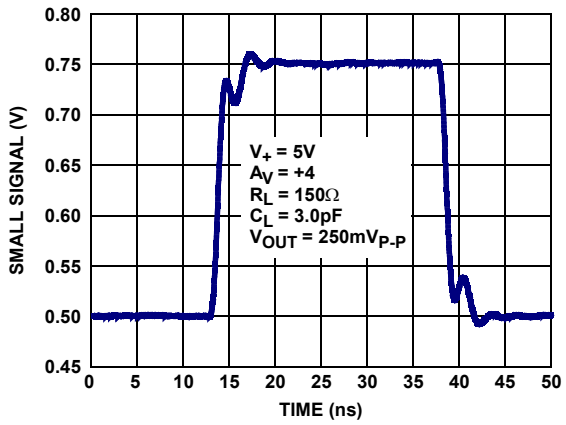


FIGURE 1. SMALL SIGNAL STEP RESPONSE

Features

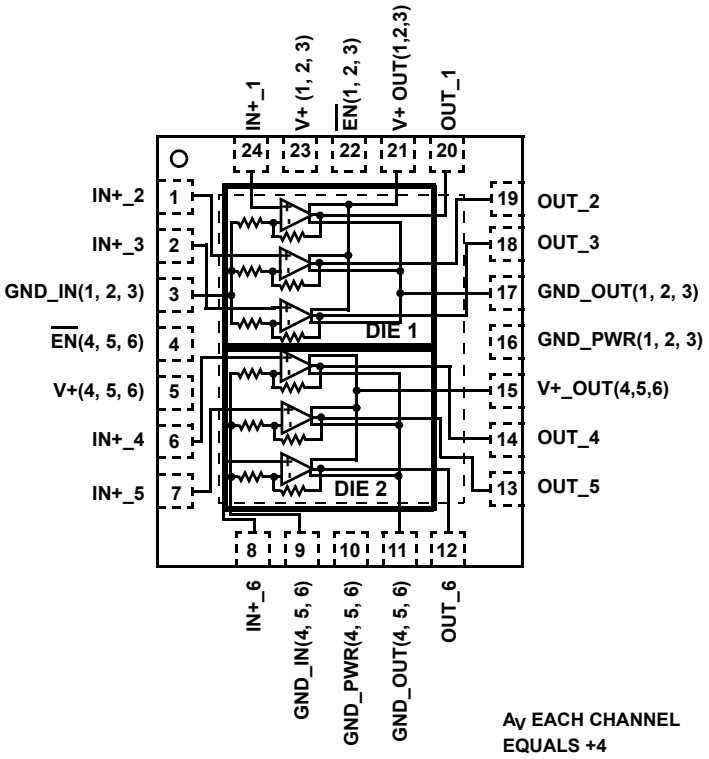
- 400MHz -3dB Bandwidth
- 2500V/µs Typical Slew Rate, R_L = 150Ω
- Supplies from 3V to 5.5V
- Rail-to-Rail Output (R_L = 1k)
- Input Ground Sensing
- Fast 25ns Disable
- Low Cost
- Pb-Free (RoHS Compliant)

Applications

- Video RGB Line Driver
- LCD Based Projectors Pixel Control

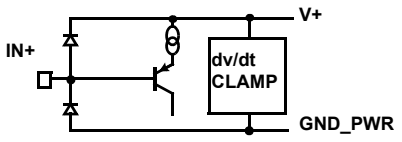
Pinout

ISL55036
24 LD TQFN
TOP VIEW

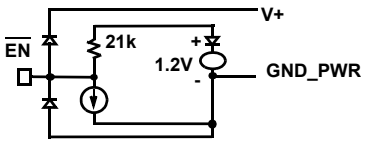


Pin Descriptions

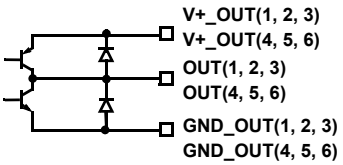
24 LD TQFN	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	IN+_2	Circuit 1	Amplifier 2 non-inverting input
2	IN+_3	Circuit 1	Amplifier 3 non-inverting input
3	GND_IN(1, 2, 3)	Circuit 4	Common reference input for Amplifiers 1, 2, 3
4	$\overline{EN}$(4, 5, 6)	Circuit 2	$\overline{Enable}$ pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state. Channels 4, 5, 6
5	V+(4, 5, 6)	Circuit 5	Positive power supply for Channels 4, 5, 6.
6	IN+_4	Circuit 1	Amplifier 4 non-inverting input
7	IN+_5	Circuit 1	Amplifier 5 non-inverting input
8	IN+_6	Circuit 1	Amplifier 6 non-inverting input
9	GND_IN(4, 5, 6)	Circuit 5	Common reference input for Amplifiers 4, 5, 6
10	GND_PWR(4, 5, 6)	Circuit 5	Power supply ground for Channels 4, 5, 6.
11	GND_OUT(4, 5, 6)	Circuit 3	Output power supply ground for Channels 4, 5, 6.
12	OUT_ 6	Circuit 3	Amplifier 6 output
13	OUT_ 5	Circuit 3	Amplifier 5 output
14	OUT_4	Circuit 3	Amplifier 4 output
15	V+_OUT(4, 5, 6)	Circuit 3	Output power supply for Channels 4, 5, 6.
16	GND_PWR(1, 2, 3)	Circuit 4	Power supply ground Channels 1, 2, 3.
17	GND_OUT(1, 2, 3)	Circuit 3	Output power supply ground Channels 1, 2, 3.
18	OUT_3	Circuit 3	Amplifier 3 output
19	OUT_2	Circuit 3	Amplifier 2 output
20	OUT_1	Circuit 3	Amplifier 1 output
21	V+_OUT(1, 2, 3)	Circuit 3	Output power supply Channels 1, 2, 3.
22	$\overline{EN}$(1, 2, 3)	Circuit 2	$\overline{Enable}$ pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state. Channels 1, 2, 3
23	V+(1, 2, 3)	Circuit 4	Positive power supply for Channels 1, 2, 3.
24	IN+_1	Circuit 1	Amplifier 1 non-inverting input
	Thermal Pad	Circuit 6	Thermal heat sink pad makes electrical contact the IC substrate and must be connected to same ground potential as the ground pins.



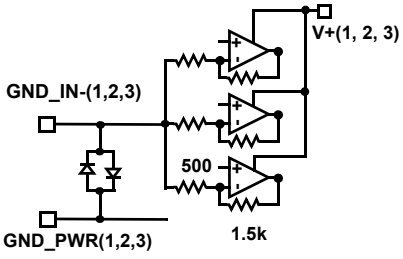
CIRCUIT 1



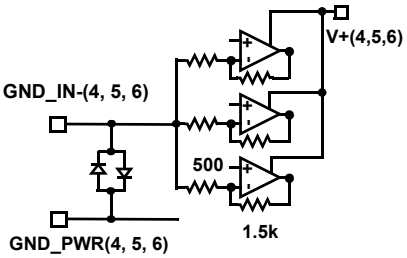
CIRCUIT 2



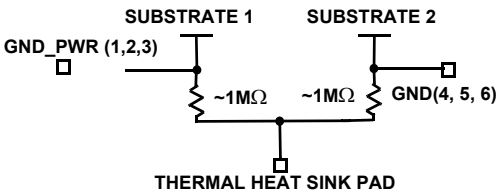
CIRCUIT 3



CIRCUIT 4



CIRCUIT 5



CIRCUIT 6

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V+ to GND 5.75V
Supply Turn On Voltage Slew Rate 1V/µs
$\overline{EN}$ Input Current 4mA
Input Voltage . . . . . V+ + 0.3V to GND - 0.3V
Continuous Output Current 40mA
ESD Rating:
Human Body Model 3,000V
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
24 Ld TQFN Package 42
Storage Temperature . . . . . -65°C to +125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

V_+ = 5V, T_A = +25°C, R_L = 1k to $V_+/2$, A_V = 4, V_{IN} = 0.1VDC, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
INPUT CHARACTERISTICS						
TCV_{OS}	Offset Voltage Temperature Coefficient	Measured from -40°C to +85°C		-3		µV/°C
IB	Input Bias Current	V_{IN} = 0V	-10	-5.5	-2.5	µA
R_{IN}	Input Resistance			7		MΩ
C_{IN}	Input Capacitance			0.5		pF
OUTPUT CHARACTERISTICS						
V_{OS}	Output Offset Voltage	Note 2	-14	-2	10	mV
A_{CL}	Closed Loop Gain	R_L = 1k, 150Ω, V_{OUT} = 0.5V to 4V	3.9	4	4.1	V/V
R_{OUT}	Output Resistance	A_V = +4		30		mΩ
V_{OP}	Positive Output Voltage Swing	R_L = 1kΩ to 2.5V		4.86		V
		R_L = 150Ω to 2.5V		4.65		V
V_{ON}	Negative Output Voltage Swing	R_L = 1kΩ to 2.5V		27		mV
		R_L = 150Ω to 2.5V		140		mV
I_{SC} (source)	Output Short Circuit Current	R_L = 10Ω to GND, V_{IN} = 1.5V	60	95		mA
I_{SC} (sink)	Output Short Circuit Current	R_L = 10Ω to + 2.5V, V_{IN} = 0V	70	105		mA
POWER SUPPLY						
PSRR	Power Supply Rejection Ratio @ 1kHz	V+ = 5V; V_{SOURCE} = $1V_{P-P}$; f = 1kHz sine wave		78		dB
I_{S-ON}	Supply Current - Enabled per Amplifier	R_L = Open	6.0	7.2	8.5	mA
I_{S-OFF}	Supply Current - All Amplifiers Disabled	R_L = Open	0.5	1.1	2	mA
ENABLE						
t_{EN}	Enable Time	R_L = 150Ω, V_{IN} = 0.25V		250		ns
t_{DS}	Disable Time	R_L = 150Ω, V_{IN} = 0.25V		25		ns
V_{IH-ENB}	$\overline{ENABLE}$ Pin Voltage for Power-Up			0.8		V
V_{IL-ENB}	$\overline{ENABLE}$ Pin Voltage for Shut-Down			2		V

Electrical Specifications $V_+ = 5V$, $T_A = +25°C$, $R_L = 1k$ to $V_+/2$, $A_V = 4$, $V_{IN} = 0.1VDC$, Unless Otherwise Specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
I_{IH-ENB}	$\overline{ENABLE}$ Pin Input Current High	$V_{\overline{EN}} = 5V$	1	5.5	20	µA
I_{IL-ENB}	$\overline{ENABLE}$ Pin Input for Current Low	$V_{\overline{EN}} = 0V$	-4		4	µA
AC PERFORMANCE						
BW	-3dB Bandwidth	$R_L = 150\Omega$, $C_L = 3pF$		400		MHz
BW	±0.1dB Bandwidth	$R_L = 150\Omega$, $C_L = 3pF$		40		MHz
Peak	Peaking	$R_L = 150\Omega$, $C_L = 3pF$		1		dB
dG	Differential Gain	$V_{IN} = 0.1V$ to $1.0V$, $V_{OUT} = 100mV_{P-P}$, $f = 3.58MHz$, $R_L = 150\Omega$		0.06		%
dP	Differential Phase			0.01		°
e_{N-OUT}	Output Noise Voltage	f = 10kHz		50		nV/√Hz
i_N	Input Noise Current	f = 10kHz		0.9		pA/√Hz
ISO	Off-State Isolation $f_O = 10MHz$	$V_{IN} = 0.6VDC + 1V_{P-P}$, $C_L = 3pF$, $R_L = 150\Omega$		-100		dB
X-TALK	Die to Die Crosstalk $f_O = 10MHz$	$V_{IN} = 0.6VDC + 1V_{P-P}$, $C_L = 3pF$, $R_L = 150\Omega$		-85		dB
	Same Die Channel-to-Channel Crosstalk, $f_O = 10MHz$			-65		dB
PSRR	Power Supply Rejection Ratio $f_O = 10MHz$	$V_{SOURCE} = 1V_{P-P}$, $C_L = 3pF$, $R_L = 150\Omega$		-55		dB
TRANSIENT RESPONSE						
SR	Slew Rate 25% to 75%	$R_L = 150\Omega$, $V_{OUT} = 0.5V$ to $4.5V$		2500		V/µs
t_r, t_f Large Signal	Rise Time, t_r 20% to 80%	$V_{OUT} = 4V_{P-P}$, $R_L = 150\Omega$, $C_L = 3pF$		1.4		ns
	Fall Time, t_f 20% to 80%			1		ns
	Rise Time, t_r 20% to 80%	$V_{OUT} = 2V_{P-P}$, $R_L = 150\Omega$, $C_L = 3pF$		0.8		ns
	Fall Time, t_f 20% to 80%			0.7		ns
t_r, t_f, Small Signal	Rise Time, t_r 20% to 80%	$V_{OUT} = 0.2V_{P-P}$, $R_L = 150\Omega$, $C_L = 3pF$		0.75		ns
	Fall Time, t_f 20% to 80%			0.7		ns
OS	Overshoot	200mV step		5		%
t_{PD}	Propagation Delay	200mV step		0.6		ns
t_S	1% Settling Time	2V step		12		ns
$t_{\overline{EN}}$	ENABLE to Output Turn-on Delay Time; 10% $\overline{EN}$ - 10% V_{OUT}	$V_{OUT} = 1VDC$, $R_L = 150\Omega$, $C_L = 3pF$		250		ns
	ENABLE to Output Turn-off Delay Time; 10% $\overline{EN}$ - 10% V_{OUT}	$V_{OUT} = 1VDC$, $R_L = 150\Omega$, $C_L = 3pF$		25		ns

NOTES:

2. V_{OS} is extrapolated from 2 output voltage measurements, with $V_{IN} = 62.5mV$ and $V_{IN} = 125mV$, $R_L = 1k$.
3. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

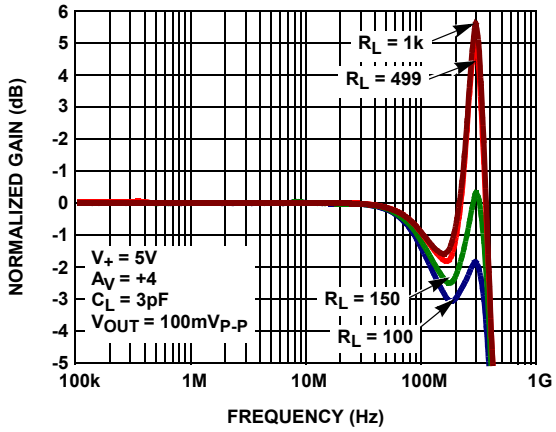


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD}

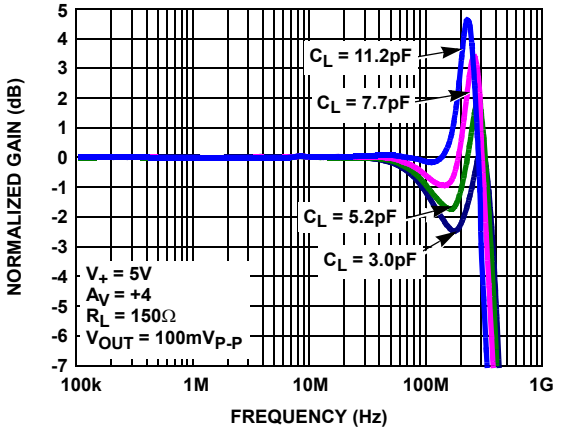


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

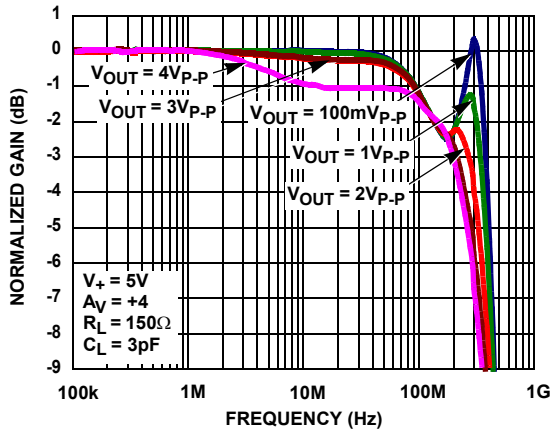


FIGURE 4. -3dB BANDWIDTH vs V_{OUT}

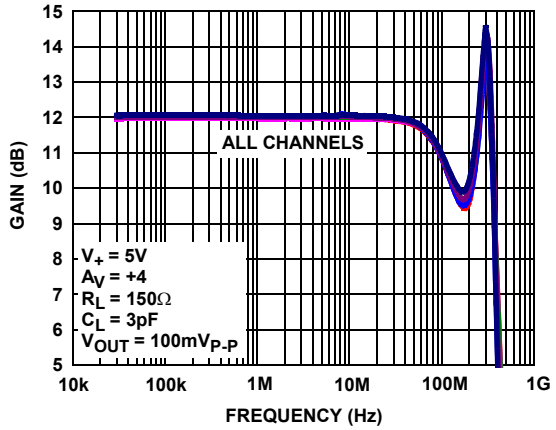


FIGURE 5. GAIN vs FREQUENCY - ALL CHANNELS

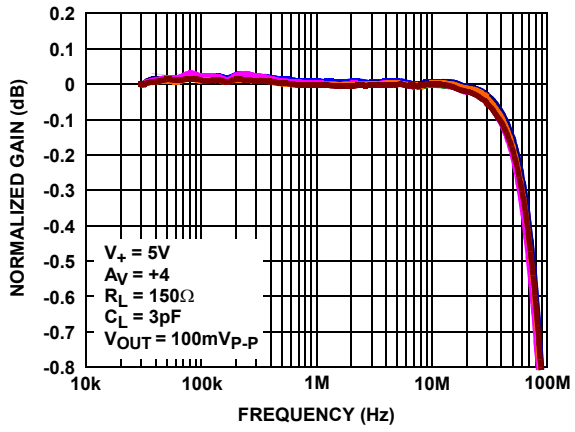


FIGURE 6. 0.1 dB GAIN FLATNESS

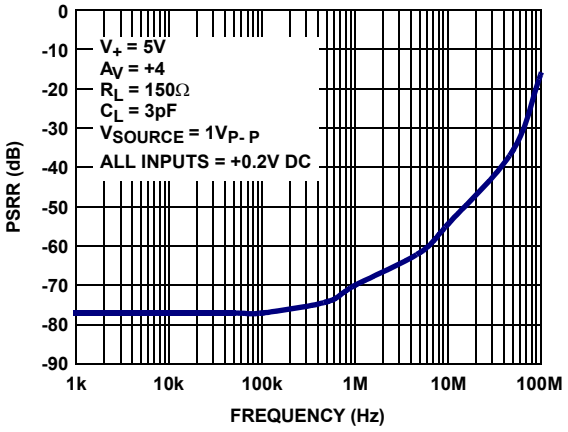


FIGURE 7. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

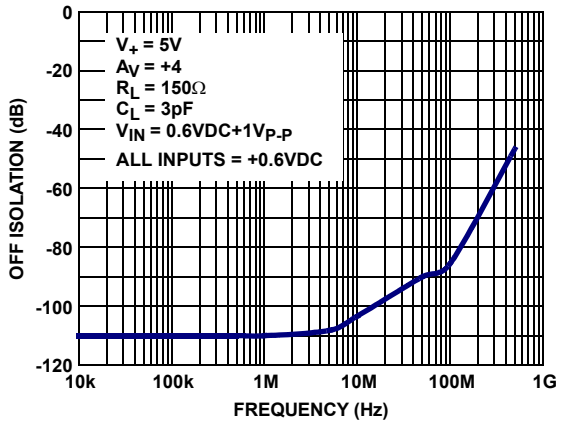


FIGURE 8. OFF ISOLATION vs FREQUENCY

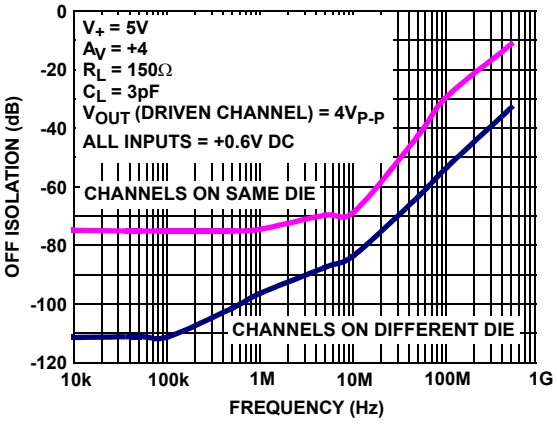


FIGURE 9. CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY

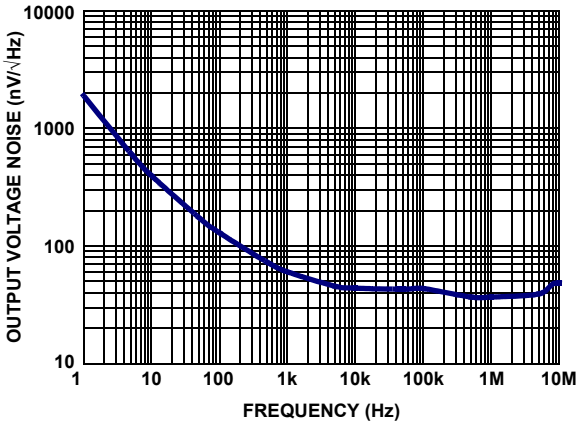


FIGURE 10. OUTPUT NOISE VOLTAGE vs FREQUENCY

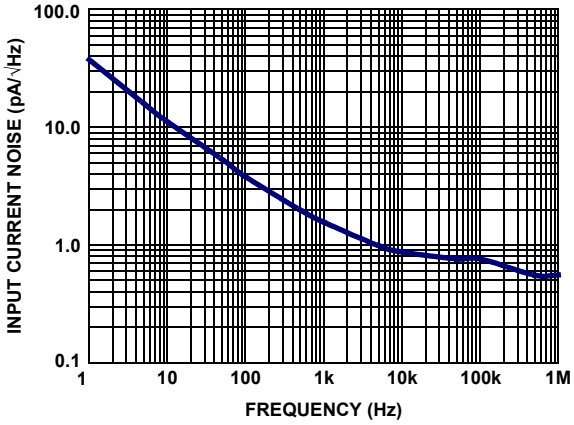


FIGURE 11. INPUT REFERRED NOISE CURRENT vs FREQUENCY

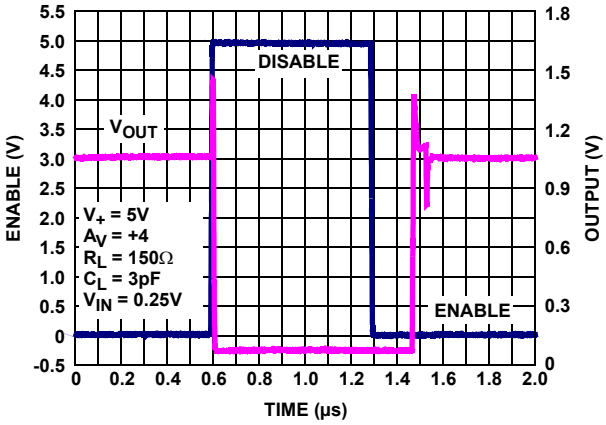


FIGURE 12. ENABLE/DISABLE TIMING

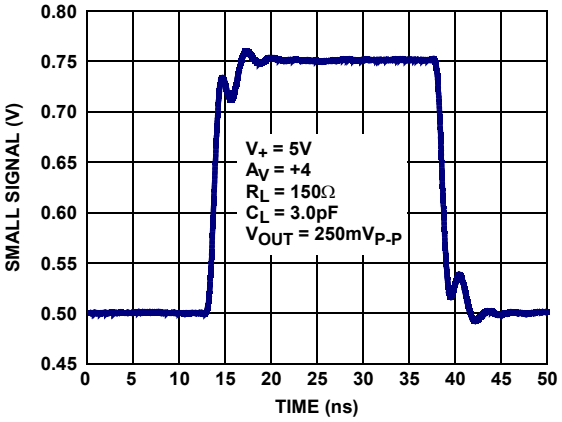


FIGURE 13. SMALL SIGNAL STEP RESPONSE

Typical Performance Curves (Continued)

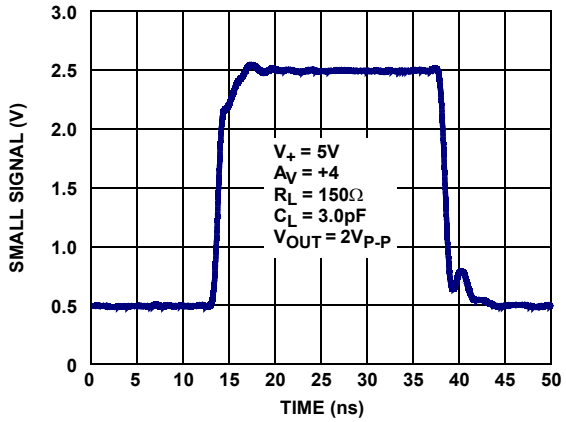


FIGURE 14. SMALL SIGNAL ($2V_{P-P}$) STEP RESPONSE

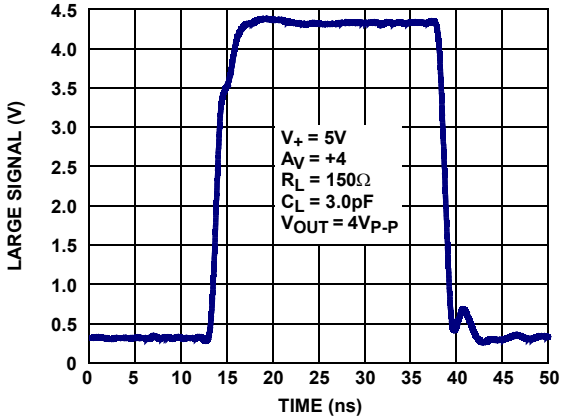


FIGURE 15. LARGE SIGNAL ($4V_{P-P}$) STEP RESPONSE

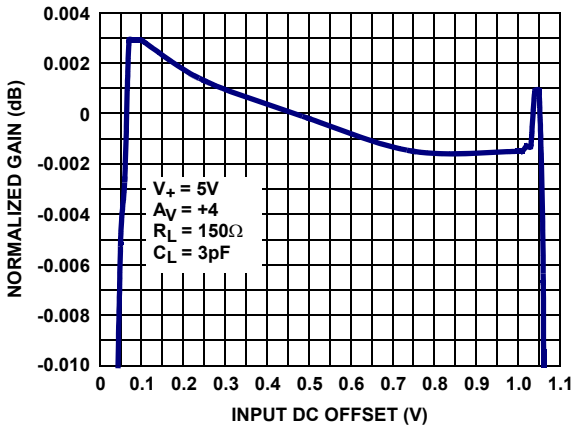


FIGURE 16. DIFFERENTIAL GAIN

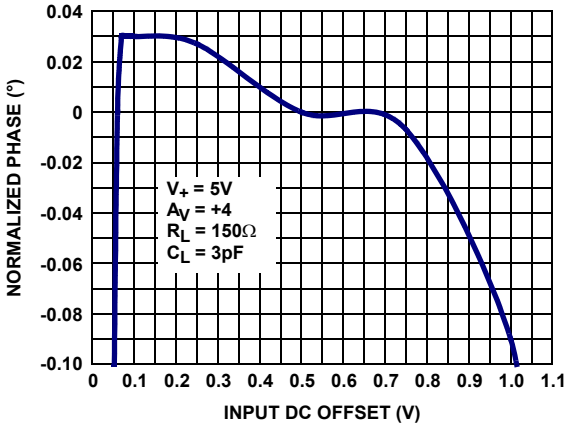


FIGURE 17. DIFFERENTIAL PHASE

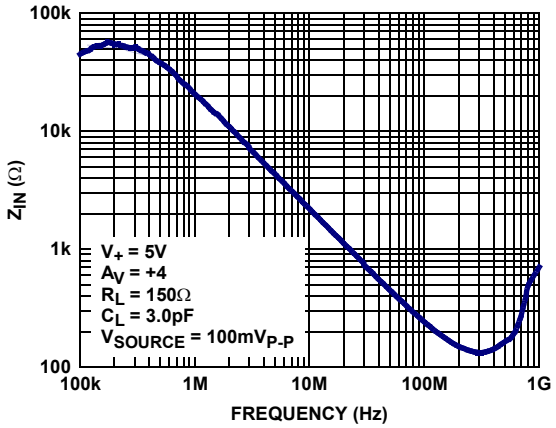


FIGURE 18. Z_{IN} vs FREQUENCY

Typical Performance Curves (Continued)

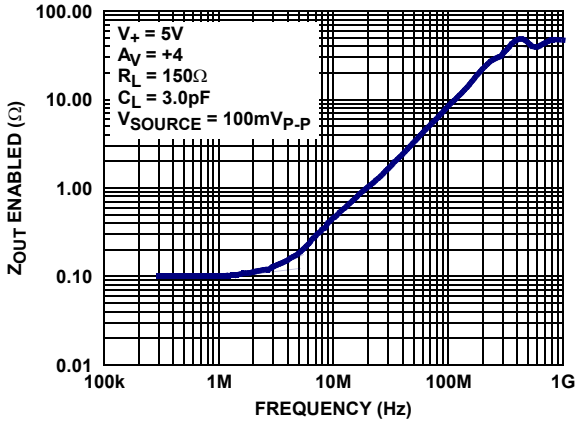


FIGURE 19. Z_{OUT} (ENABLED) vs FREQUENCY

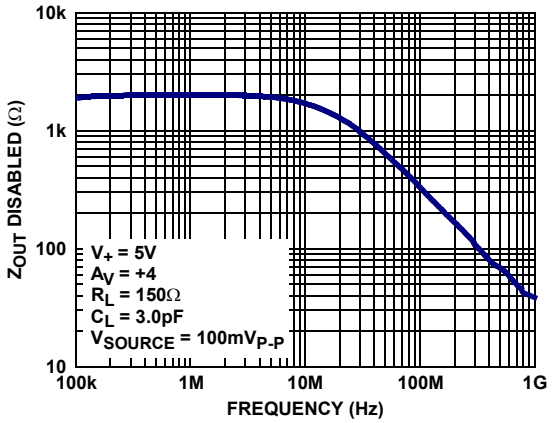


FIGURE 20. Z_{OUT} (DISABLED) vs FREQUENCY

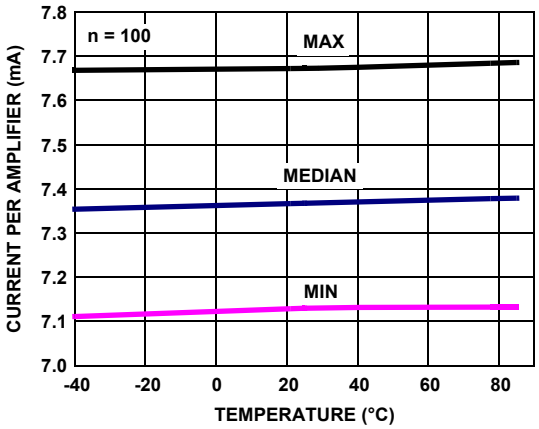


FIGURE 21. ENABLED SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V

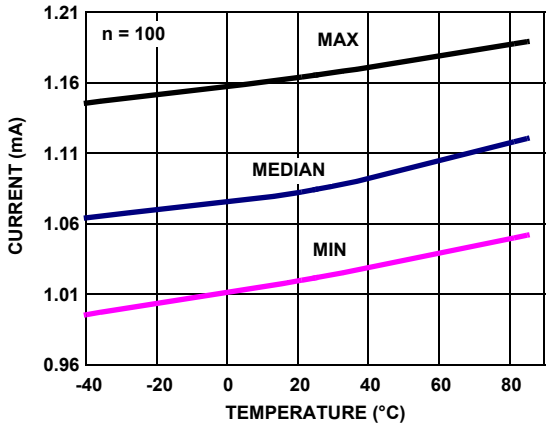


FIGURE 22. DISABLED SUPPLY CURRENT vs TEMPERATURE, V_S = ±2.5V

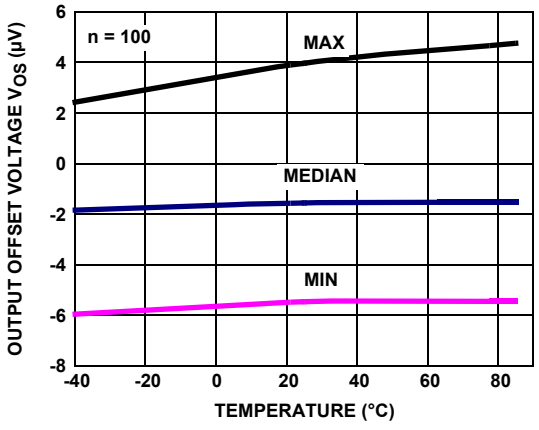


FIGURE 23. OUTPUT OFFSET VOLTAGE V_{OS} vs TEMPERATURE, V_S = ±2.5V, R_L = 1k

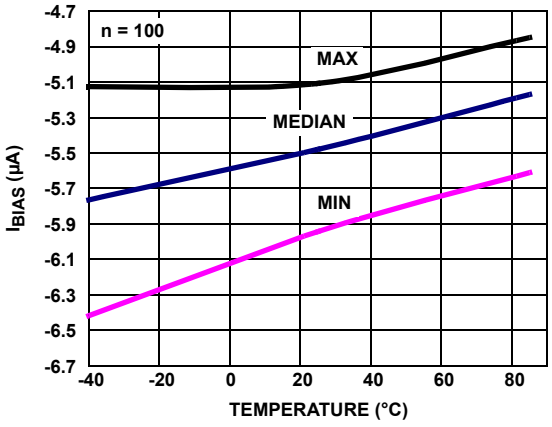


FIGURE 24. I_{BIAS} vs TEMPERATURE, V_S = ±2.5V

Typical Performance Curves (Continued)

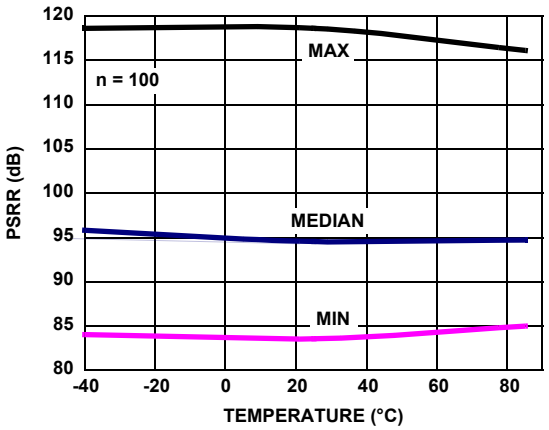


FIGURE 25. PSRR vs TEMPERATURE 4.5V TO 5.5V

Application Information

General

The ISL55036 single supply, fixed gain hex amplifier is well suited for a variety of video applications. The device features a PNP ground-sensing input stage and a bipolar rail-to-rail output stage.

The ISL55036 is designed for general purpose video, communication, instrumentation, and industrial applications. The 6 fixed gain amplifiers operate independently, however, they are organized into 2 triple amplifier groups as shown in Figure 26. Each group has its own set of power supply pins, ground pins, enable-disable logic and input ground reference pins.

Ground Connections

For the best isolation performance and crosstalk rejection, all GND pins must connect directly to the GND plane. In addition, the electrically conductive thermal pad should also connect directly to ground.

Power Considerations

Each triple amplifier group has its own power supply and ground pins. There are dedicated V_+ OUT and GND V_{OUT} pins to power only the output stage. A separate set of power and ground pins power the rest of each of the triple op amps (V_+ and PWR GND). Providing separate power pins provides a way to prevent high speed transient currents in the output stage from bleeding into the sensitive amplifier input and gain stages. To maximize crosstalk isolation, each power supply pin should have its own de-coupling capacitors connected as close to the pin as possible (0.1µF in parallel with 1nF recommended).

The ESD protection circuits use internal diodes from all pins to the V_+ and ground pins. In addition, a dv/dt-triggered clamp is connected between the V_+ and V_- pins, as shown in the Equivalent Circuits 1 through 4 on page 2. The dv/dt triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the maximum rate of rise is not exceeded.

$\overline{EN}$ and Power-Down States

The $\overline{EN}$ pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{EN}$ pin. The power-down state is established within approximately 25ns, if a logic high (>2V) is placed on the $\overline{EN}$ pin. In the power-down state, supply current is reduced significantly by shutting the three amplifiers off. The output presents a relatively high impedance (~2kΩ) to the output pin. Multiplexing several outputs together is possible using the enable/disable function as long as the application can tolerate the limited power-down output impedance.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 40mA. Adequate thermal heat sinking of the parts is also required.

PC Board Layout

The AC performance of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components, such as chip resistors and chip capacitors, is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners. Use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be

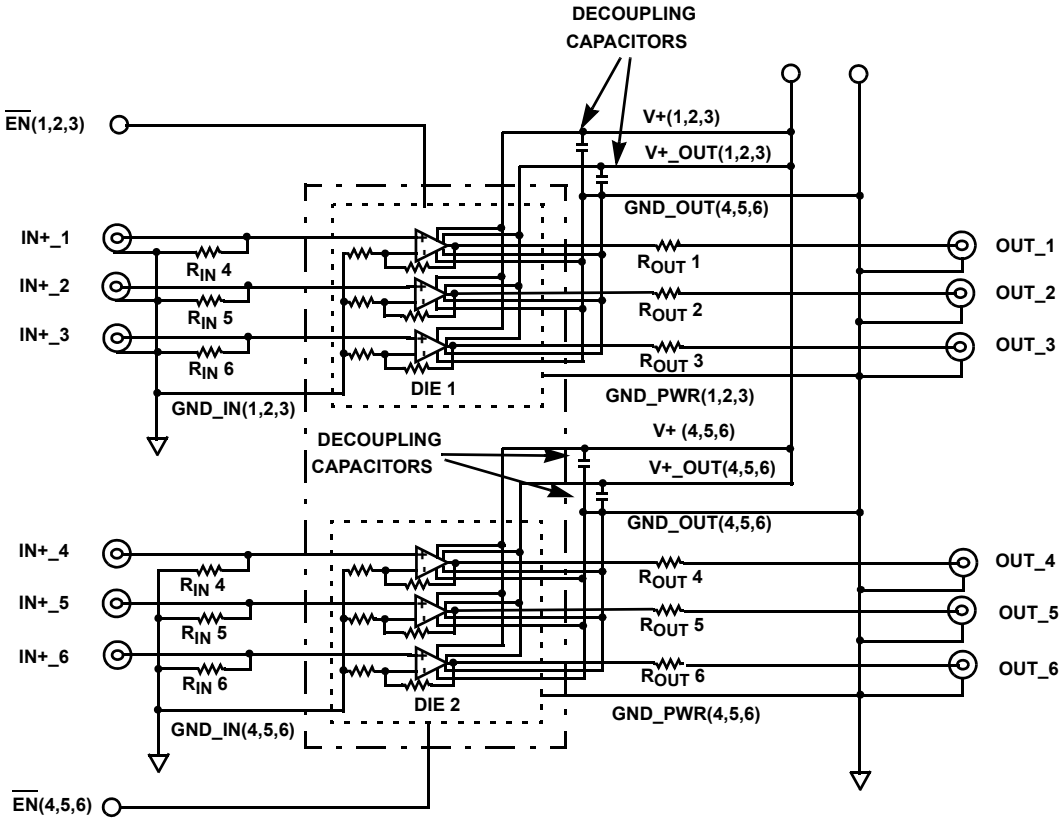


FIGURE 26. BASIC APPLICATION CIRCUIT

degraded for traces greater than one inch, unless controlled impedance (50Ω or 75Ω) strip lines or microstrips are used.

- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing, use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- A minimum of 2 power supply decoupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible. Avoid vias between the capacitor and the device because vias add unwanted inductance. Larger capacitors can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.
- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

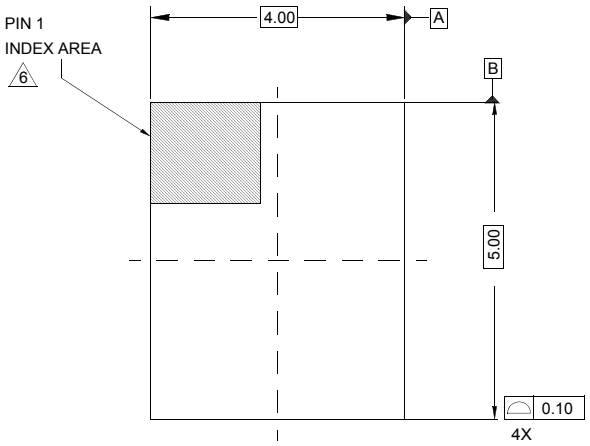
The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to power supply ground through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the power ground pins through the substrate, the thermal pad must be tied to the power supply ground to prevent unwanted current flow through the thermal pad. Maximum AC performance is achieved if the thermal pad has good contact to the IC ground pins. Heat sinking requirements can be satisfied using thermal vias directly beneath the thermal pad to a heat dissipating layer of a square at least 1” on a side.

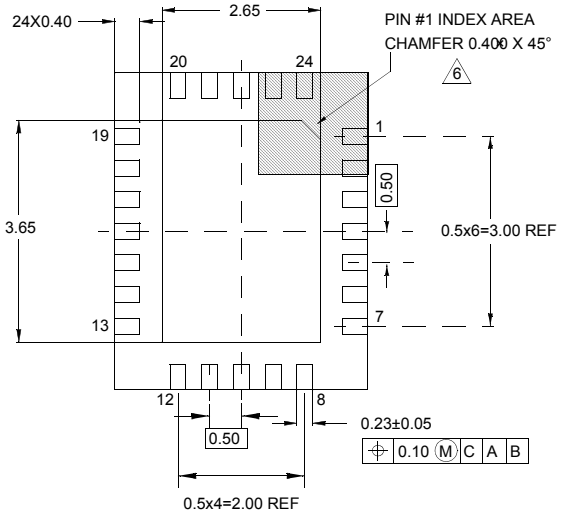
Package Outline Drawing

L24.4x5C

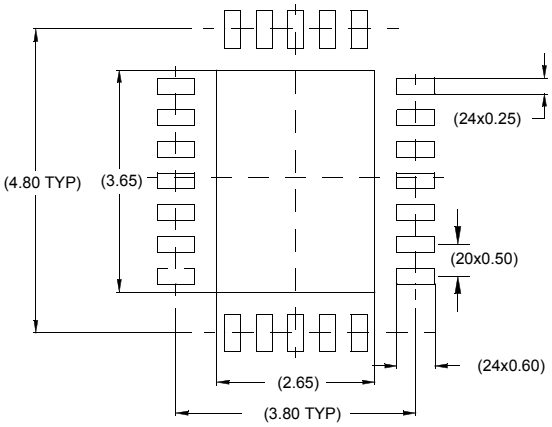
24 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 10/07



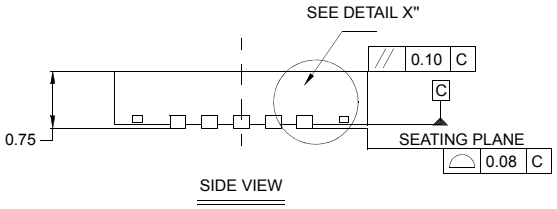
TOP VIEW



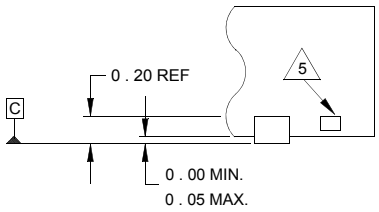
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.28mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.