

ISL32490E, ISL32492E, ISL32493E, ISL32495E, ISL32496E, ISL32498E

±60V Fault Protected, 5V, RS-485/RS-422 Transceivers with ±25V CMR and ESD Protection

FN7786  
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The [ISL32490E](#), [ISL32492E](#), [ISL32493E](#), [ISL32495E](#), [ISL32496E](#), [ISL32498E](#) are fault protected, 5V powered, differential transceivers that exceed the RS-485 and RS-422 standards for balanced communication. The RS-485 transceiver pins (driver outputs and receiver inputs) are fault protected up to ±60V and are protected against ±16.5kV ESD strikes without latch-up. Additionally, the extended Common Mode Range (CMR) allows these transceivers to operate in environments with common mode voltages up to ±25V (>2x the RS-485 requirement), making this fault protected RS-485 family one of the most robust on the market.

Transmitters (Tx) deliver an exceptional 2.5V (typical) differential output voltage into the RS-485 specified 54Ω load. This yields better noise immunity than standard RS-485 ICs, or allows up to six 120Ω terminations in star network topologies.

Receiver (Rx) inputs feature a “full fail-safe” design that ensures a logic high Rx output if Rx inputs are floating, shorted, or on a terminated but undriven (idle) bus. Rx outputs have high drive levels; typically, 15mA at  $V_{OL} = 1V$  (for opto-coupled, isolated applications).

Half duplex (Rx inputs and Tx outputs multiplexed together) and full duplex pinouts are available. Refer to [Table 1 on page 2](#) for key features and configurations by device number.

For fault protected or wide common mode range RS-485 transceivers with cable invert (polarity reversal) pins, refer to the [ISL32483E](#) datasheet.

**Related Literature**

- For a full list of related documents, visit our website
- [ISL32490E](#), [ISL32492E](#), [ISL32493E](#), [ISL32495E](#), [ISL32496E](#), and [ISL32498E](#) product pages

**Features**

- Fault protected RS-485 bus pins . . . . . up to ±60V
- Extended CMR . . . . . ±25V (more than twice the range required for RS-485)
- ±16.5kV HBM ESD protection on RS-485 bus pins
- 1/4 unit load for up to 128 devices on the bus
- High transient overvoltage tolerance. . . . . ±80V
- Full fail-safe (open, short, terminated) RS-485 receivers
- High Rx  $I_{OL}$  for opto-couplers in isolated designs
- Hot plug circuitry; Tx and Rx outputs remain three-state during power-up/power-down
- Choice of RS-485 data rates. . . . . 250kbps to 15Mbps
- Low quiescent supply current. . . . . 2.3mA
- Ultra low shutdown supply current. . . . . 10μA

**Applications**

- Utility meters/automated meter reading systems
- High node count RS-485 systems
- PROFIBUS and RS-485 based field bus networks, and factory automation
- Security camera networks
- Building lighting and environmental control systems
- Industrial/process control networks

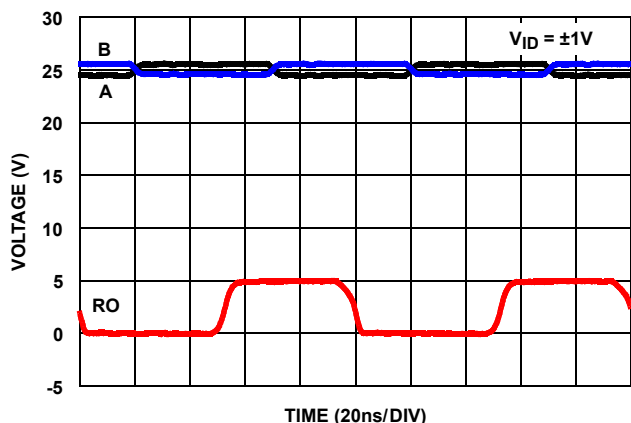


FIGURE 1. EXCEPTIONAL Rx OPERATES AT >15Mbps EVEN WITH A ±25V COMMON MODE VOLTAGE

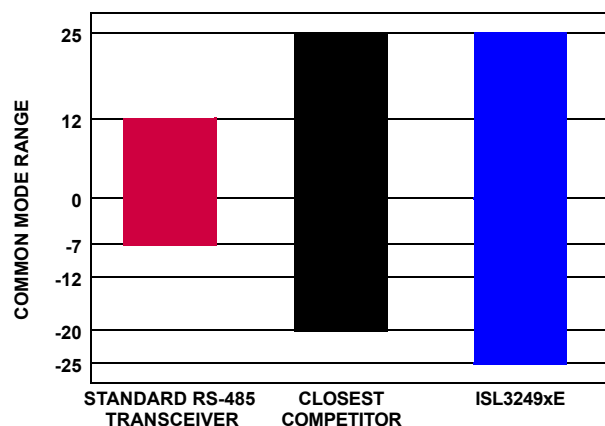


FIGURE 2. ISL3249xE DELIVERS SUPERIOR COMMON MODE RANGE vs STANDARD RS-485 DEVICES

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	HALF/FULL DUPLEX	DATA RATE (Mbps)	SLEW-RATE LIMITED?	EN PINS?	HOT PLUG?	QUIESCENT I <sub>CC</sub> (mA)	LOW POWER SHDN?	PIN COUNT
ISL32490E	Full	0.25	Yes	Yes	Yes	2.3	Yes	10, 14
ISL32492E	Half	0.25	Yes	Yes	Yes	2.3	Yes	8
ISL32493E	Full	1	Yes	Yes	Yes	2.3	Yes	10, 14
ISL32495E	Half	1	Yes	Yes	Yes	2.3	Yes	8
ISL32496E	Full	15	No	Yes	Yes	2.3	Yes	10, 14
ISL32498E	Half	15	No	Yes	Yes	2.3	Yes	8

## Ordering Information

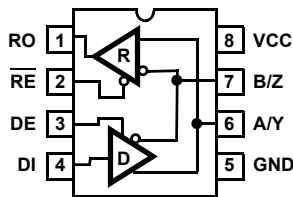
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL32490EIBZ	ISL32490 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32490EIUZ	2490E	-40 to +85	10 Ld MSOP	M10.118
ISL32492EIBZ	32492 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32492EIUZ	2492E	-40 to +85	8 Ld MSOP	M8.118
ISL32493EIBZ	ISL32493 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32493EIUZ	2493E	-40 to +85	10 Ld MSOP	M10.118
ISL32495EIBZ	32495 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32495EIUZ	2495E	-40 to +85	8 Ld MSOP	M8.118
ISL32496EIBZ	ISL32496 EIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL32496EIUZ	2496E	-40 to +85	10 Ld MSOP	M10.118
ISL32498EIBZ	32498 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL32498EIUZ	2498E	-40 to +85	8 Ld MSOP	M8.118

### NOTES:

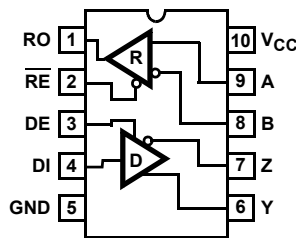
1. Add "-T" suffix for 2.5k unit or "-T7A" suffix for 250 unit tape and reel option. Refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the product information pages for [ISL32490E](#), [ISL32492E](#), [ISL32493E](#), [ISL32495E](#), [ISL32496E](#), [ISL32498E](#). For more information on MSL, refer to [TB363](#).

## Pin Configurations

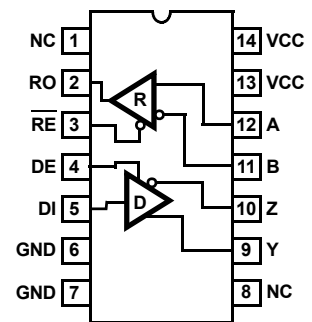
ISL32492E, ISL32495E, ISL32498E  
(8 LD MSOP, 8 LD SOIC)  
TOP VIEW



ISL32490E, ISL32493E, ISL32496E  
(10 LD MSOP)  
TOP VIEW



ISL32490E, ISL32493E, ISL32496E  
(14 LD SOIC)  
TOP VIEW



NOTE: Evaluate creepage and clearance requirements at your maximum fault voltage before using small pitch packages such as MSOP.

## Truth Tables

TRANSMITTING				
INPUTS			OUTPUTS	
RE	DE	DI	Z	Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z (see Note)	High-Z (see Note)

NOTE: Low Power Shutdown Mode (see [Note 11 on page 9](#)).

RECEIVING				
INPUTS				OUTPUT
RE	DE Half Duplex	DE Full Duplex	A-B	RO
0	0	X	$V_{AB} \geq -0.01V$	1
0	0	X	$-0.01V > V_{AB} > -0.2V$	Undetermined
0	0	X	$V_{AB} \leq -0.2V$	0
0	0	X	Inputs Open/Shorted	1
1	0	0	X	High-Z (see Note)
1	1	1	X	High-Z

NOTE: Low Power Shutdown Mode (see [Note 11 on page 9](#)).

## Pin Descriptions

PIN NAME	8 LD PIN #	10 LD PIN #	14 LD PIN #	FUNCTION
RO	1	1	2	Receiver output. If $A-B \geq -10mV$ , RO is high; if $A-B \leq -200mV$ , RO is low; if A and B are unconnected (floating), shorted together, or connected to an undriven, terminated bus, RO is high.
RE	2	2	3	Receiver output enable. RO is enabled when RE is low; RO is high impedance when RE is high. Internally pulled low.
DE	3	3	4	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. Internally pulled high.
DI	4	4	5	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	5	5	6, 7	Ground connection.
A/Y	6	-	-	$\pm 60V$ fault and $\pm 16.5kV$ HBM ESD protected RS-485/RS-422 level, non-inverting receiver input and non-inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
B/Z	7	-	-	$\pm 60V$ fault and $\pm 16.5kV$ HBM ESD protected RS-485/RS-422 level, inverting receiver input and inverting driver output. Pin is an input if DE = 0; pin is an output if DE = 1.
A	-	9	12	$\pm 60V$ fault and $\pm 15kV$ HBM ESD protected RS-485/RS-422 level, non-inverting receiver input.
B	-	8	11	$\pm 60V$ fault and $\pm 15kV$ HBM ESD protected RS-485/RS-422 level, inverting receiver input.
Y	-	6	9	$\pm 60V$ fault and $\pm 15kV$ HBM ESD protected RS-485/RS-422 level, non-inverting driver output.

## Pin Descriptions (Continued)

PIN NAME	8 LD PIN #	10 LD PIN #	14 LD PIN #	FUNCTION
Z	-	7	10	±60V fault and ±15kV HBM ESD protected RS-485/RS-422 level, inverting driver output.
VCC	8	10	13, 14	System power supply input (4.5V to 5.5V).
NC	-	-	1, 8	No internal connection.

## Typical Operating Circuits

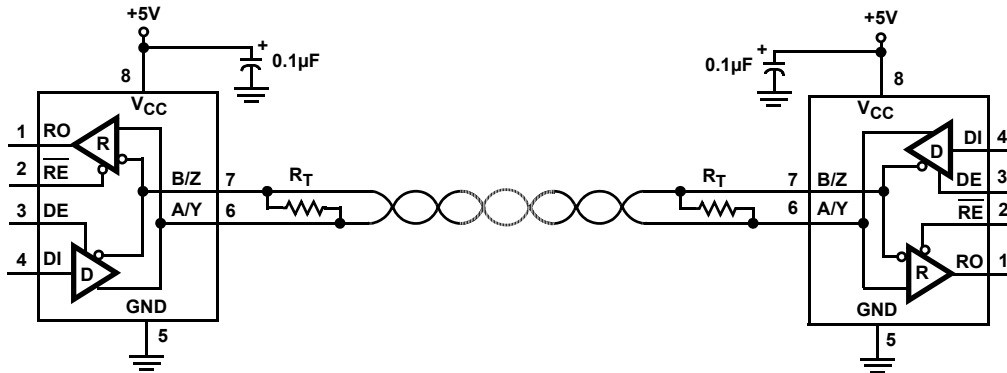


FIGURE 3. ISL32492E, ISL32495E, ISL32498E HALF DUPLEX EXAMPLE

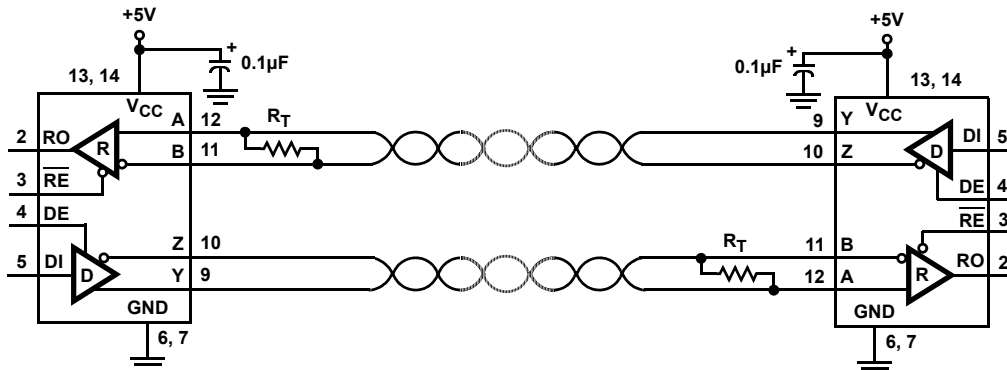


FIGURE 4. ISL32490E, ISL32493E, ISL32496E FULL DUPLEX EXAMPLE (SOIC PIN NUMBERS SHOWN)

## Absolute Maximum Ratings

V <sub>CC</sub> to Ground	7V
Input Voltages	
DI, DE, $\overline{RE}$	-0.3V to (V <sub>CC</sub> + 0.3V)
Input/Output Voltages	
A/Y, B/Z, A, B, Y, Z	±60V
A/Y, B/Z, A, B, Y, Z (Transient Pulse Through 100Ω, (Note 15))	±80V
RO	-0.3V to (V <sub>CC</sub> + 0.3V)
Short Circuit Duration	
Y, Z	Indefinite
ESD Rating	see "ESD PERFORMANCE" on page 6
Latch-up (Tested per JEDEC78, Level 2, Class A)	+125°C

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld MSOP Package (Notes 4, 5)	140	40
8 Ld SOIC Package (Notes 4, 5)	108	47
10 Ld MSOP Package (Notes 4, 5)	135	50
14 Ld SOIC Package (Notes 4, 5)	88	39
Maximum Junction Temperature (Plastic Package)	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Pb-free Reflow Profile	Refer to <a href="#">TB493</a>	

## Recommended Operating Conditions

Supply Voltage (V <sub>CC</sub> )	5V
Temperature Range	-40°C to +85°C
Bus Pin Common Mode Voltage Range	-25V to +25V

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to [TB379](#) for details.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.

**Electrical Specifications** V<sub>CC</sub> = 4.5V to 5.5V; unless otherwise specified. Typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = +25°C (Note 6). **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
<b>DC CHARACTERISTICS</b>							
V <sub>OD1</sub>	Driver Differential V <sub>OUT</sub> (No load)		Full	-	-	V <sub>CC</sub>	V
V <sub>OD2</sub>	Driver Differential V <sub>OUT</sub> (Loaded, <a href="#">Figure 5A</a> )	R <sub>L</sub> = 100Ω (RS-422)	Full	<b>2.4</b>	3.2	-	V
		R <sub>L</sub> = 54Ω (RS-485)	Full	<b>1.5</b>	2.5	V <sub>CC</sub>	V
		R <sub>L</sub> = 54Ω (PROFIBUS, V <sub>CC</sub> ≥ 5V)	Full	<b>2.0</b>	2.5		
		R <sub>L</sub> = 21Ω (Six 120Ω Terminations for Star Configurations, V <sub>CC</sub> ≥ 4.75V)	Full	<b>0.8</b>	1.3	-	V
ΔV <sub>OD</sub>	Change in Magnitude of Driver Differential V <sub>OUT</sub> for Complementary Output States	R <sub>L</sub> = 54Ω or 100Ω ( <a href="#">Figure 5A</a> )	Full	-	-	<b>0.2</b>	V
V <sub>OD3</sub>	Driver Differential V <sub>OUT</sub> with Common Mode Load ( <a href="#">Figure 5B</a> )	R <sub>L</sub> = 60Ω, -7V ≤ V <sub>CM</sub> ≤ 12V	Full	<b>1.5</b>	2.1	V <sub>CC</sub>	V
		R <sub>L</sub> = 60Ω, -25V ≤ V <sub>CM</sub> ≤ 25V (V <sub>CC</sub> ≥ 4.75V)	Full	<b>1.7</b>	2.3		
		R <sub>L</sub> = 21Ω, -15V ≤ V <sub>CM</sub> ≤ 15V (V <sub>CC</sub> ≥ 4.75V)	Full	<b>0.8</b>	1.1	-	V
V <sub>OC</sub>	Driver Common-Mode V <sub>OUT</sub> ( <a href="#">Figure 5</a> )	R <sub>L</sub> = 54Ω or 100Ω	Full	<b>-1</b>	-	<b>3</b>	V
		R <sub>L</sub> = 60Ω or 100Ω, -20V ≤ V <sub>CM</sub> ≤ 20V	Full	<b>-2.5</b>	-	<b>5</b>	V
ΔV <sub>OC</sub>	Change in Magnitude of Driver Common Mode V <sub>OUT</sub> for Complementary Output States	R <sub>L</sub> = 54Ω or 100Ω ( <a href="#">Figure 5A</a> )	Full	-	-	<b>0.2</b>	V
I <sub>OSD</sub>	Driver Short-circuit Current	DE = V <sub>CC</sub> , -25V ≤ V <sub>O</sub> ≤ 25V ( <a href="#">Note 8</a> )	Full	<b>-250</b>	-	<b>250</b>	mA
I <sub>OSD1</sub>		At First Fold-back, 22V ≤ V <sub>O</sub> ≤ -22V	Full	<b>-83</b>	-	<b>83</b>	mA
I <sub>OSD2</sub>		At Second Fold-back, 35V ≤ V <sub>O</sub> ≤ -35V	Full	<b>-13</b>	-	<b>13</b>	mA
V <sub>IH</sub>	Logic Input High Voltage	DE, DI, $\overline{RE}$	Full	<b>2.5</b>	-	-	V
V <sub>IL</sub>	Logic Input Low Voltage	DE, DI, $\overline{RE}$	Full	-	-	<b>0.8</b>	V

**Electrical Specifications**  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6). **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS		TEMP ( $^\circ C$ )	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
$I_{IN1}$	Logic Input Current	DI		Full	<b>-1</b>	-	<b>1</b>	$\mu A$
		DE, $\overline{RE}$		Full	<b>-15</b>	6	<b>15</b>	$\mu A$
$I_{IN2}$	Input/Output Current (A/Y, B/Z)	DE = 0V, $V_{CC} = 0V$ or $5.5V$	$V_{IN} = 12V$	Full	-	110	<b>250</b>	$\mu A$
			$V_{IN} = -7V$	Full	<b>-200</b>	-75	-	$\mu A$
			$V_{IN} = \pm 25V$	Full	<b>-800</b>	$\pm 240$	<b>800</b>	$\mu A$
			$V_{IN} = \pm 60V$ (Note 16)	Full	<b>-6</b>	$\pm 0.5$	<b>6</b>	mA
$I_{IN3}$	Input Current (A, B) (Full Duplex Versions Only)	$V_{CC} = 0V$ or $5.5V$	$V_{IN} = 12V$	Full	-	90	<b>125</b>	$\mu A$
			$V_{IN} = -7V$	Full	<b>-100</b>	-70	-	$\mu A$
			$V_{IN} = \pm 25V$	Full	<b>-500</b>	$\pm 200$	<b>500</b>	$\mu A$
			$V_{IN} = \pm 60V$ (Note 16)	Full	<b>-3</b>	$\pm 0.4$	<b>3</b>	mA
$I_{OZD}$	Output Leakage Current (Y, Z) (Full Duplex Versions Only)	$\overline{RE} = 0V$ , DE = 0V, $V_{CC} = 0V$ or $5.5V$	$V_{IN} = 12V$	Full	-	20	<b>200</b>	$\mu A$
			$V_{IN} = -7V$	Full	<b>-100</b>	-5	-	$\mu A$
			$V_{IN} = \pm 25V$	Full	<b>-500</b>	$\pm 40$	<b>500</b>	$\mu A$
			$V_{IN} = \pm 60V$ (Note 16)	Full	<b>-3</b>	$\pm 0.1$	<b>3</b>	mA
$V_{TH}$	Receiver Differential Threshold Voltage	$-25V \leq V_{CM} \leq 25V$		Full	<b>-200</b>	-100	<b>-10</b>	mV
$\Delta V_{TH}$	Receiver Input Hysteresis	$-25V \leq V_{CM} \leq 25V$		25	-	25	-	mV
$V_{OH}$	Receiver Output High Voltage	$I_O = -2mA$ , $V_{ID} = -10mV$		Full	<b><math>V_{CC} - 0.5</math></b>	4.75	-	V
		$I_O = -8mA$ , $V_{ID} = -10mV$		Full	<b>2.8</b>	4.2	-	V
$V_{OL}$	Receiver Output Low Voltage	$I_O = 6mA$ , $V_{ID} = -200mV$		Full	-	0.27	<b>0.4</b>	V
$I_{OL}$	Receiver Output Low Current	$V_O = 1V$ , $V_{ID} = -200mV$		Full	<b>15</b>	22	-	mA
$I_{OZR}$	Three-state (High Impedance) Receiver Output Current	$0V \leq V_O \leq V_{CC}$		Full	<b>-1</b>	0.01	<b>1</b>	$\mu A$
$I_{OSR}$	Receiver Short-circuit Current	$0V \leq V_O \leq V_{CC}$		Full	<b><math>\pm 12</math></b>	-	<b><math>\pm 110</math></b>	mA
<b>SUPPLY CURRENT</b>								
$I_{CC}$	No Load Supply Current (Note 7)	DE = $V_{CC}$ , $\overline{RE} = 0V$ or $V_{CC}$ , DI = 0V or $V_{CC}$		Full	-	2.3	<b>4.5</b>	mA
$I_{SHDN}$	Shutdown Supply Current	DE = 0V, $\overline{RE} = V_{CC}$ , DI = 0V or $V_{CC}$		Full	-	10	<b>50</b>	$\mu A$
<b>ESD PERFORMANCE</b>								
	RS-485 Pins (A, Y, B, Z, A/Y, B/Z)	Human Body Model, From Bus Pins to GND	Half Duplex	25	-	$\pm 16.5$	-	kV
			Full Duplex	25	-	$\pm 15$	-	kV
	All Pins	Human Body Model, per JEDEC		25	-	$\pm 8$	-	kV
		Machine Model		25	-	$\pm 700$	-	V
<b>DRIVER SWITCHING CHARACTERISTICS (250kbps Versions - ISL32490E, ISL32492E)</b>								
$t_{PLH}$ , $t_{PHL}$	Driver Differential Output Delay	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	320	<b>450</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	-	-	<b>1000</b>	ns
$t_{SKEW}$	Driver Differential Output Skew	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	6	<b>30</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	-	-	<b>50</b>	ns

**Electrical Specifications**  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6). **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ . (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 14)	TYP	MAX (Note 14)	UNITS	
$t_R, t_F$	Driver Differential Rise or Fall Time	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	<b>400</b>	650	<b>1200</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	<b>300</b>	-	<b>1350</b>	ns
$f_{MAX}$	Maximum Data Rate	$C_D = 820pF$ (Figure 8)	Full	<b>0.25</b>	1.5	-	Mbps	
$t_{ZH}$	Driver Enable to Output High	SW = GND (Figure 7), (Note 9)	Full	-	-	<b>1200</b>	ns	
$t_{ZL}$	Driver Enable to Output Low	SW = $V_{CC}$ (Figure 7), (Note 9)	Full	-	-	<b>1200</b>	ns	
$t_{LZ}$	Driver Disable from Output Low	SW = $V_{CC}$ (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{HZ}$	Driver Disable from Output High	SW = GND (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns	
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	SW = GND (Figure 7), (Notes 11, 12)	Full	-	-	<b>2500</b>	ns	
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	SW = $V_{CC}$ (Figure 7), (Notes 11, 12)	Full	-	-	<b>2500</b>	ns	

**DRIVER SWITCHING CHARACTERISTICS (1Mbps Versions - ISL32493E, ISL32495E)**

$t_{PLH}, t_{PHL}$	Driver Differential Output Delay	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	70	<b>125</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	-	-	<b>350</b>	ns
$t_{SKEW}$	Driver Differential Output Skew	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	4.5	<b>15</b>	ns
			$-25V \leq V_{CM} \leq 25V$ (Note 17)	Full	-	-	<b>25</b>	ns
$t_R, t_F$	Driver Differential Rise or Fall Time	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	<b>70</b>	170	<b>300</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	<b>70</b>	-	<b>550</b>	ns
$f_{MAX}$	Maximum Data Rate	$C_D = 820pF$ (Figure 8)	Full	<b>1</b>	4	-	Mbps	
$t_{ZH}$	Driver Enable to Output High	SW = GND (Figure 7), (Note 9)	Full	-	-	<b>350</b>	ns	
$t_{ZL}$	Driver Enable to Output Low	SW = $V_{CC}$ (Figure 7), (Note 9)	Full	-	-	<b>300</b>	ns	
$t_{LZ}$	Driver Disable from Output Low	SW = $V_{CC}$ (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{HZ}$	Driver Disable from Output High	SW = GND (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns	
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	SW = GND (Figure 7), (Notes 11, 12)	Full	-	-	<b>2000</b>	ns	
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	SW = $V_{CC}$ (Figure 7), (Notes 11, 12)	Full	-	-	<b>2000</b>	ns	

**DRIVER SWITCHING CHARACTERISTICS (15Mbps Versions - ISL32496E, ISL32498E)**

$t_{PLH}, t_{PHL}$	Driver Differential Output Delay	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	21	<b>45</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	-	-	<b>80</b>	ns
$t_{SKEW}$	Driver Differential Output Skew	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	-	3	<b>6</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	-	-	<b>7</b>	ns

**Electrical Specifications**  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6). **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ . (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 14)	TYP	MAX (Note 14)	UNITS	
$t_R, t_F$	Driver Differential Rise or Fall Time	$R_D = 54\Omega$ , $C_D = 50pF$ (Figure 6)	No CM Load	Full	<b>5</b>	17	<b>30</b>	ns
			$-25V \leq V_{CM} \leq 25V$	Full	<b>5</b>	-	<b>30</b>	ns
$f_{MAX}$	Maximum Data Rate	$C_D = 470pF$ (Figure 8)	Full	<b>15</b>	25	-	Mbps	
$t_{ZH}$	Driver Enable to Output High	$SW = GND$ (Figure 7), (Note 9)	Full	-	-	<b>100</b>	ns	
$t_{ZL}$	Driver Enable to Output Low	$SW = V_{CC}$ (Figure 7), (Note 9)	Full	-	-	<b>100</b>	ns	
$t_{LZ}$	Driver Disable from Output Low	$SW = V_{CC}$ (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{HZ}$	Driver Disable from Output High	$SW = GND$ (Figure 7)	Full	-	-	<b>120</b>	ns	
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns	
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	$SW = GND$ (Figure 7), (Notes 11, 12)	Full	-	-	<b>2000</b>	ns	
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	$SW = V_{CC}$ (Figure 7), (Notes 11, 12)	Full	-	-	<b>2000</b>	ns	

**RECEIVER SWITCHING CHARACTERISTICS (250kbps Versions - ISL32490E, ISL32492E)**

$f_{MAX}$	Maximum Data Rate	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	<b>0.25</b>	5	-	Mbps
$t_{PLH}, t_{PHL}$	Receiver Input to Output Delay	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	-	200	<b>280</b>	ns
$t_{SKD}$	Receiver Skew   $t_{PLH} - t_{PHL}$	(Figure 9)	Full	-	4	<b>10</b>	ns
$t_{ZL}$	Receiver Enable to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = V_{CC}$ (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{ZH}$	Receiver Enable to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = GND$ (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{LZ}$	Receiver Disable from Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = V_{CC}$ (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{HZ}$	Receiver Disable from Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = GND$ (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = GND$ (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = V_{CC}$ (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns

**RECEIVER SWITCHING CHARACTERISTICS (1Mbps Versions - ISL32493E, ISL32495E)**

$f_{MAX}$	Maximum Data Rate	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	<b>1</b>	15	-	Mbps
$t_{PLH}, t_{PHL}$	Receiver Input to Output Delay	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	-	90	<b>150</b>	ns
$t_{SKD}$	Receiver Skew   $t_{PLH} - t_{PHL}$	(Figure 9)	Full	-	4	<b>10</b>	ns
$t_{ZL}$	Receiver Enable to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = V_{CC}$ (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{ZH}$	Receiver Enable to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = GND$ (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{LZ}$	Receiver Disable from Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = V_{CC}$ (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{HZ}$	Receiver Disable from Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , $SW = GND$ (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns



**Electrical Specifications**  $V_{CC} = 4.5V$  to  $5.5V$ ; unless otherwise specified. Typical values are at  $V_{CC} = 5V$ ,  $T_A = +25^\circ C$  (Note 6). **Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
$t_{ZH}(SHDN)$	Receiver Enable from Shutdown to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns
$t_{ZL}(SHDN)$	Receiver Enable from Shutdown to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns
<b>RECEIVER SWITCHING CHARACTERISTICS (15Mbps Versions - ISL32496E, ISL32498E)</b>							
$f_{MAX}$	Maximum Data Rate	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	<b>15</b>	25	-	Mbps
$t_{PLH}$ , $t_{PHL}$	Receiver Input to Output Delay	$-25V \leq V_{CM} \leq 25V$ (Figure 9)	Full	-	35	<b>70</b>	ns
$t_{SKD}$	Receiver Skew   $t_{PLH} - t_{PHL}$	(Figure 9)	Full	-	4	<b>10</b>	ns
$t_{ZL}$	Receiver Enable to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{ZH}$	Receiver Enable to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 10), (Note 10)	Full	-	-	<b>50</b>	ns
$t_{LZ}$	Receiver Disable from Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{HZ}$	Receiver Disable from Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 10)	Full	-	-	<b>50</b>	ns
$t_{SHDN}$	Time to Shutdown	(Note 11)	Full	<b>60</b>	160	<b>600</b>	ns
$t_{ZH}(SHDN)$	Receiver Enable from Shutdown to Output High	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = GND (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns
$t_{ZL}(SHDN)$	Receiver Enable from Shutdown to Output Low	$R_L = 1k\Omega$ , $C_L = 15pF$ , SW = $V_{CC}$ (Figure 10), (Notes 11, 13)	Full	-	-	<b>2000</b>	ns

## NOTES:

- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Supply current specification is valid for loaded drivers when  $DE = 0V$ .
- Applies to peak current. See "Typical Performance Curves" beginning on page 14 for more information.
- Keep  $\overline{RE} = 0$  to prevent the device from entering SHDN.
- The  $\overline{RE}$  signal high time must be short enough (typically  $<100ns$ ) to prevent the device from entering SHDN.
- Transceivers are put into shutdown by bringing  $\overline{RE}$  high and  $DE$  low. If the inputs are in this state for fewer than  $60ns$ , the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least  $600ns$ , the parts are guaranteed to enter shutdown. See "Low Power Shutdown Mode" on page 13.
- Keep  $\overline{RE} = V_{CC}$ , and set the  $DE$  signal low time  $>600ns$  to ensure that the device enters SHDN.
- Set the  $\overline{RE}$  signal high time  $>600ns$  to ensure that the device enters SHDN.
- Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- Tested according to TIA/EIA-485-A, Section 4.2.6 ( $\pm 80V$  for  $15\mu s$  at a 1% duty cycle).
- See "Caution" statement below the "Latch-up (Tested per JESD78, Level 2, Class A)  $+125^\circ C$ " on page 5.
- This parameter is not production tested.

## Test Circuits and Waveforms

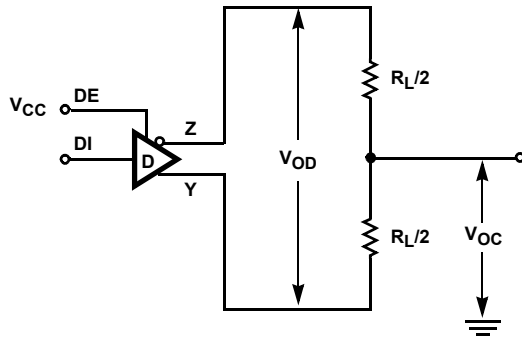


FIGURE 5A.  $V_{OD}$  AND  $V_{OC}$

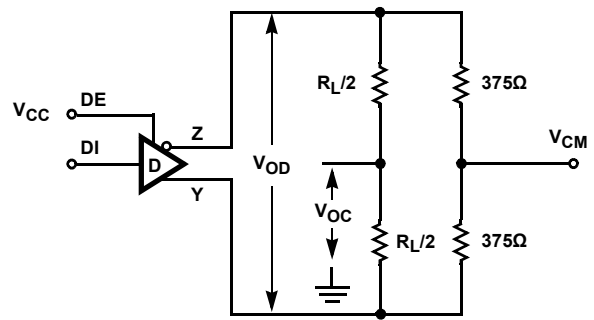


FIGURE 5B.  $V_{OD}$  AND  $V_{OC}$  WITH COMMON MODE LOAD

FIGURE 5. DC DRIVER TEST CIRCUITS

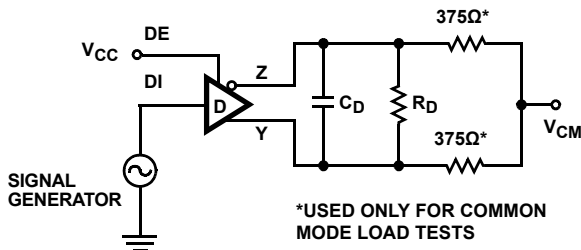


FIGURE 6A. TEST CIRCUIT

FIGURE 6. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES

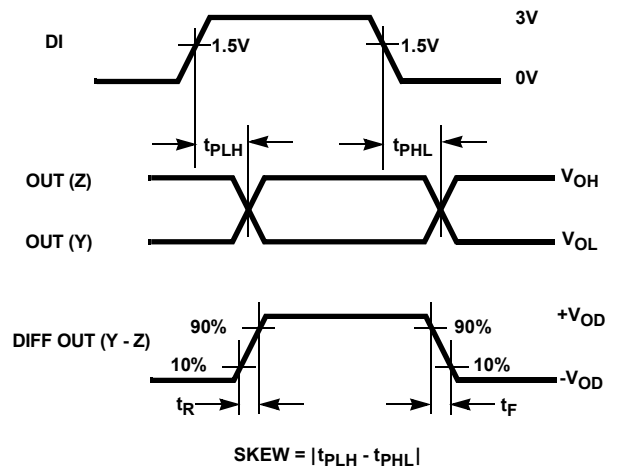


FIGURE 6B. MEASUREMENT POINTS

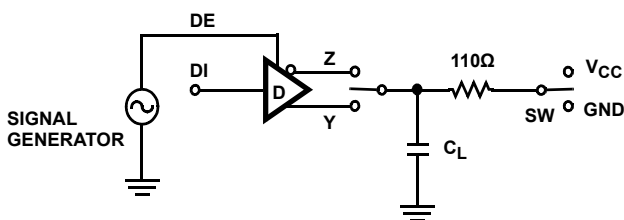


FIGURE 7A. TEST CIRCUIT

FIGURE 7. DRIVER ENABLE AND DISABLE TIMES

PARAMETER	OUTPUT	$\overline{RE}$	DI	SW	$C_L$ (pF)
$t_{HZ}$	Y/Z	X	1/0	GND	50
$t_{LZ}$	Y/Z	X	0/1	$V_{CC}$	50
$t_{ZH}$	Y/Z	0 (Note 9)	1/0	GND	100
$t_{ZL}$	Y/Z	0 (Note 9)	0/1	$V_{CC}$	100
$t_{ZH(SHDN)}$	Y/Z	1 (Note 12)	1/0	GND	100
$t_{ZL(SHDN)}$	Y/Z	1 (Note 12)	0/1	$V_{CC}$	100

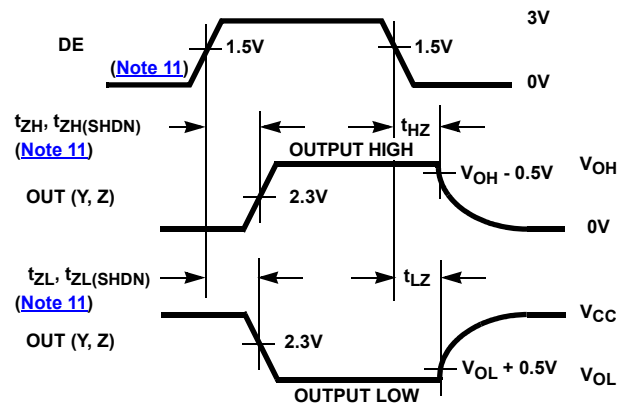


FIGURE 7B. MEASUREMENT POINTS

## Test Circuits and Waveforms (Continued)

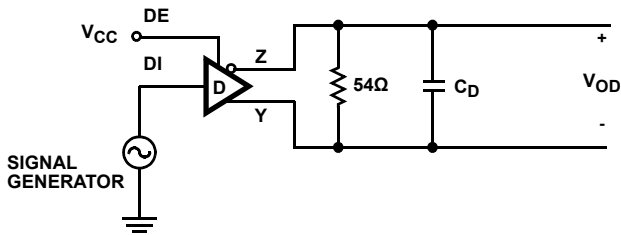


FIGURE 8A. TEST CIRCUIT

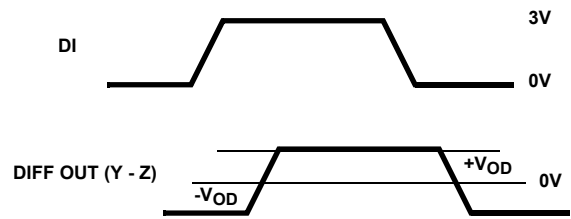


FIGURE 8B. MEASUREMENT POINTS

FIGURE 8. DRIVER DATA RATE

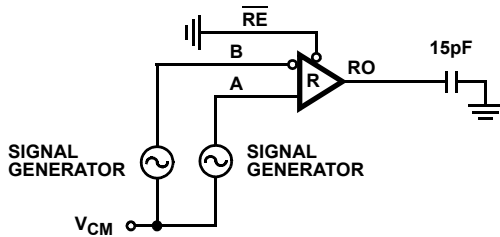


FIGURE 9A. TEST CIRCUIT

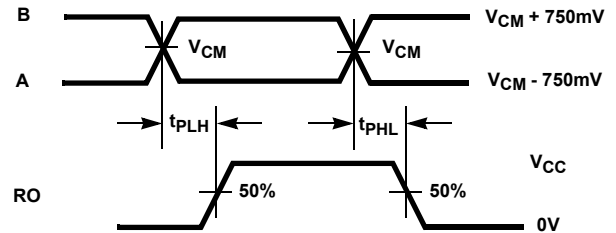
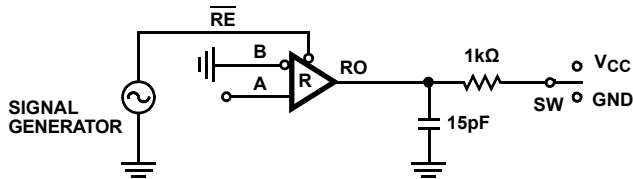


FIGURE 9B. MEASUREMENT POINTS

FIGURE 9. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	DE	A	SW
$t_{HZ}$	0	+1.5V	GND
$t_{LZ}$	0	-1.5V	$V_{CC}$
$t_{ZH}$ (Note 10)	0	+1.5V	GND
$t_{ZL}$ (Note 10)	0	-1.5V	$V_{CC}$
$t_{ZH(SHDN)}$ (Note 13)	0	+1.5V	GND
$t_{ZL(SHDN)}$ (Note 13)	0	-1.5V	$V_{CC}$

FIGURE 10A. TEST CIRCUIT

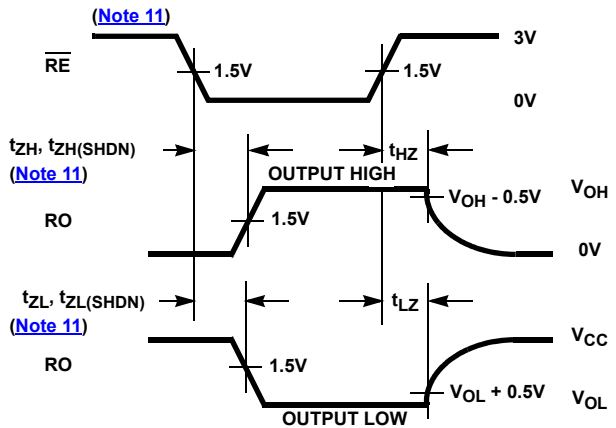


FIGURE 10B. MEASUREMENT POINTS

FIGURE 10. RECEIVER ENABLE AND DISABLE TIMES

## Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards used for long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one-unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one-unit load devices (any combination of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that

drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended Common Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000 feet; thus, the wide CMR is necessary to handle ground potential differences as well as voltages induced in the cable by external fields.

The ISL3249xE is a family of ruggedized RS-485 transceivers that improves on the RS-485 basic requirements and increases

system reliability. The CMR increases to  $\pm 25V$ , while the RS-485 bus pins (receiver inputs and driver outputs) include fault protection against voltages and transients up to  $\pm 60V$ . Additionally, larger than required differential output voltages ( $V_{OD}$ ) increase noise immunity, while the  $\pm 16.5kV$  built-in ESD protection complements the fault protection.

## Receiver (Rx) Features

These devices utilize a differential input receiver for maximum noise immunity and CMR. Input sensitivity is greater than  $\pm 200mV$ , as required by the RS-422 and RS-485 specifications.

The receiver input (load) current surpasses the RS-422 specification of 3mA and is four times lower than the RS-485 "Unit Load (UL)" requirement of 1mA maximum. Thus, these products are known as "one-quarter UL" transceivers, and there can be up to 128 of these devices on a network while still complying with the RS-485 loading specification.

The Rx functions with common mode voltages as great as  $\pm 25V$ , making them ideal for industrial or long networks where induced voltages are a realistic concern.

All the receivers include a "full fail-safe" function that guarantees a high-level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (that is, an idle bus).

Rx outputs feature high drive levels (typically 22mA at  $V_{OL} = 1V$ ) to ease the design of optically coupled isolated interfaces.

Receivers easily meet the data rates supported by the corresponding driver, and all receiver outputs are three-statable using the active low  $\overline{RE}$  input.

The Rx in the 250kbps and 1Mbps versions includes noise filtering circuitry to reject high-frequency signals. The 1Mbps version typically rejects pulses narrower than 50ns (equivalent to 20Mbps), while the 250kbps Rx rejects pulses below 150ns (6.7Mbps).

## Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 1.5V across a  $54\Omega$  load (RS-485) and at least 2.4V across a  $100\Omega$  load (RS-422). The drivers feature low propagation delay skew to maximize bit width and minimize EMI, and all drivers are three-statable using the active high DE input.

The 250kbps and 1Mbps driver outputs are slew rate limited to minimize EMI and to minimize reflections in unterminated or improperly terminated networks. The ISL32496E and ISL32498E driver outputs are not limited; thus, faster output transition times allow data rates of at least 15Mbps.

## High Overvoltage (Fault) Protection Increases Ruggedness

Note: The available smaller pitch package (MSOP) may not meet the creepage and clearance (C&C) requirements for  $\pm 60V$  levels. The user is advised to determine his C&C requirements before selecting a package type.

The  $\pm 60V$  fault protection (referenced to the IC GND) on the RS-485 pins makes these transceivers some of the most rugged

on the market. This level of protection makes the ISL3249xE perfect for applications where power (such as 24V and 48V supplies) must be routed in the conduit with the data lines, or for outdoor applications where large transients are likely to occur. When power is routed with the data lines, even a momentary short between the supply and data lines will destroy an unprotected device. The  $\pm 60V$  fault levels of this family are at least five times higher than the levels specified for standard RS-485 ICs. The ISL3249xE protection is active whether the Tx is enabled or disabled, and even if the IC is powered down.

If transients or voltages (including overshoots and ringing) greater than  $\pm 60V$  are possible, then additional external protection is required.

## Widest Common Mode Voltage (CMV) Tolerance Improves Operating Range

RS-485 networks operating in industrial complexes or over long distances are susceptible to large CMV variations. Either of these operating environments can suffer from large node-to-node ground potential differences or CMV pickup from external electromagnetic sources, and devices with only the minimum required +12V to -7V CMR can malfunction. The ISL3249xE's extended  $\pm 25V$  CMR is the widest available, allowing operation in environments that would overwhelm lesser transceivers. Additionally, the Rx will not phase invert (erroneously change state), even with CMVs of  $\pm 40V$  or differential voltages as large as 40V.

## High $V_{OD}$ Improves Noise Immunity and Flexibility

The ISL3249xE driver design delivers larger differential output voltages ( $V_{OD}$ ) than the RS-485 standard requires or than most RS-485 transmitters can deliver. The typical  $\pm 2.5V$   $V_{OD}$  provides more noise immunity than networks built using many other transceivers.

Another advantage of the large  $V_{OD}$  is the ability to drive more than two bus terminations, which allows for utilizing the ISL3249xE in "star" and other multi-terminated, nonstandard network topologies. [Figure 12 on page 14](#) details the transmitter's  $V_{OD}$  vs  $I_{OUT}$  characteristic and includes load lines for four ( $30\Omega$ ) and six ( $20\Omega$ )  $120\Omega$  terminations. [Figure 12](#) shows that the driver typically delivers  $\pm 1.3V$  into six terminations, and the "[Electrical Specifications](#)" on [page 5](#) guarantees a  $V_{OD}$  of  $\pm 0.8V$  at  $21\Omega$  over the full temperature range. The RS-485 standard requires a minimum 1.5V  $V_{OD}$  into two terminations, but the ISL3249xE devices deliver RS-485 voltage levels with two to three times the number of terminations.

## Hot Plug Function

When a piece of equipment powers up, a period of time occurs during which the processor or ASIC driving the RS-485 control lines (DE,  $\overline{RE}$ ) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3249xE devices incorporate a "hot plug" function. Circuitry monitoring  $V_{CC}$  ensures that during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and  $\overline{RE}$ , if  $V_{CC}$  is less

than  $\approx 3.5\text{V}$ . This allows the processor/ASIC to stabilize and drive the RS-485 control lines to the proper states. Figure 11 illustrates the power-up and power-down performance of the ISL3249xE compared to an RS-485 IC without the hot plug feature.

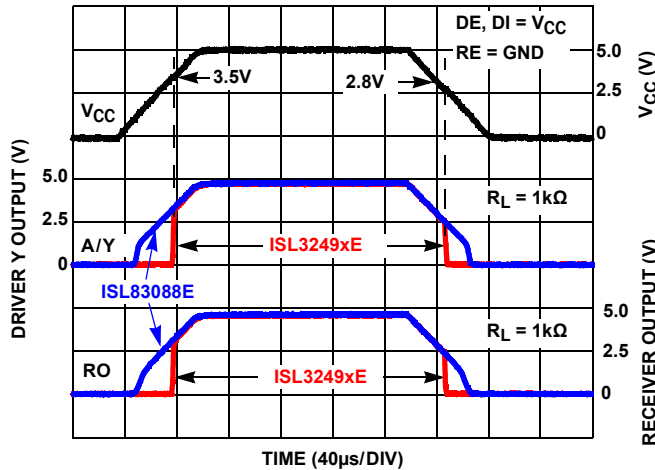


FIGURE 11. HOT PLUG PERFORMANCE (ISL3249xE) vs ISL83088E WITHOUT HOT PLUG CIRCUITRY

## ESD Protection

All pins on these devices include Class 3 ( $>8\text{kV}$ ) Human Body Model (HBM) ESD protection structures that can survive ESD events commonly seen during manufacturing. Even so, the RS-485 pins (driver outputs and receiver inputs) incorporate more advanced structures, allowing them to survive ESD events in excess of  $\pm 16.5\text{kV}$  HBM ( $\pm 15\text{kV}$  for the full-duplex versions). The RS-485 pins are particularly vulnerable to ESD strikes because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins or connecting a cable can cause an ESD event that can destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without interfering with the exceptional  $\pm 25\text{V}$  CMR. This built-in ESD protection minimizes the need for board-level protection structures (for example, transient suppression diodes) and the associated, undesirable capacitive load they present.

## Data Rate, Cables, and Terminations

RS-485 and RS-422 are intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. Devices operating at 15Mbps may be used at lengths up to 150ft (46m), but the distance can be increased to 328ft (100m) by operating at 10Mbps. The 1Mbps versions of this device can operate at full data rates with lengths up to 800ft (244m). Jitter is the limiting parameter at these faster data rates, so employing encoded data streams (e.g., Manchester coded or Return-to-Zero) can allow increased transmission distances. The 250 kbps versions of this device can operate at 115kbps or less at the full 4000ft (1220m) distance, or at 250kbps for lengths up to 3000ft (915m). DC cable attenuation is the limiting parameter, so using better quality cables (such as 22 AWG) may allow increased transmission distance.

Twisted pair is the cable of choice for RS-485/RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

Proper termination is imperative to minimize reflections when using the 15Mbps devices. Short networks using the 250kbps versions need not be terminated; however, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point or point-to-multipoint (single driver on bus, such as RS-422) networks, the main cable should be terminated in its characteristic impedance (typically  $120\Omega$ ) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

## Built-in Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst-case bus contentions undamaged. These transceivers meet this requirement using driver output short circuit current limits and on-chip thermal shutdown circuitry.

The driver output stages incorporate a double foldback, short circuit current limiting scheme, which ensures that the output current never exceeds the RS-485 specification, even at the common mode and fault condition voltage range extremes. The first foldback current level ( $\approx 70\text{mA}$ ) is set to ensure that the driver never folds back when driving loads with CMVs up to  $\pm 25\text{V}$ . The very low second foldback current setting ( $\approx 9\text{mA}$ ) minimizes power dissipation if the Tx is enabled when a fault occurs.

In the event of a major short circuit condition, devices also use a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically re-enable after the die temperature drops about  $+15^\circ\text{C}$ . If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

## Low Power Shutdown Mode

These BiCMOS transceivers all use a fraction of the power required by competitive devices, but they also include a shutdown feature that reduces the already low quiescent  $I_{CC}$  to a  $10\mu\text{A}$  trickle. These devices enter shutdown whenever the receiver and driver are *simultaneously* disabled ( $\overline{RE} = V_{CC}$  and  $DE = \text{GND}$ ) for a period of at least 600ns. Disabling both the driver and the receiver for fewer than 60ns guarantees that the transceiver will not enter shutdown.

Receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 9, 10, 11, 12 and 13 at the end of the "Electrical Specifications" table on page 9 for more information.

**Typical Performance Curves**  $V_{CC} = 5V, T_A = +25^\circ C$ ; unless otherwise specified.

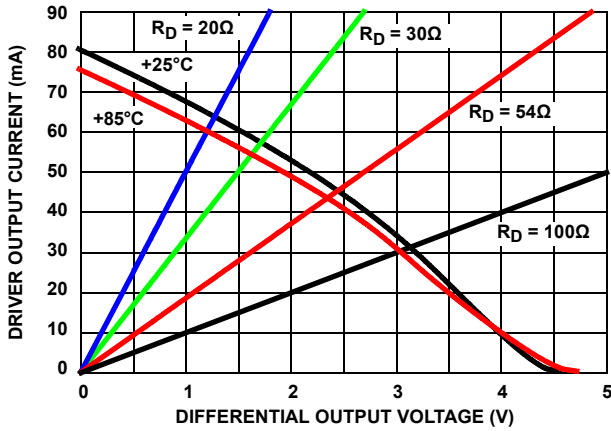


FIGURE 12. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

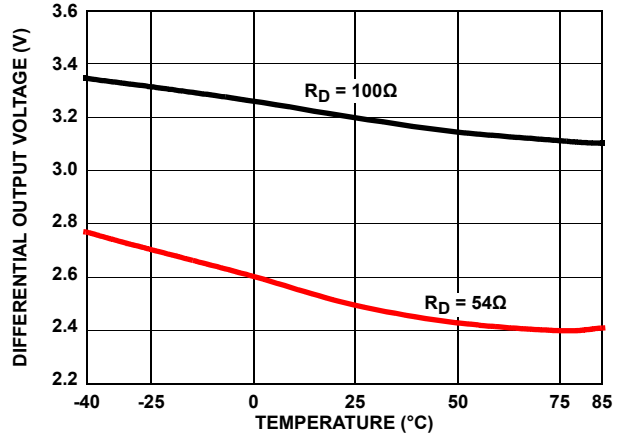


FIGURE 13. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

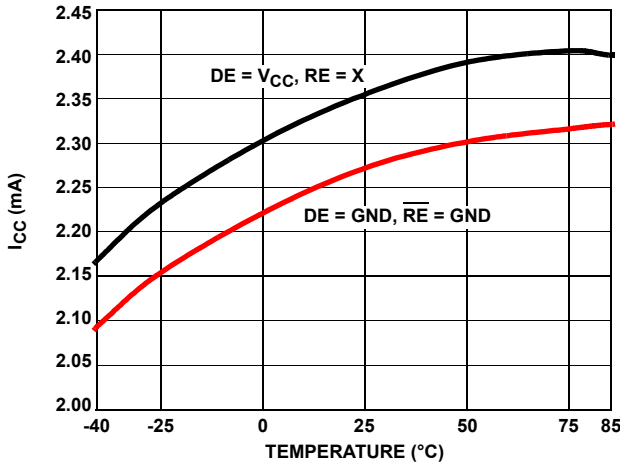


FIGURE 14. SUPPLY CURRENT vs TEMPERATURE

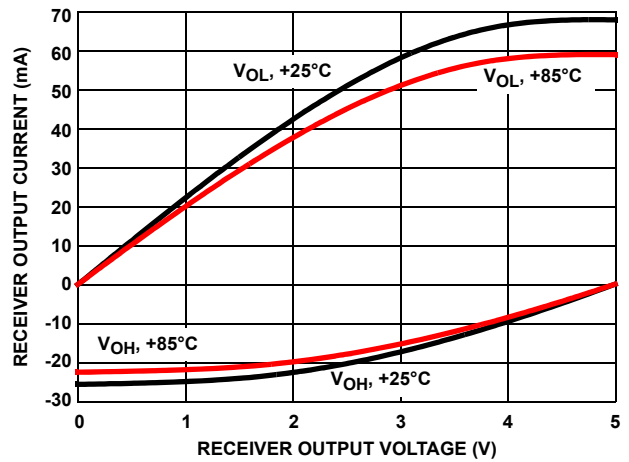


FIGURE 15. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

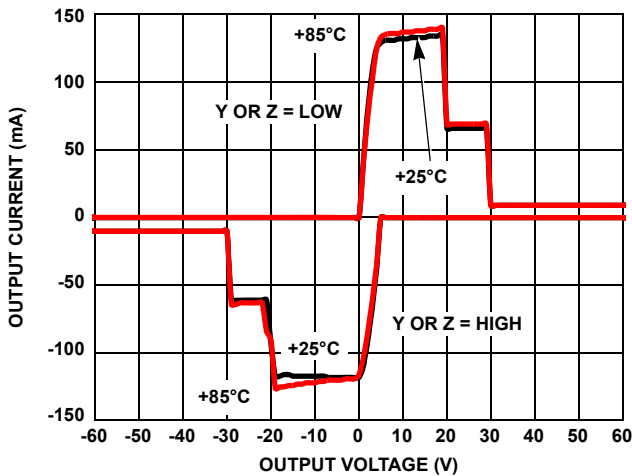


FIGURE 16. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

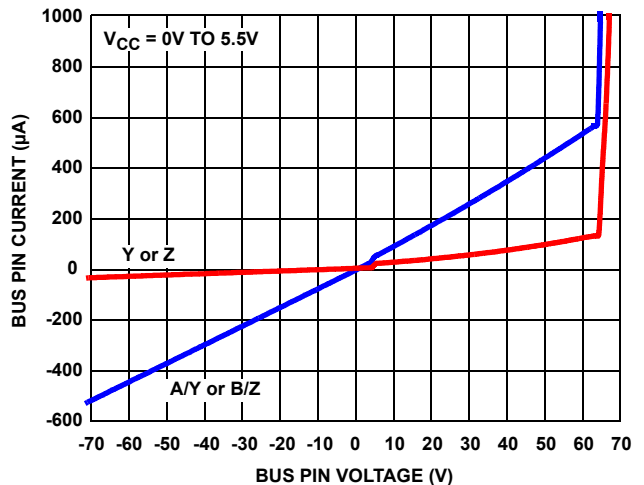


FIGURE 17. BUS PIN CURRENT vs BUS PIN VOLTAGE

**Typical Performance Curves**  $V_{CC} = 5V, T_A = +25^\circ C$ ; unless otherwise specified. (Continued)

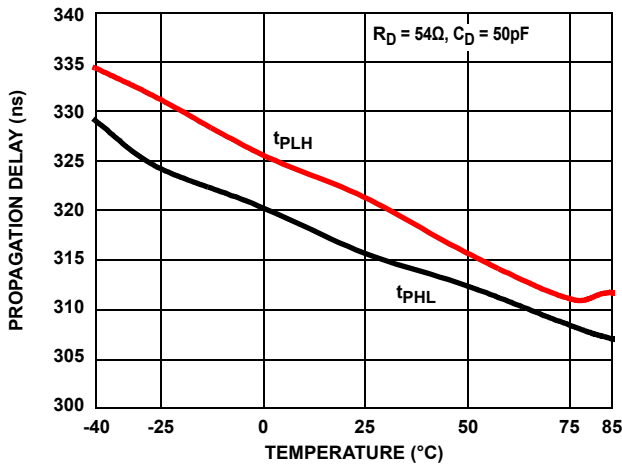


FIGURE 18. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32490E, ISL32492E)

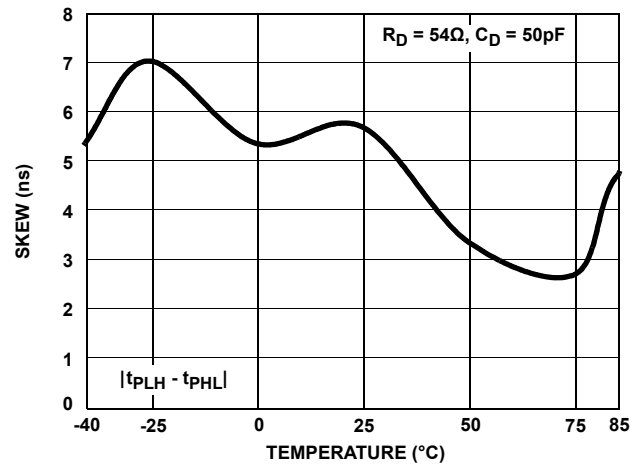


FIGURE 19. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32490E, ISL32492E)

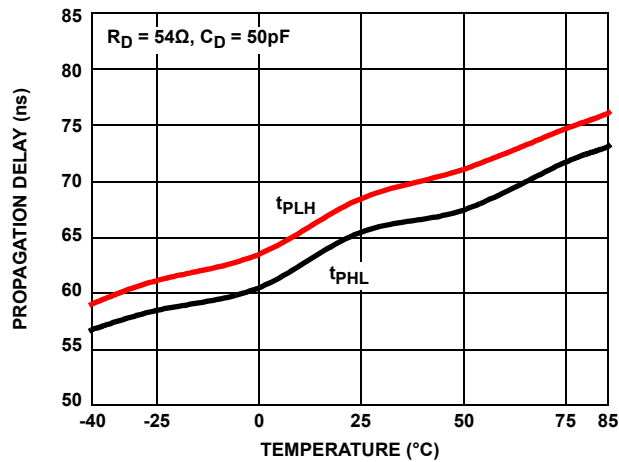


FIGURE 20. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32493E, ISL32495E)

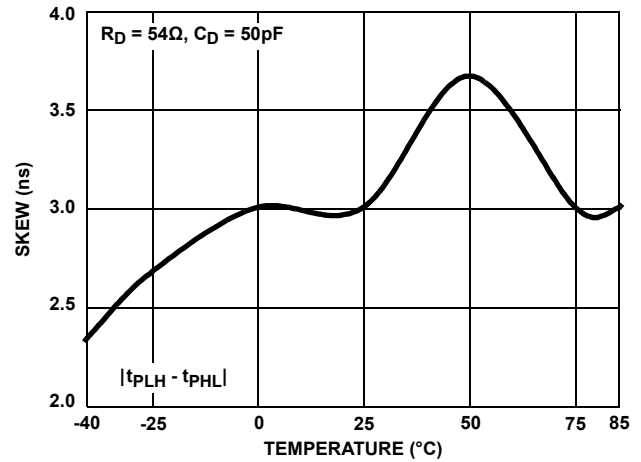


FIGURE 21. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32493E, ISL32495E)

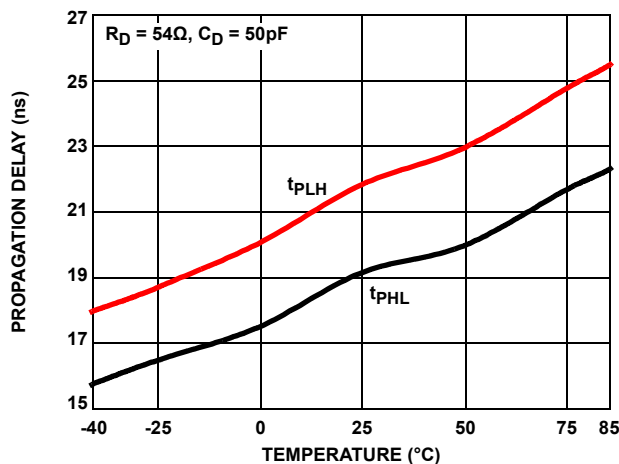


FIGURE 22. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE (ISL32496E, ISL32498E)

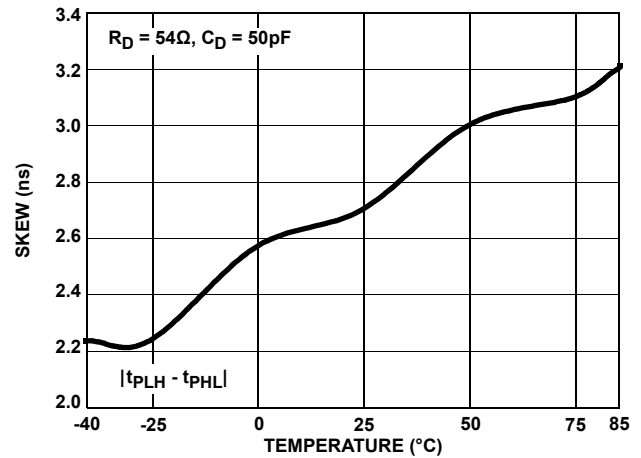


FIGURE 23. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE (ISL32496E, ISL32498E)

**Typical Performance Curves**  $V_{CC} = 5V, T_A = +25^\circ C$ ; unless otherwise specified. (Continued)

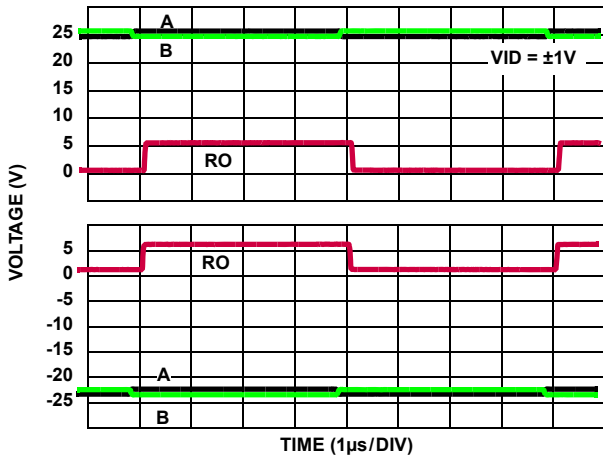


FIGURE 24. RECEIVER PERFORMANCE WITH  $\pm 25V$  CMV (ISL32490E, ISL32492E)

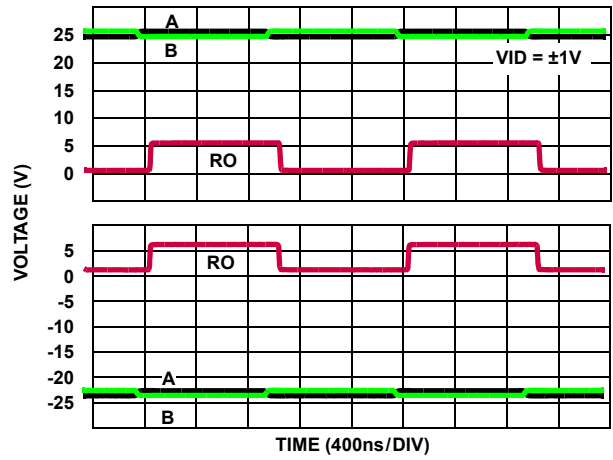


FIGURE 25. RECEIVER PERFORMANCE WITH  $\pm 25V$  CMV (ISL32493E, ISL32495E)

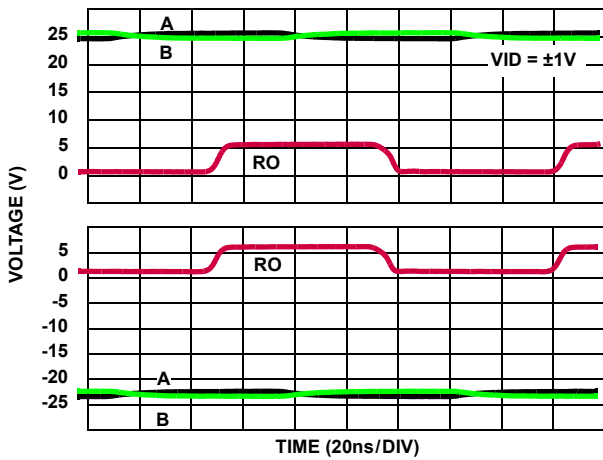


FIGURE 26. RECEIVER PERFORMANCE WITH  $\pm 25V$  CMV (ISL32496E, ISL32498E)

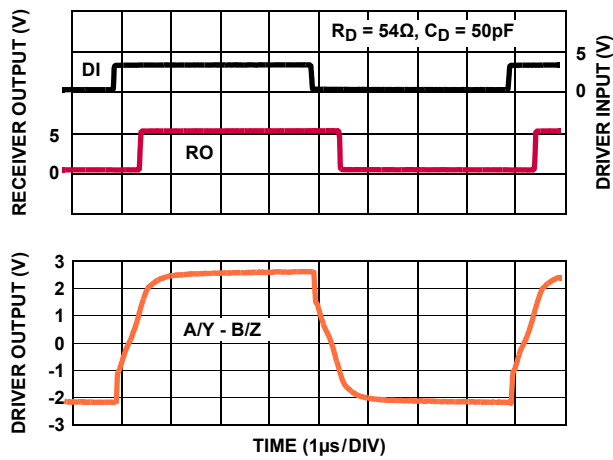


FIGURE 27. DRIVER AND RECEIVER WAVEFORMS (ISL32490E, ISL32492E)

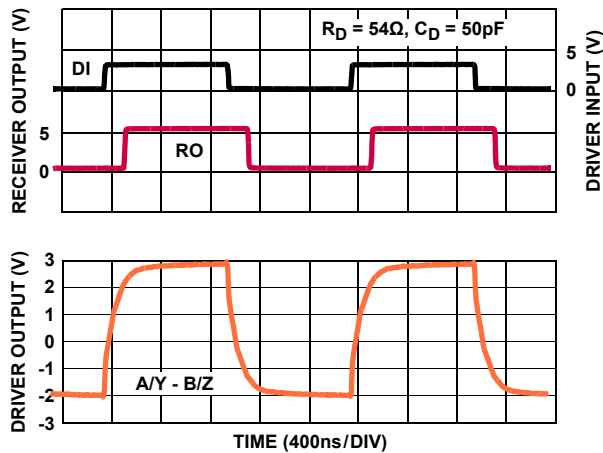


FIGURE 28. DRIVER AND RECEIVER WAVEFORMS (ISL32493E, ISL32495E)

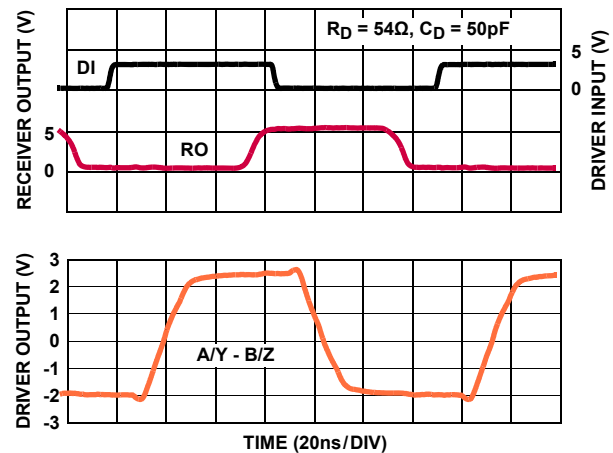


FIGURE 29. DRIVER AND RECEIVER WAVEFORMS (ISL32496E, ISL32498E)



## Die Characteristics

### SUBSTRATE POTENTIAL (POWERED UP):

GND

### PROCESS:

Si Gate BiCMOS

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 18, 2017	FN7765.5	Added Related Literature section. Updated Receiving Truth Table on page 3. Applied Intersil A Renesas Company template.
Apr 20, 2015	FN7786.4	DRIVER SWITCHING CHARACTERISTICS (250kbps Versions; ISL32490E, ISL32492E) Changed MAX limit from "1200" to "1350" in "Driver Differential Rise or Fall Time" on page 7 that has $-25V \leq V_{CM} \leq 25V$ for test condition. DRIVER SWITCHING CHARACTERISTICS (1Mbps Versions; ISL32493E, ISL32495E) Changed MAX limit from "400" to "550" in "Driver Differential Rise or Fall Time" on page 7 that has $-25V \leq V_{CM} \leq 25V$ for test condition.
Oct 14, 2014	FN7786.3	On page 7, added "Note 17" reference to the Driver Differential Output Test condition. On page 9, added Note 17, "This parameter is not production tested." On page 20 replaced M10.118 POD with latest revision.
Mar 7, 2012	FN7786.2	Updated Figure 17 on page 14 to show Pos breakdown between 60V and 70V. Updated Theta JA in "Thermal Information" on page 5 for 8 Ld SOIC from 116 to 108. Updated Package Outline Drawing on page 21. Changed Note 1 "1982" to "1994".
Nov 11, 2011	FN7786.1	Added 10 to "Pin Count" for ISL32490E, ISL32493E, ISL32496E in the Summary of Features table. Added 10 Ld MSOP option for ISL32490E, ISL32493E, ISL32496E in the "Ordering Information" table. Added 10 Ld MSOP pinout to "Pin Configurations" for ISL32490E, ISL32493E, ISL32496E. Added 10 Ld Pin # column in the "Pin Description" table. Added "(SOIC pin numbers shown)" in the "Typical Operating Circuits". Added 10 Ld MSOP information in the "Thermal Resistance" section. Added 10 Ld MSOP package outline drawing. M8.118 on page 19- Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36" M8.15 on page 22- In Typical Recommended Land Pattern, changed the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205)
Jan 18, 2011	FN7786.0	Initial release

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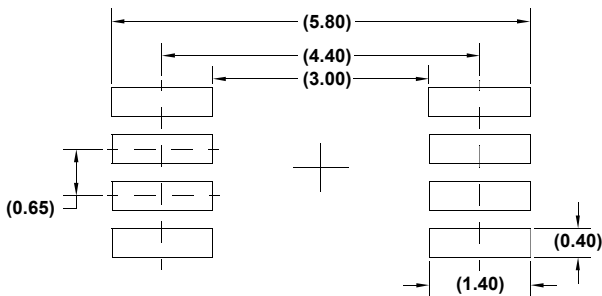
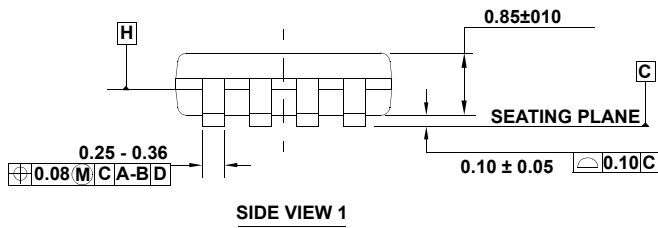
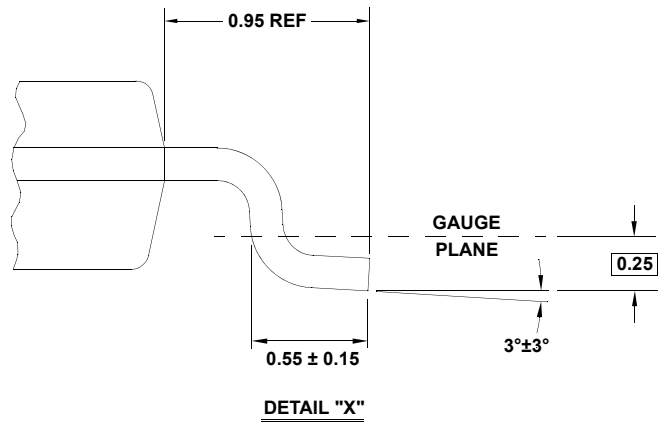
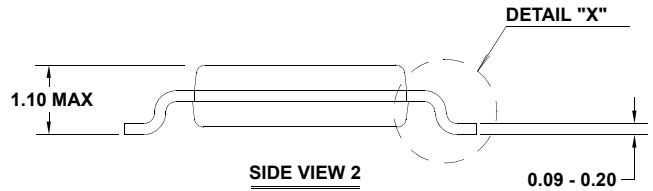
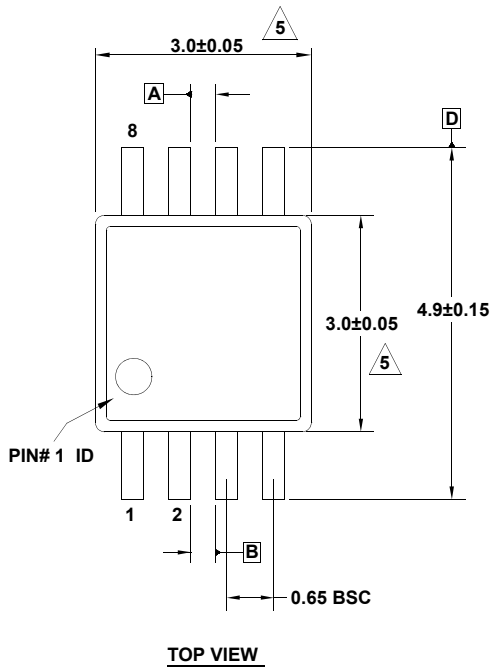
# Package Outline Drawing

For the most recent package outline drawing, see [M8.118](#).

## M8.118

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11



**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

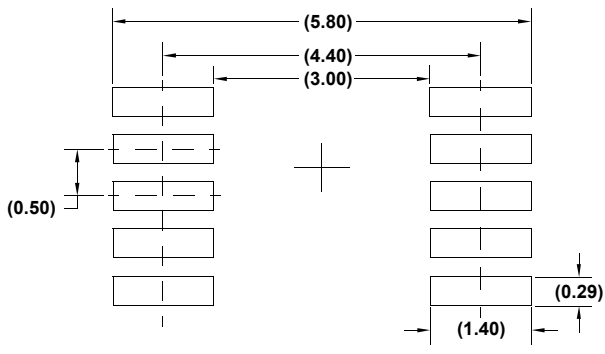
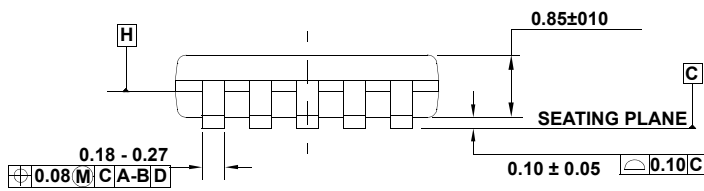
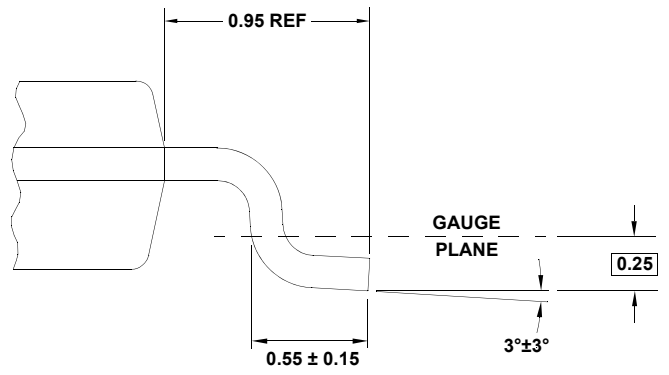
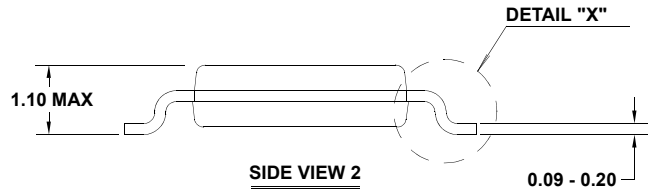
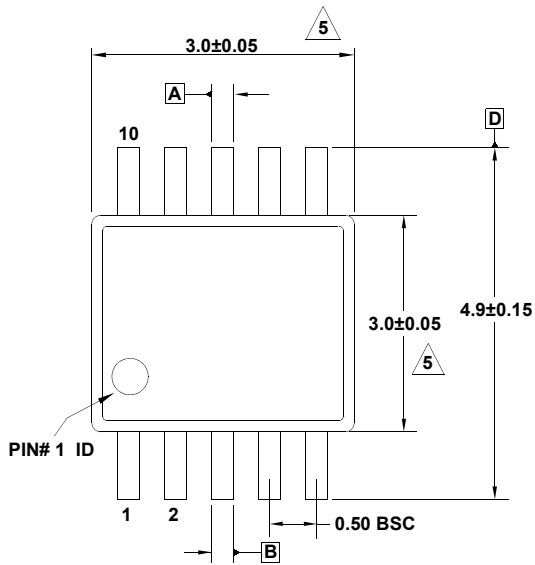
# Package Outline Drawing

For the most recent package outline drawing, see [M10.118](#).

## M10.118

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 4/12



**NOTES:**

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-BA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

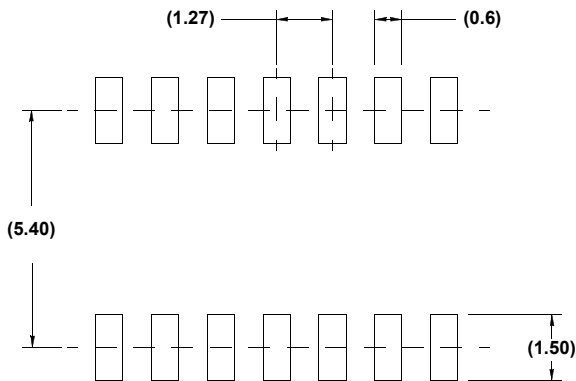
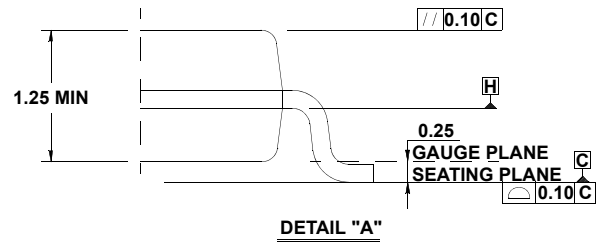
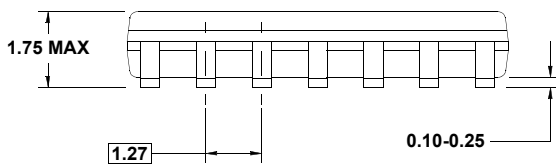
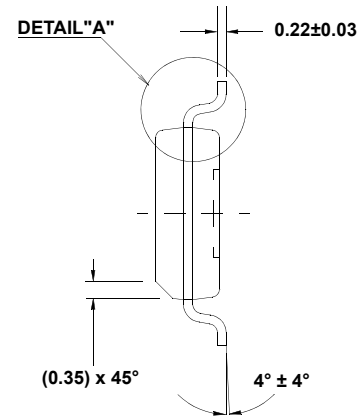
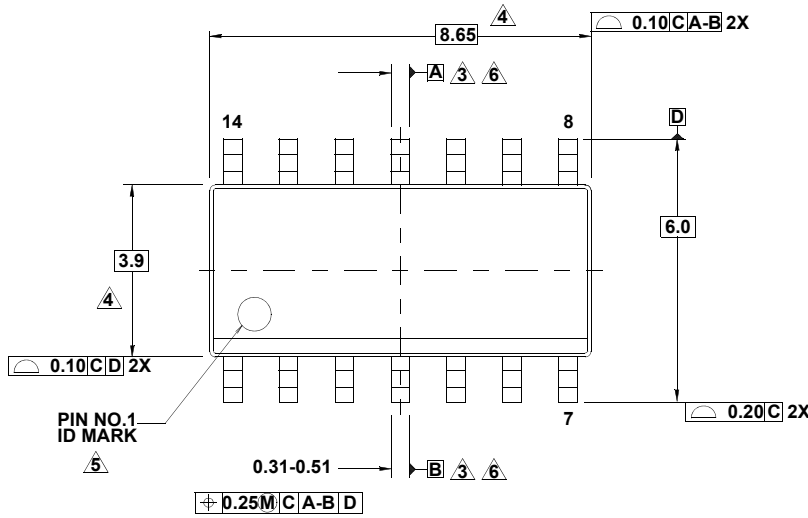
# Package Outline Drawing

For the most recent package outline drawing, see [M14.15](#).

## M14.15

### 14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 1, 10/09



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions.  
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AB.

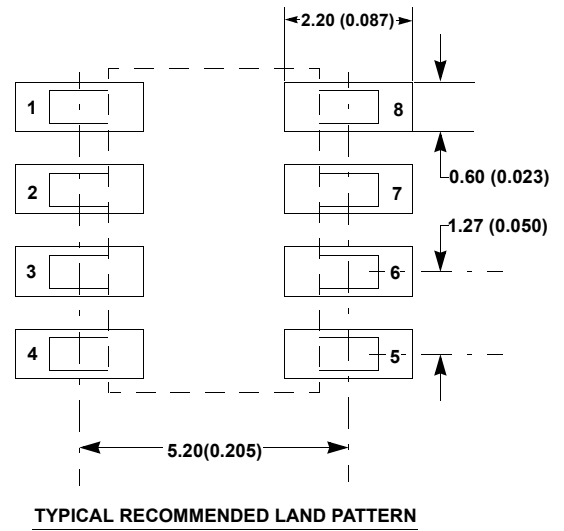
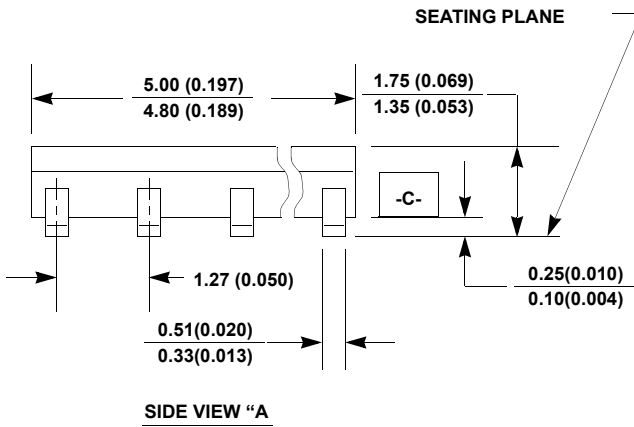
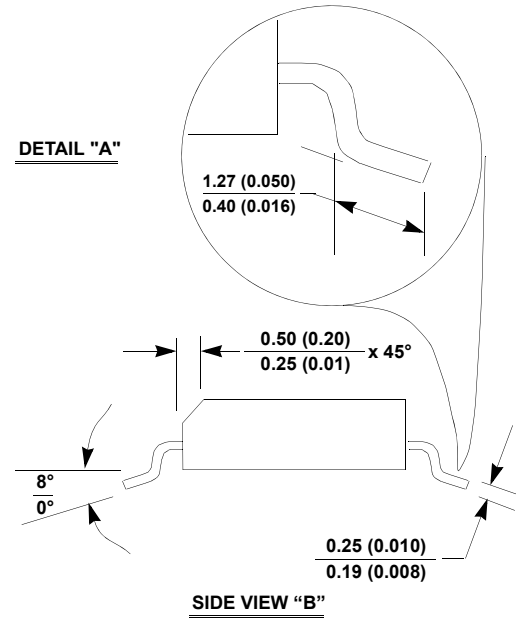
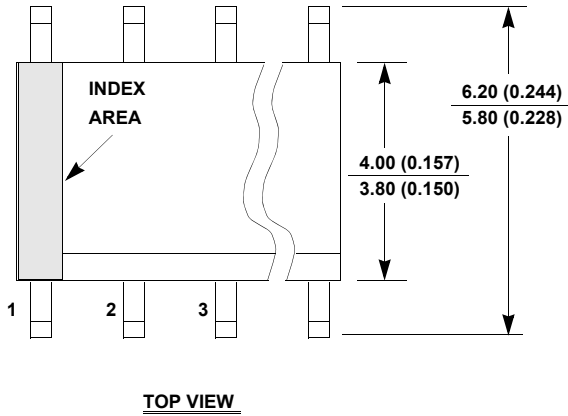
# Package Outline Drawing

## M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 1/12

For the most recent package outline drawing, see [M8.15](#).



**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.