ISL15100

Single Port, PLC Differential Line Driver

FN8577
Rev 0.00
September 19, 2013

The ISL15100 is a single port differential line driver developed for Power Line Communication (PLC) applications. The device is designed to drive heavy line loads while maintaining the high level of linearity required in OFDM PLC modem links. With 15.5dBm of total transmit signal power into 100Ω line load, the driver achieves -43dB average MTPR distortion across the output spectrum up to 86MHz.

The ISL15100 has two bias current control pins (C0, C1) to allow for four power settings (disable, low, medium, high). In disable mode, the line driver outputs maintain a high impedance in the presence of high receive signal amplitude, so it doesn't affect TDM receive signal integrity.

The ISL15100 is available in the thermally-enhanced 16 Ld QFN and is specified for operation over the full -40°C to +85°C ambient temperature range.

Features

- Single differential driver
- 100MHz Broadband PLC G.hn, EOC, HomePlug AV2
- Control pins for enable/disable and supply current selection
- High output impedance when disabled for TDM operation
- -43dBc average MTPR distortion at full line power
- Single +12V or bipolar ±6V nominal supplies
- High surge current handling capability

Applications

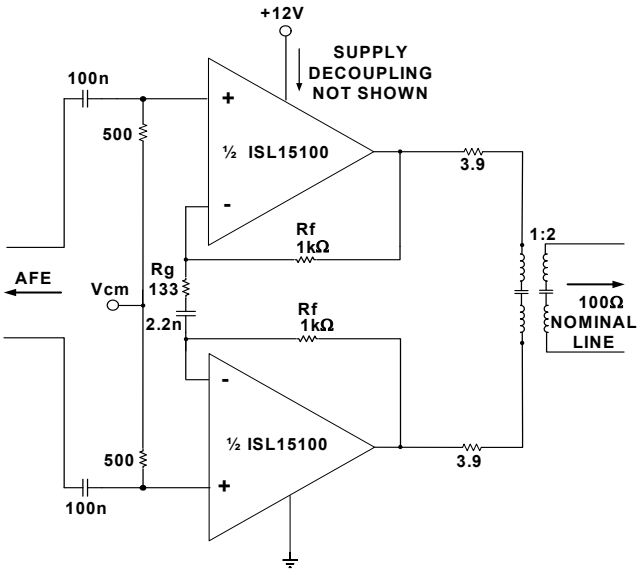
- Power Line Communication differential driver
- Pin compatible upgrade to ISL1571IRZ

Related Literature

- AN1325 "Choosing and Using Bypass Capacitors"

TABLE 1. ALTERNATE SOLUTIONS

PART #	NOMINAL ±V_S (V)	BANDWIDTH (MHz)	APPLICATIONS
ISL1571	±6, +12	200	HomePlug AV1



TYPICAL DIFFERENTIAL I/O LINE DRIVER

FIGURE 1. TYPICAL APPLICATION CIRCUIT

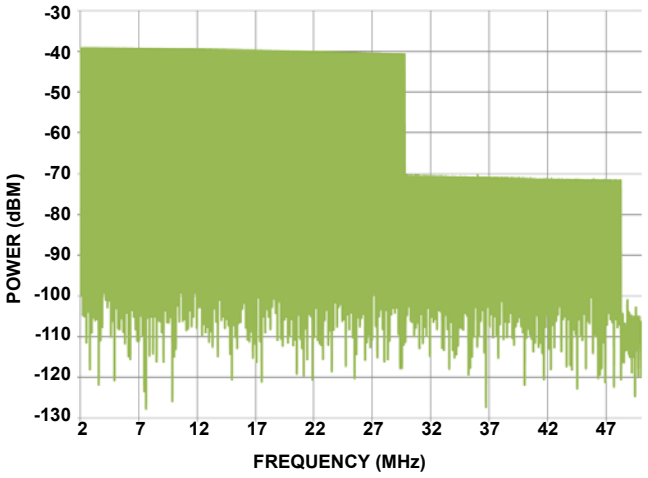


FIGURE 2. 50MHz PLC SPECTRUM

Connection Diagram

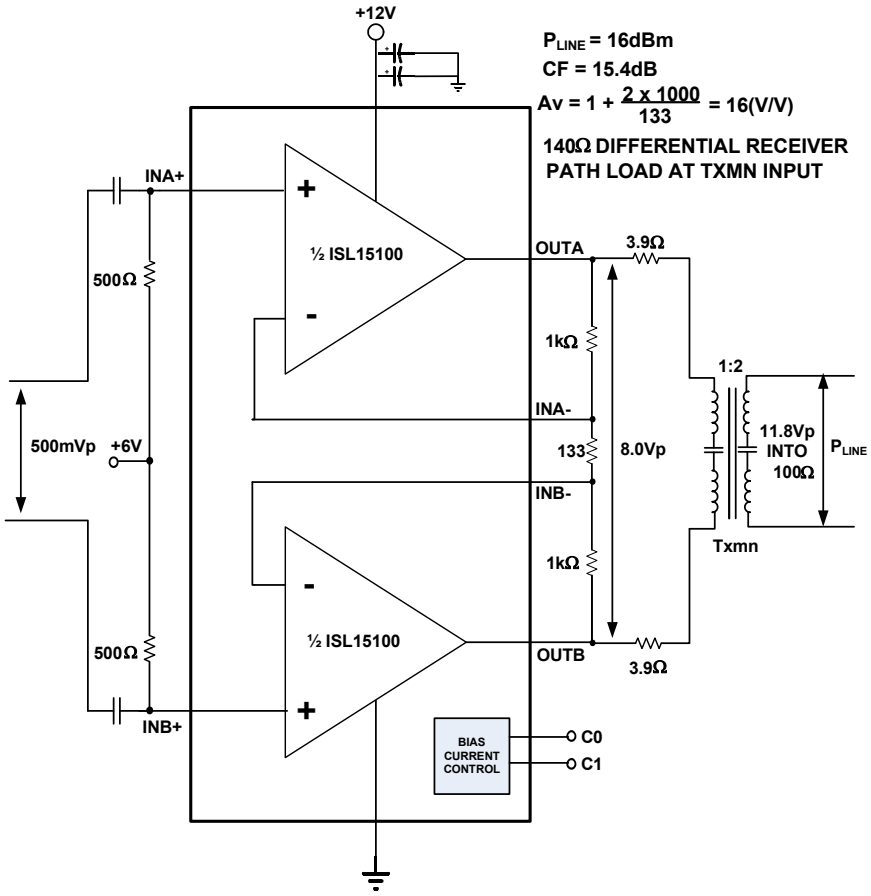


FIGURE 3. TYPICAL DIFFERENTIAL AMPLIFIER I/O

Ordering Information

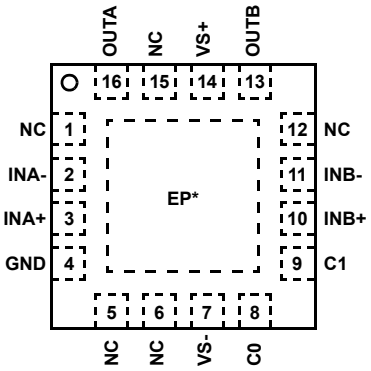
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL15100IRZ	151 00IRZ	-40 to +85	16 Ld QFN	L16.4x4H
ISL15100IRZ-T7 (Note 1)	151 00IRZ	-40 to +85	16 Ld QFN	L16.4x4H
ISL15100IRZ-T13 (Note 1)	151 00IRZ	-40 to +85	16 Ld QFN	L16.4x4H
ISL15100EVAL1Z	Evaluation Board			

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL15100. For more information on MSL please see tech brief TB363.

Pin Configuration

ISL15100
(16 LD QFN)
TOP VIEW



*EXPOSED THERMAL PAD CONNECTS TO MOST NEGATIVE SUPPLY

Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
EP	THERMAL PAD	Connect to the Most Negative Supply
1	NC	No Internal Connection
2	INA-	Amplifier A Inverting Input
3	INA+	Amplifier A Non-Inverting Input
4	GND	Ground
5	NC	No Internal Connection
6	NC	No Internal Connection
7	V_S-	Negative Supply Voltage (-6V for split supplies, GND for single supply operation)
8	C0	Digital Control Pin
9	C1	Digital Control Pin
10	INB+	Amplifier B Non-Inverting Input
11	INB-	Amplifier B Inverting Input
12	NC	No Internal Connection
13	OUTB	Amplifier B Output
14	V_S+	Positive Supply Voltage (+6V for split supplies, +12V for single supply operation)
15	NC	No Internal Connection
16	OUTA	Amplifier A Output

C0, C1 Truth Table

C1	C0	FUNCTION
0	0	High Bias Setting
0	1	Medium Bias Setting
1	0	Low Bias Setting
1	1	Outputs Disabled (Power Down)

Absolute Maximum Ratings (T_A = +25°C)

V_S+ Voltage to V_S- or GND . . . . . -0.3V to +13.3V
INA+, INB+ Voltage . . . . . GND to V_S+
C_0, C_1 Voltage to GND . . . . . -0.3V to V_S+
Current into any Input 8mA
Continuous Output Current for Long Term Reliability 50mA
Latch-up (Tested per JESD78D, Class II) 100mA
ESD Rating
Human Body Model (Tested per JESD22-A114F) 4kV
Charge Device Model (Tested per JESD22-C101E) 1.5kV
Machine Model (Tested per JESD22-A115C) 300V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 4, 5)	53	16.5

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Ambient Temperature Range . . . . . -40°C to +85°C
Junction Temperature Range . . . . . -40°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_S+ = +12V, V_S- = GND = 0V, see Figure 3, Full Bias (C_0 = C_1 = 0V), T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DYNAMIC PERFORMANCE						
-3dB Bandwidth	BW	Figure 3, $2V_{P-P}$ differential output at pins		180		MHz
Slew Rate	SR	Differential V_{OUT} (V_{OUTA} - V_{OUTB}) from -5V to +5V ($10V_{P-P}$)		1200		V/µs
Total Harmonic Distortion	THD, Low Frequency, Light Load	200kHz, differential $12V_{P-P}$, across ≥350Ω differential load		-88	-67	dBc
	THD, Low Frequency, Heavy Load	200kHz, differential $12V_{P-P}$, across 29Ω differential load		-72	-68	dBc
	THD, High Frequency, Light Load	4MHz, differential $12V_{P-P}$, across ≥350Ω differential load		-64	-58	dBc
	THD, High Frequency, Heavy Load	4MHz, differential $12V_{P-P}$, across 29Ω differential load		-51	-48	dBc
Avg. Multi-Tone Power Ratio	MTPR	2MHz to 50MHz, 25kHz tone spacing, P_{LINE} = 15.5dBm, CF = 15dB		-43		dBc
Off State Multi-Tone Power Ratio	MTPR-OFF	2MHz to 50MHz, 25kHz tone spacing, P_{LINE} = 15.5dBm, CF = 15dB		-55		dBc
Non-inverting Input Spot Voltage Noise	Eni	F > 1MHz, spot noise voltage on INA+ and INB+ inputs separately		6		$nV/\sqrt{Hz}$
Non-inverting Input Spot Current Noise	Ini+	F > 1MHz, spot noise current on INA+ and INB+ inputs separately		13		$pA/\sqrt{Hz}$
Inverting Input Spot Current Noise	Ini-	F > 1MHz, spot noise current on INA- and INB- inputs separately		50		$pA/\sqrt{Hz}$
DC AND INPUT CHARACTERISTICS						
Non-Inverting Input Bias Current	I_{B+}	Non-inverting inputs, INA+ and INB+, at mid-supply voltage (Note 7)	-7	2	7	µA
Non-Inverting Input Bias Current Mismatch	I_{B+DM}	Difference between the INA+ and INB+ bias currents	-0.5	0	0.5	µA
Inverting Input Bias Current	I_{B-}	Inverting inputs, INA- and INB-, at mid supply voltage (Note 7)	-90	-30	55	µA

Electrical Specifications

V_S+ = +12V, V_S- = GND = 0V, see Figure 3, Full Bias (C_0 = C_1 = 0V), T_A = +25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Inverting Input Bias Current Mismatch	I_{B-DM}	Difference between the INA- and INB- input bias currents	-35	0	35	µA
Inverting Input Bias Current Common Mode	I_{B-CM}	Average inverting input bias currents (Note 7)	-90	-30	55	µA
Input Offset Voltage	V_{IOA}, V_{IOB}	Voltage difference from INA+ to INA- and from INB+ to INB-	-85	0	85	mV
Input Offset Voltage Mismatch	V_{IODM}	V_{IOA} - V_{IOB}	-5	0	5	mV
Input Offset Voltage Common Mode	V_{IOCM}	Average offset voltage across the two inputs	-80	20	80	mV
Differential Mode Output Offset Voltage	V_{OSDM}	Output referred total effect of all differential DC error terms	-7.8	0	7.8	mV
Common Mode Output Offset Voltage	V_{OSCM}	Output referred total effect of all common mode DC errors	-105	40	145	mV
Input Headroom to Positive Supply	(V_S+) - $V_{IN(MAX)}$	INA+ and INB+ required margin to V_S+ supply		3		V
Input Headroom to Negative Supply	$V_{IN(MIN)}$ - (V_S-)	INA+ and INB+ required margin to V_S- supply		3		V
OUTPUT CHARACTERISTICS						
Output Swing	V_{O-OPEN}	V_S = ±6V, Differential R_{LOAD} ≥ 1kΩ, each output pin voltage range	±4.85	±5.0		V
	$V_{O-LOADED}$	V_S = ±6V, V_O in linear region, Differential R_{LOAD} = 29Ω, each output pin voltage range.		±4.6		V
		V_S = ±6V, V_O driven into the rail, differential R_{LOAD} = 29Ω, each output pin voltage range.	±4.2	±4.7		V
Output Current	I_O	Linear output current (not short circuit)	±300	±400		mA
POWER SUPPLY						
Bipolar Supply Range	±V_S	Symmetric supply, pin 4 at GND for logic reference	±4	±6	±6.6	V
Single Supply Range	V_S+	Single supply with V_S- and pin 4 at GND	8	12	13.2	V
Positive Supply Currents	I_S+ (Full bias)	$V_{O(DIFF)}$ = 0V, C_0 = C_1 = 0V	27	32	37	mA
	I_S+ (Medium bias)	$V_{O(DIFF)}$ = 0V, C_0 = 3.3V, C_1 = 0V	19	23	26	mA
	I_S+ (Low bias)	$V_{O(DIFF)}$ = 0V, C_0 = 0V, C_1 = 3.3V	12	15	18	mA
	I_S+ (Power down)	C_0 = C_1 = 3.3V	5.5	7	8.5	mA
C_0, C_1 Input High Current	I_{INH}, C_0 or C_1	C_0 = C_1 = 3.3V (Note 7)	-150	-90	-30	µA
C_0, C_1 Input Low Current	I_{INL}, C_0 or C_1	C_0 = C_1 = 0V (Note 7)	-1.5	1	1.5	µA
C_0, C_1 Logic High Voltage	V_{INH}	Pin 4 at GND, logic reference pin	2	3.3	5.5	V
C_0, C_1 Logic Low Voltage	V_{INL}	Pin 4 at GND, logic reference pin	-0.3	0	0.8	V

NOTES:

6. Compliance to data sheet limits is assured by one or more methods: production test, characterization and/or design.
7. Positive currents flow out of the pin.

Applications Information

Product Description

The ISL15100 is a differential operational amplifier designed for line driving in power line communications (PLC). It is a low distortion, current mode feedback amplifier that draws moderately low supply current. Due to the current feedback architecture, the ISL15100 closed-loop -3dB bandwidth is dependent on the value of the feedback resistor. The desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G.

Feedback Resistor Values

The ISL15100 has been designed and specified with R_F = 1kΩ for A_V = +16. As is the case with all current feedback amplifiers, wider bandwidth at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of the feedback resistor will cause rolloff to occur at a lower frequency.

Quiescent Current vs Temperature

The ISL15100 was designed to have the quiescent current increase with temperature, which maintains good distortion performance at high temperatures.

Supply Voltage Range

The ISL15100 operates with bipolar supply voltages from ±4.0V to ±6.6V (±6.65V maximum). Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages.

Single Supply Operation

If a single supply is desired, values from +8.0V to +13.2V (+13.3V maximum) can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either:

1. DC bias the inputs at an appropriate common mode voltage and AC-couple the signal.
2. Ensure the driving signal is within the common mode range of the ISL15100.

Multi-Tone Power Ratio (MTPR)

G.hn PLC uses OFDM modulation to digitally encode data for communication. A carrier spacing of 24.41kHz is used in power lines, and 48.82kHz is used in phone lines.

In multi-tone signaling, linearity is shown in the MTPR measurement. MTPR measures the difference in power of a carrier tone vs. a missing tone.

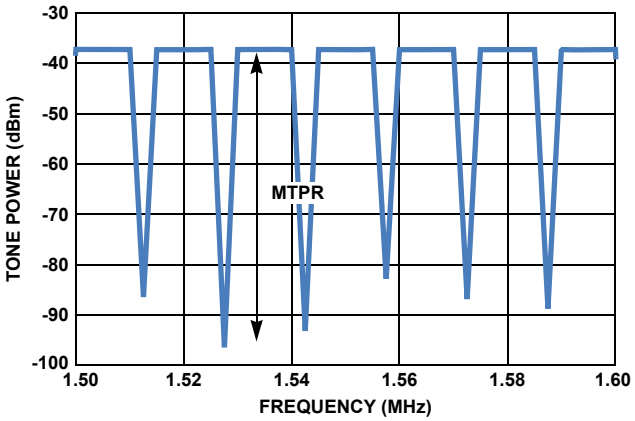


FIGURE 4. PLC SIGNAL TONES WITH 25kHz SPACING

Figure 4 shows ISL15100's MTPR performance for a narrow frequency span.

Disable Linearity

Unlike DSL, communication in PLC systems is half duplex meaning only one device can transmit at a time. When the line driver is not transmitting, it is disabled and the receiver is enabled. Figure 5 shows the shared transmit and receive signal path of two ends. When Txa is transmitting, optimal MTPR is achieved if Txb is removed. Since Txb cannot be removed, the best MTPR occurs if the line driver is a very high impedance when disabled.

R_{BM} are resistors to limit fault currents, and to provide a driving impedance to the transformer, thus setting its frequency span. R_{BM} is typically low in value (<10Ω).

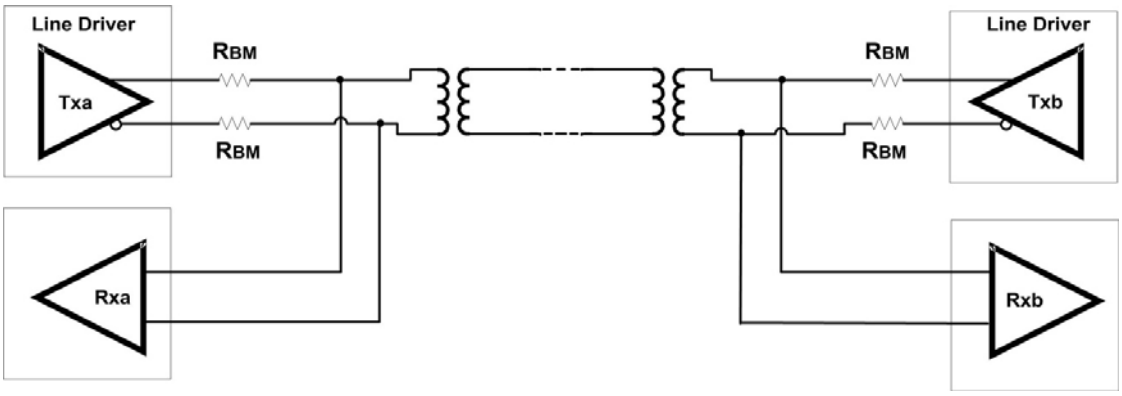


FIGURE 5. Tx AND Rx SIGNAL PATH. CASE1:[Txa: ON, Rxa: OFF, Txb: OFF, Rxb: ON]. CASE2:[Txa: OFF, Rxa: ON, Txb: ON, Rxb: OFF]

PC Board Design Recommendation

To minimize parasitic capacitance in the ISL15100 design, consider laying out short output traces. Also, select low capacitance protection devices, and use line transformers with low interwinding capacitance in the signal path.

The supply decoupling capacitors must be close to the supply pins to minimize parasitic inductance in the supply paths. High frequency load currents are pulled through these capacitors, so placement of the 0.1µF capacitors close to the supply pin(s) improves dynamic performance. The higher value 4.7µF capacitors provide low frequency decoupling, so they can be placed farther from the supply pins.

The ISL15100's thermal pad (EP) should be connected to V_S- (ground in single supply applications). For good thermal control, include a thermal pad in the layout footprint, as shown in the "Typical Recommended Land Pattern" on the "Package Outline Drawing" page. Adding vias to this thermal pad helps dissipate heat away from the package. The ISL15100 evaluation board uses four 10mil (hole size) vias with 20mil diameter pads.

Thermal Resistance and Power Dissipation

Thermal resistance for junction to ambient, T_{JA}, is +53°C/W. The power dissipation at 12V supply is 600mW. The ambient temperature allowed given the maximum junction temperature of +150°C is:

$$T_A = T_J - \theta_{JA} \times Pd \quad \text{(EQ. 1)}$$

$$T_A = +150°C - 53°(C/W)*600mW = +118°C$$

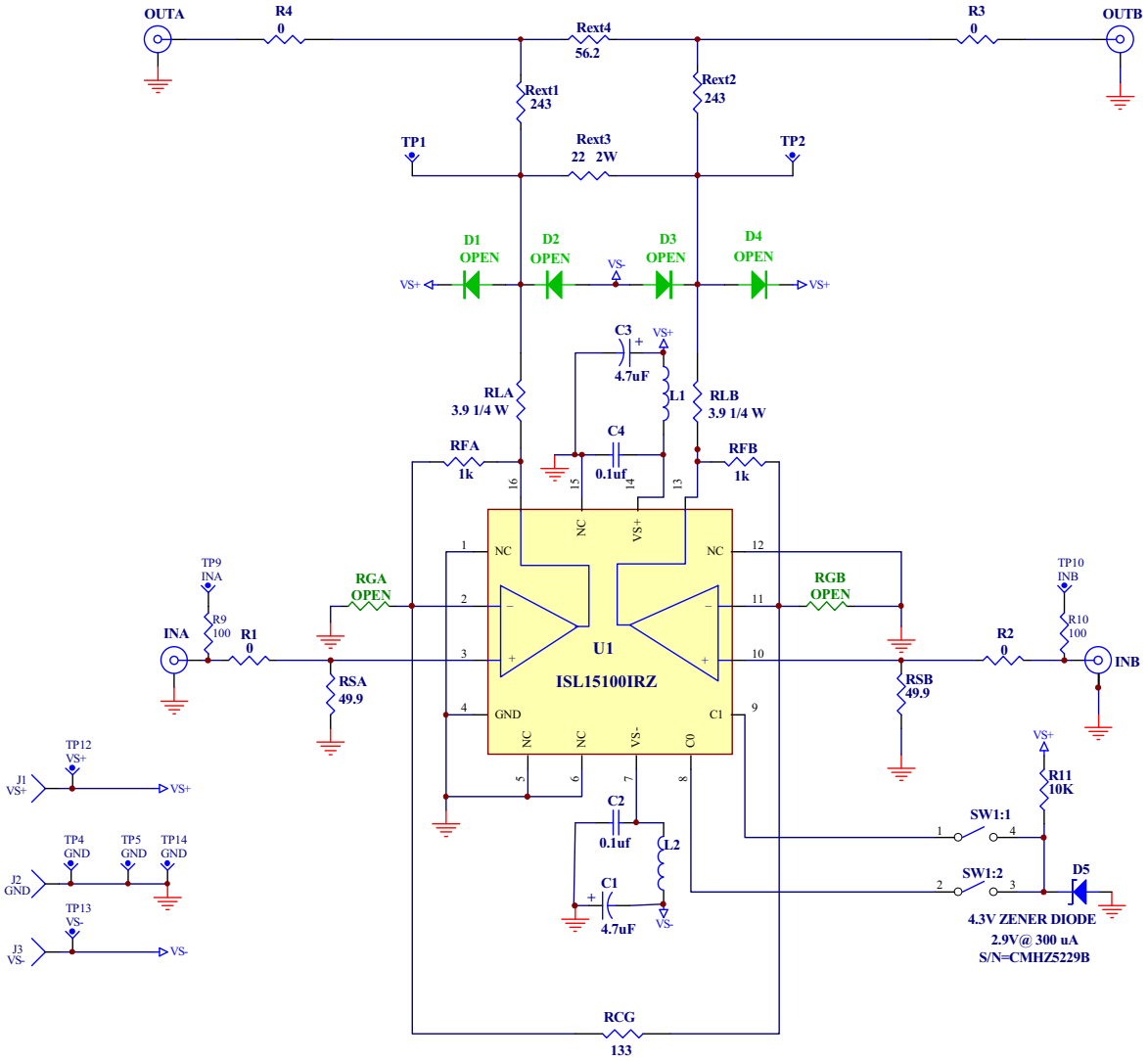


FIGURE 6. ISL15100 EVALUATION BOARD

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 19 2013	FN8577.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

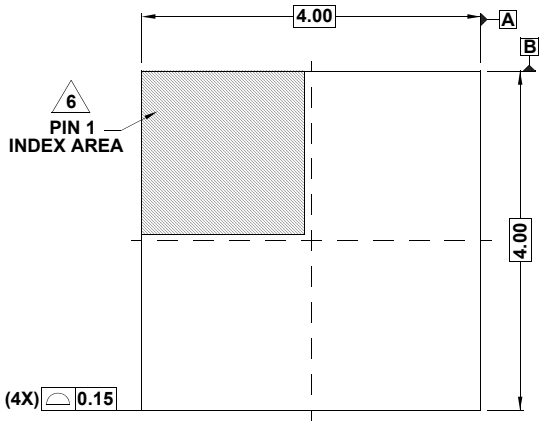
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

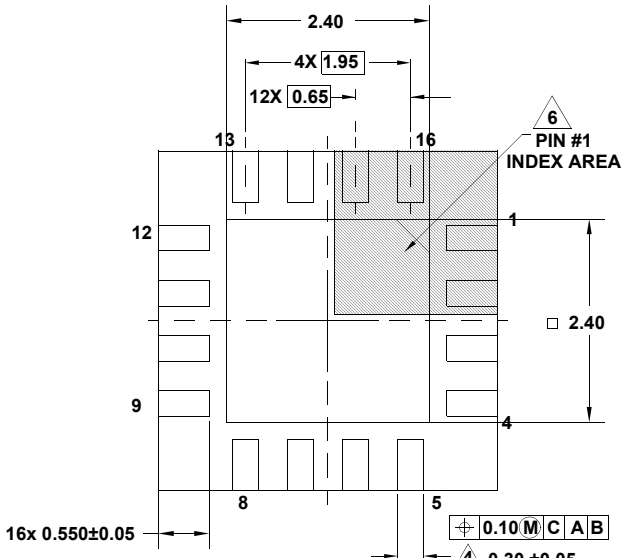
L16.4x4H

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

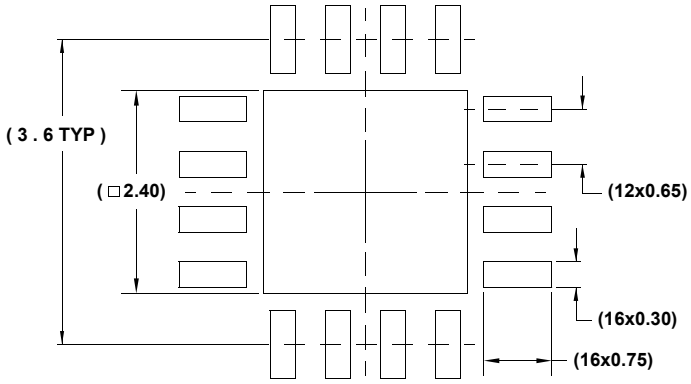
Rev 0, 1/12



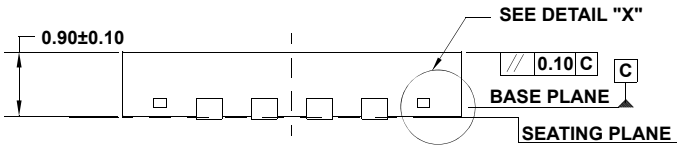
TOP VIEW



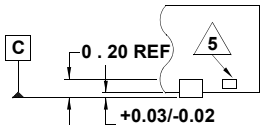
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.