# HMC858LC4B

## 14 Gpbs, 2:1 DIFFERENTIAL SELECTOR WITH PROGRAMMABLE OUTPUT VOLTAGE

### Typical Applications

The HMC858LC4B is ideal for:

- 2:1 Multiplexer up to 14 Gbps
- 16G Fiber Channel
- Serial Data Transmission up to 14 Gbps
- Redundant Path Switching
- Built-in Test
- Broadband Test & Measurement

### Features

Supports High Data Rates: up to 14 Gbps

Differential or Single-Ended Operation

Fast Rise and Fall Times: 19 / 20 ps

Low Power Consumption: 221 mW typ.

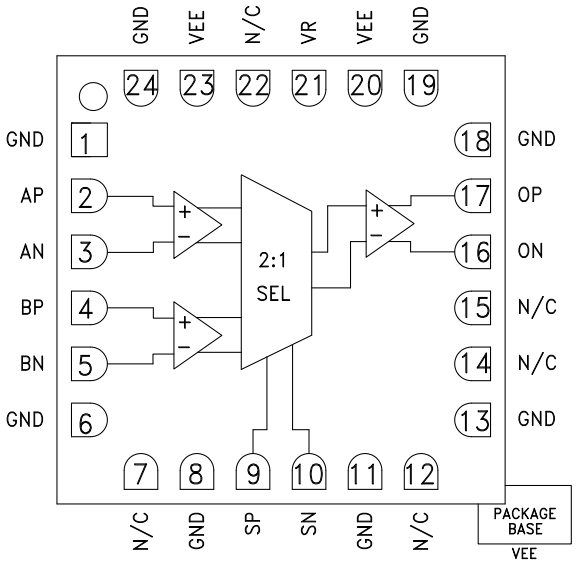
Programmable Differential
Output Voltage Swing: 500 - 1300 mVp-p

Propagation Delay: 87 ps

Single Supply: -3.3 V

24 Lead Ceramic 4x4 mm SMT Package: 16 $mm^2$

### Functional Diagram




### General Description

The HMC858LC4B is a 2:1 Selector designed to sup-port data transmission rates of up to 14 Gbps, and selector port operation of up to 14 GHz. The selector routes one of the two differential inputs to the differential output upon assertion of the proper select port. The HMC858LC4B also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All differential input signals to the HMC858LC4B are terminated with 50 ohms to ground on-chip, and may be either AC or DC coupled. The outputs of the HMC858LC4B may be operated either differentially or single-ended. Outputs can be connected directly to a 50 ohm terminated system, while DC blocking capacitors may be used if the terminating system is 50 ohms to a non-ground DC voltage. The HMC-858LC4B operates from a single -3.3V DC supply and is available in a ceramic RoHS-compliant, 4x4 mm SMT package.

### Electrical Specifications, $T_A$ = +25 °C, Vee = -3.3 V

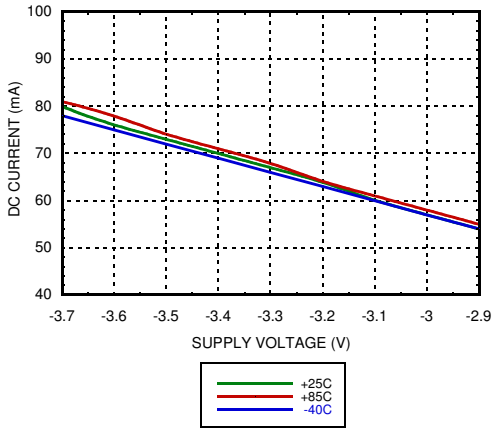
| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Power Supply Voltage | | -3.6 | -3.3 | -3.0 | V |
| Power Supply Current | | | 67 | | mA |
| Maximum Data Rate | | | 14 | | Gbps |
| Maximum Select Rate | | | 14 | | GHz |
| Input Voltage Range | | -1.5 | | 0.5 | V |
| Input Differential Range | | 0.1 | | 2.0 | Vp-p |
| Input Return Loss | Frequency <16 GHz | | 10 | | dB |
| Output Amplitude | Single-Ended, peak-to-peak | | 540 | | mVp-p |
| | Differential, peak-to-peak | | 1080 | | mVp-p |
| Output High Voltage | | | -20 | | mV |
| Output Low Voltage | | | -560 | | mV |

## Electrical Specifications *(continued)*

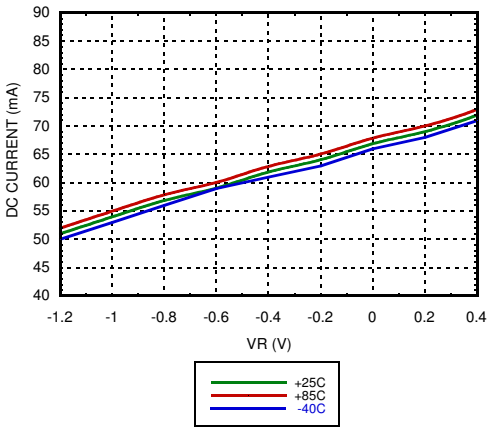
| Parameter | Conditions | Min. | Typ. | Max | Units |
|---|---|---|---|---|---|
| Output Rise / Fall Time | Differential, 20% - 80% | | 19 / 20 | | ps |
| Output Return Loss | Frequency <16 GHz | | 10 | | dB |
| Random Jitter, Jr | rms [1] | | 0.08 | 0.11 | ps rms |
| Deterministic Jitter, Jd | peak-to-peak, $2^{15}$-1 PRBS input [1] | | 2 | | ps, p-p |
| Propagation Delay, A or B to $D_{OUT}$, td | | | 87 | | ps |
| Propagation Delay Select to Data, tds | | | 89 | | ps |

[1] Added jitter calculated by de-embedding the source's jitter at 13 Gbps, $2^{15}$ -1 PRBS input.

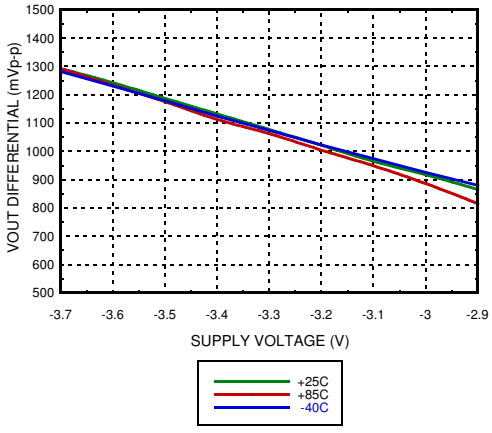
### DC Current vs. Supply Voltage [1][2]



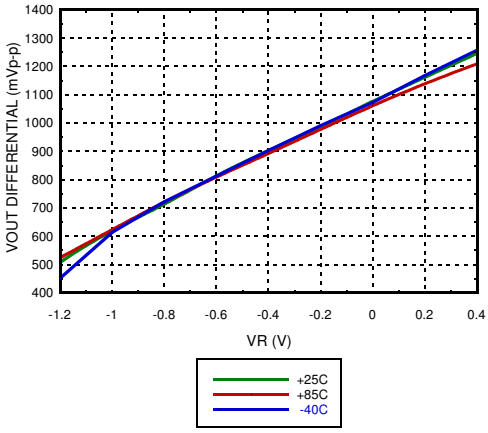

### DC Current vs. VR [2][3]




### Output Differential Voltage vs. Supply Voltage [1][2]

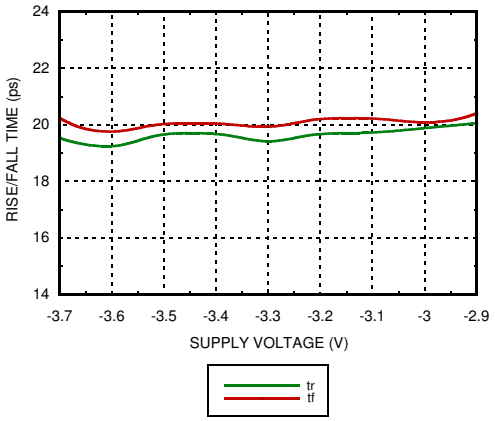



### Output Differential Voltage vs. VR [2][3]

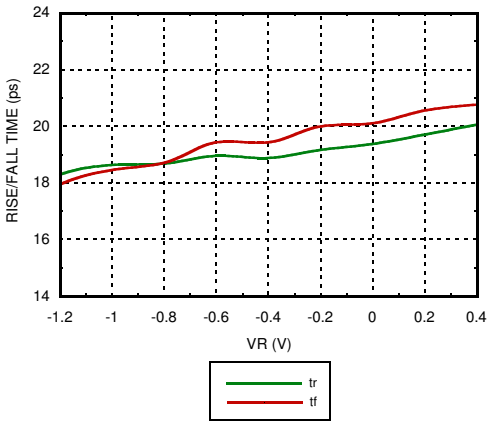



[1] VR = 0.0 V [2] Frequency = 13 GHz Vee = -3.3 V

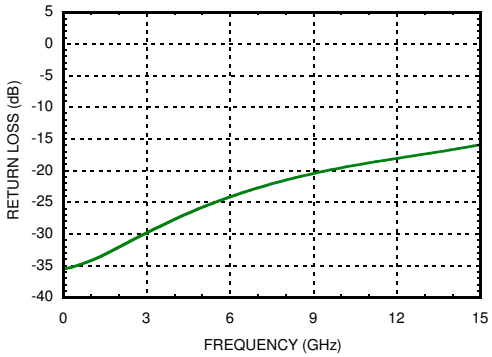
### Rise / Fall Time vs. Supply Voltage [1][2]



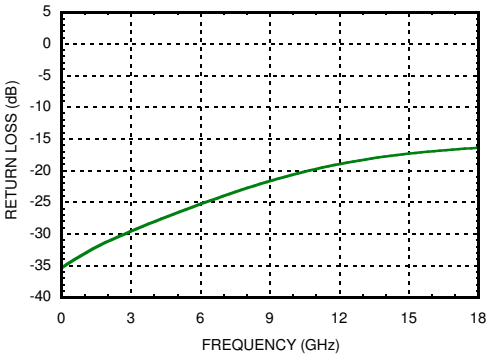

### Rise / Fall Time vs. VR [2][3]



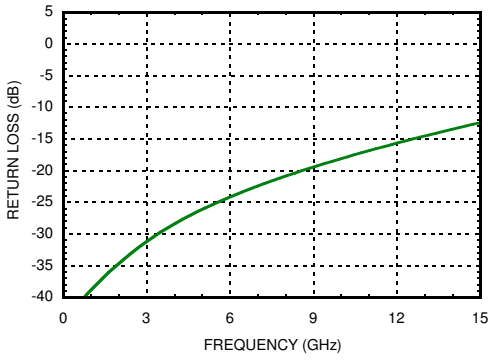

### Select Input Return Loss vs. Frequency [1][3][4]



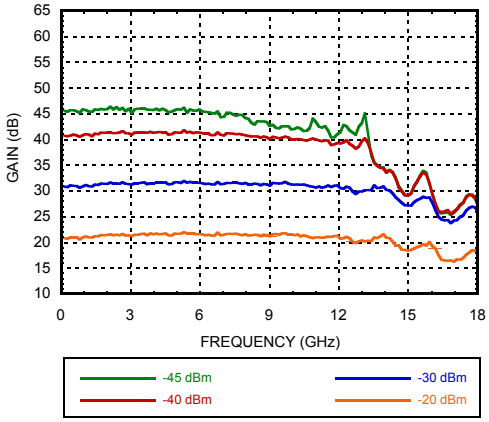

### Data Input Return Loss vs. Frequency [1][3][4]




### Output Return Loss vs. Frequency [1][3][4]

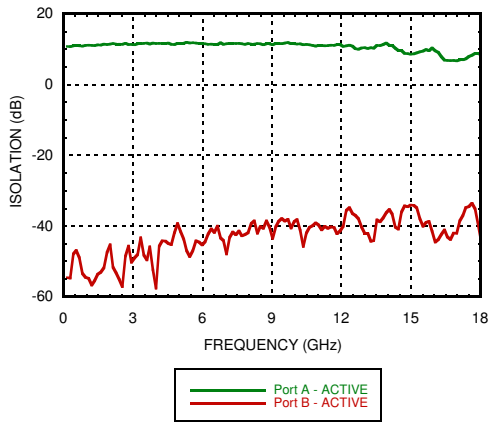



### Response vs. Input Power [1][3][5]

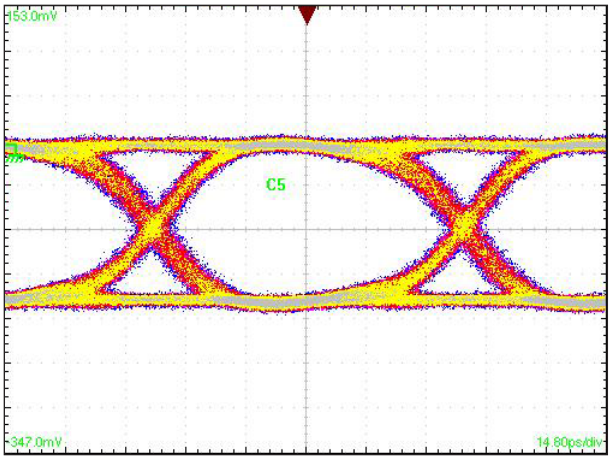



[1] VR = 0.0 V [2] Frequency = 13 GHz [3] Vee = -3.3 V
[4] Device measured on evaluation board with gating after connector [5] Device measured on evaluation board with port extensions

### Isolation [1][2][3]

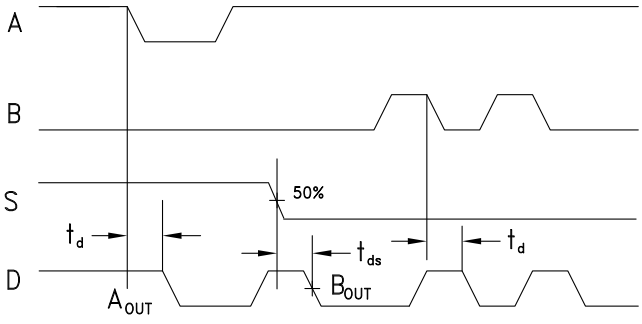



### Eye Diagram




[1] Test Conditions:
Waveform generated with an Agilent N4903A
J-Bert differential 400 mV 13 Gbps PN $2^{15}$-1 input signal.
Eye Diagram data presented on a Tektronix CSA 8000

### Timing Diagram




td = propagation delay, A to D
tds = propagation delay, Select to D

### Truth Table

| Inputs | | Outputs |
|---|---|---|
| SP | SN | DP |
| H | L | A -> D |
| L | H | B -> D |
| H = Positive voltage level<br>L = Negative voltage level | | |
| Notes:<br>D = DP - DN<br>S = SP - SN | | |

[1] VR = 0.0 V [2] Vee = -3.3 V [3] Device measured on evaluation board with port extensions

# HMC858LC4B

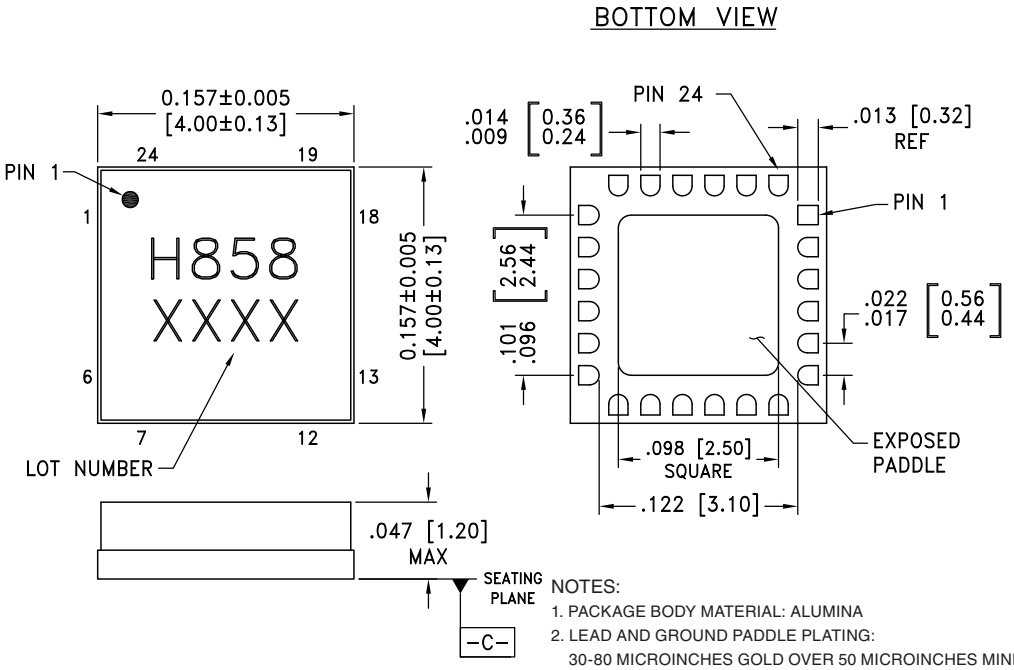
## 14 Gpbs, 2:1 DIFFERENTIAL SELECTOR WITH PROGRAMMABLE OUTPUT VOLTAGE

### Absolute Maximum Ratings

| | |
|---|---|
| Power Supply Voltage (Vee) | -3.75 V to +0.5 V |
| Input Signals | -2.0 V to 0.5 V |
| Output Signals | -1.5 V to 0.5 V |
| Junction Temperature | 125 °C |
| Continuous Pdiss (T = 85 °C (derate 30.0 mW/°C above 85 °C) | 1.22 W |
| Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case device to package paddle | 32.8 °C/W |
| Storage Temperature | -65 °C to +150 °C |
| Operating Temperature | -40 to +85 °C |
| ESD Sensitivity (HBM) | Class 1C |

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

### Outline Drawing



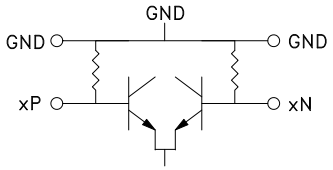
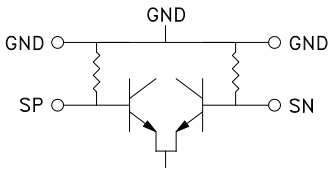
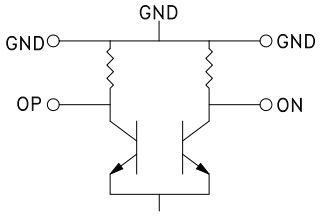

NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

### Package Information

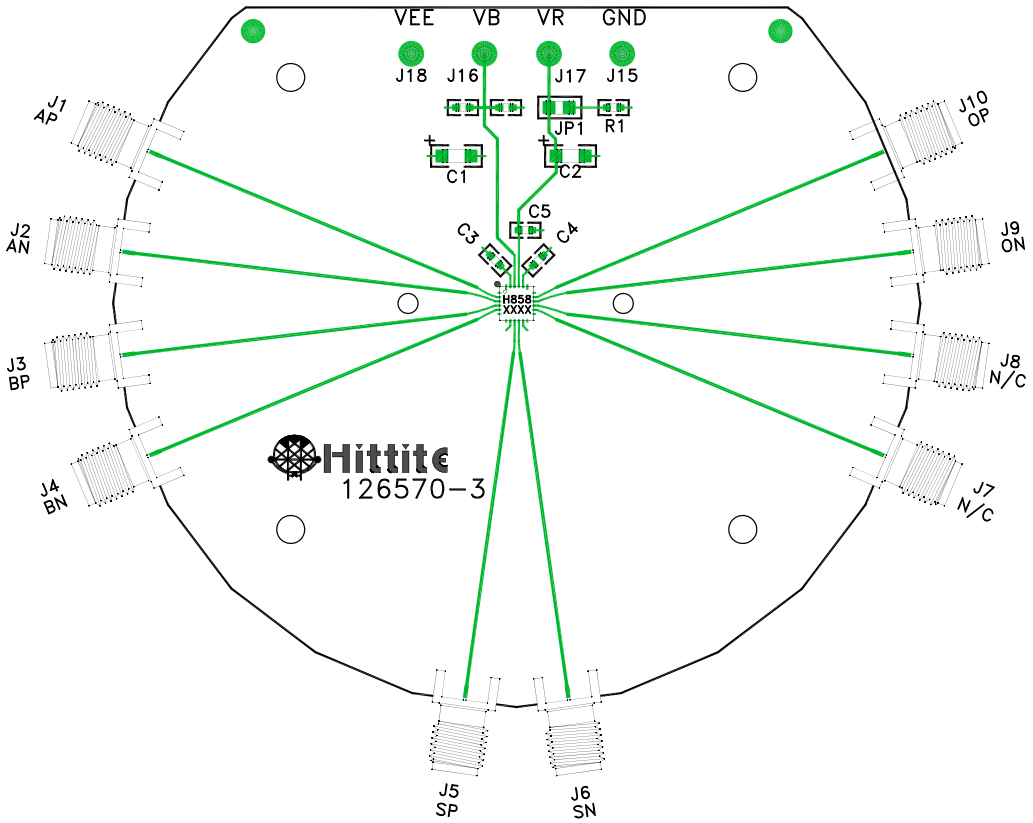
| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking [2] |
|---|---|---|---|---|
| HMC858LC4B | Alumina, White | Gold over Nickel | MSL3 [1] | H858<br>XXXX |

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

## Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|---|---|---|---|
| 1, 6, 8, 11, 13, 18 | GND | Signal Grounds |   |
| 2, 3, 4, 5 | AP, AN, BP, BN | Differential Inputs: Current Mode Logic (CML) referenced to positive supply. |   |
| 7, 12, 14, 15, 22 | N/C | No connection necessary. These pins may be connected to RF/DC ground without affecting performance. | |
| 9, 10 | SP, SN | Differential Select Inputs: Current Mode Logic (CML) referenced to positive supply. |   |
| 16, 17 | ON, OP | Differential Outputs: Current Mode Logic (CML) referenced to positive supply. |   |
| 19, 24 | GND | Supply Grounds |   |
| 20, 23 Package Base | Vee | These pins and the exposed paddle must be connected to the negative voltage supply. | |

### Evaluation PCB




### List of Materials for Evaluation PCB 126572 [1]

| Item | Description |
|---|---|
| J1 - J6, J9, J10 | PCB Mount SMA RF Connectors |
| J15 - J18 | DC Pin |
| JP1 | 0.1" Header with Shorting Jumper |
| C1, C2 | 4.7 µF Capacitor, Tantalum |
| C3 - C5 | 100 pF Capacitor, 0603 Pkg. |
| R1 | 10 Ohm Resistor, 0603 Pkg. |
| U1 | HMC858LC4B 2:1 Differential Selector |
| PCB [2] | 126570-3 Evaluation Board |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

## Application Circuit