HMC759LP3E

v00.0909

0.25 dB LSB BiCMOS MMIC 7-BIT DIGITAL ATTENUATOR, 10 - 300 MHz

Typical Applications

The HMC759LP3E is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

0.25 dB LSB Steps to 31.75 dB

Power-Up State Selection

High Input IP3: +40 dBm

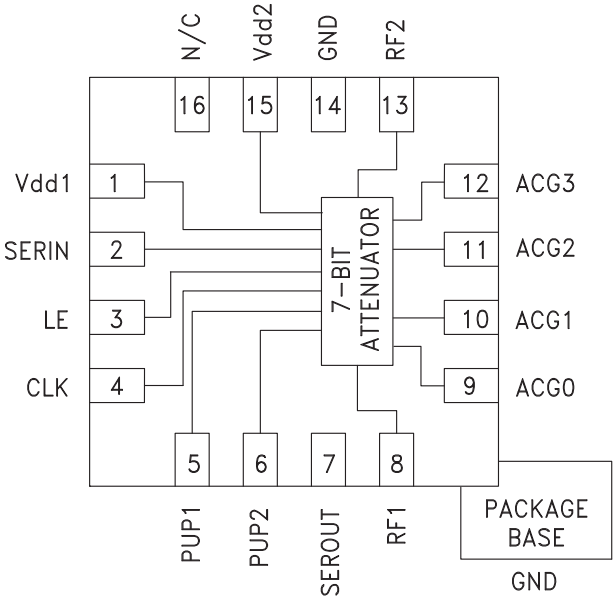
TTL/CMOS Compatible, Serial Control

Excellent State & Step Accuracy ±0.25 dB

Single +5V Supply

16 Lead 3x3mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC759LP3E is a 7-bit BiCMOS Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The control interface is CMOS/TTL compatible and accepts a three wire serial input. The HMC759LP3E features user selectable power up states and a serial output port for cascading other Hittite serial controlled components. The HMC759LP3E is housed in a RoHS compliant 3x3 mm QFN leadless package, and occupies only 9 mm^2.

Electrical Specifications

T_A = +25 °C, 50Ω System, with Vdd1 = Vdd2 = +5V & Vctl = 0/+5V

Parameter	Frequency (MHz)	Min.	Typ.	Max.	Units
Insertion Loss	10 - 300		3.3	4.5	dB
Attenuation Range	10 - 300		31.75		dB
Return Loss (RF1, RF2, All Atten. States)	10 - 300		10		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States	10 - 300	± (0.05 + 1.5% of Atten. Settling) Max.			dB
Input Power for 1 dB Compression	10 - 50 50 - 300		20 21		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power = 0 dBm Each Tone)	10 - 50 50 - 300		39 >40		dBm dBm
Bias Current (Idd1 + Idd2)	10 - 300	300	650	1000	µA
Switching Time (50% LE to 90% RF)	10 - 300		15		ns

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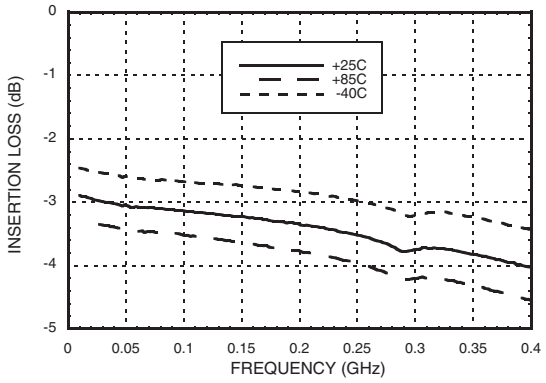
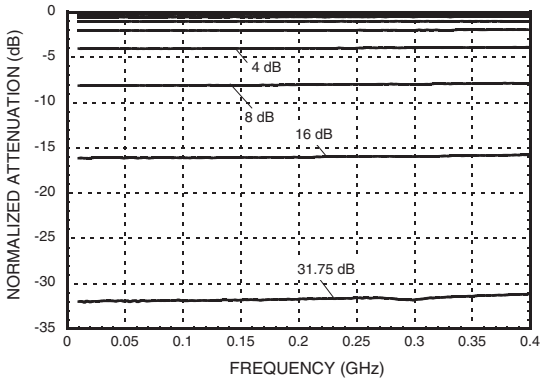
Insertion Loss vs. Temperature [1]



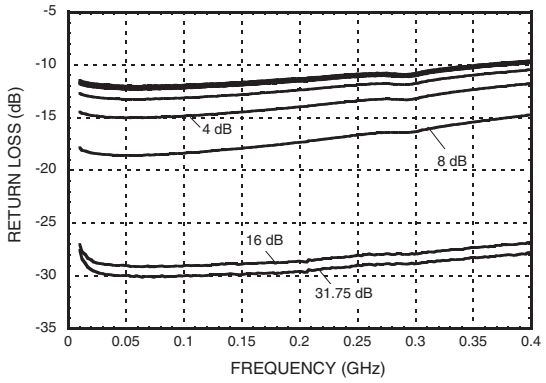
Normalized Attenuation [1]

(Only Major States are Shown)



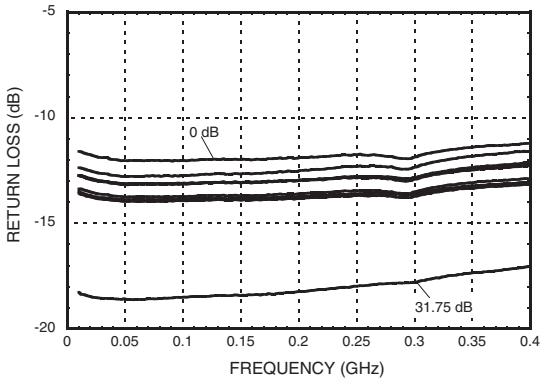
Input Return Loss [1]

(Only Major States are Shown)

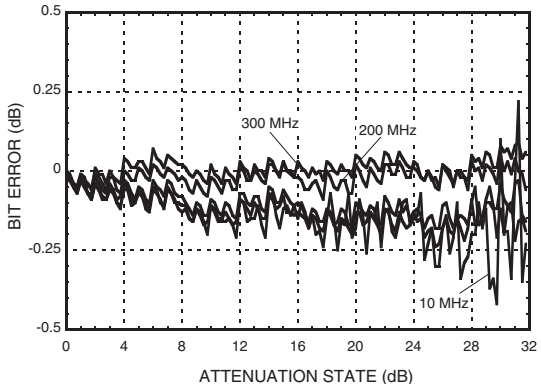


Output Return Loss [1]

(Only Major States are Shown)

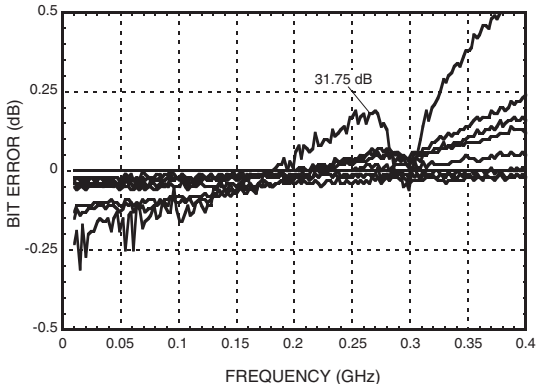


Bit Error vs. Attenuation State [2]



Bit Error vs. Frequency [2]

(Only Major States are Shown)



[1] Data taken with broadband DC blocking on RF input and output ports.

[2] C1, C2 = 10nF

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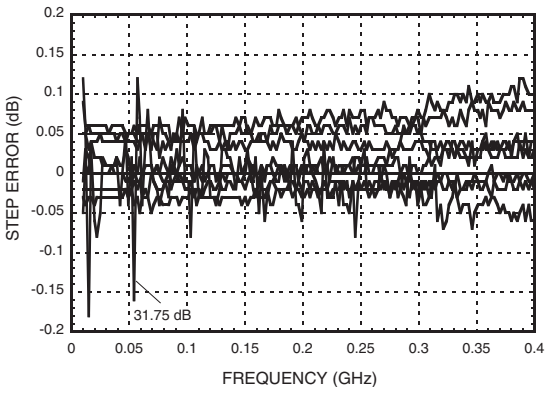
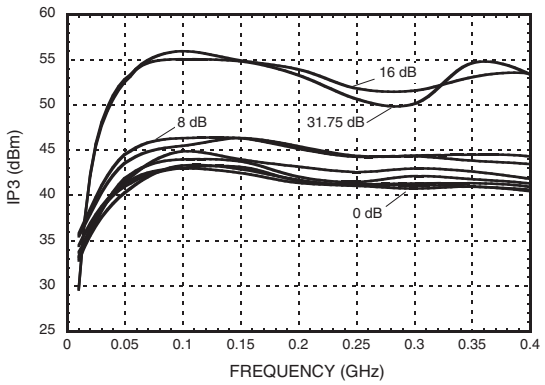
Worst Case Step Error Between Successive Attenuation States [1]



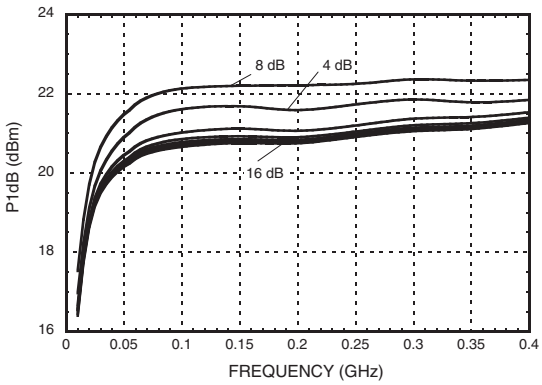
IP3 vs. Attenuation States [1]

(Only Major States are Shown)



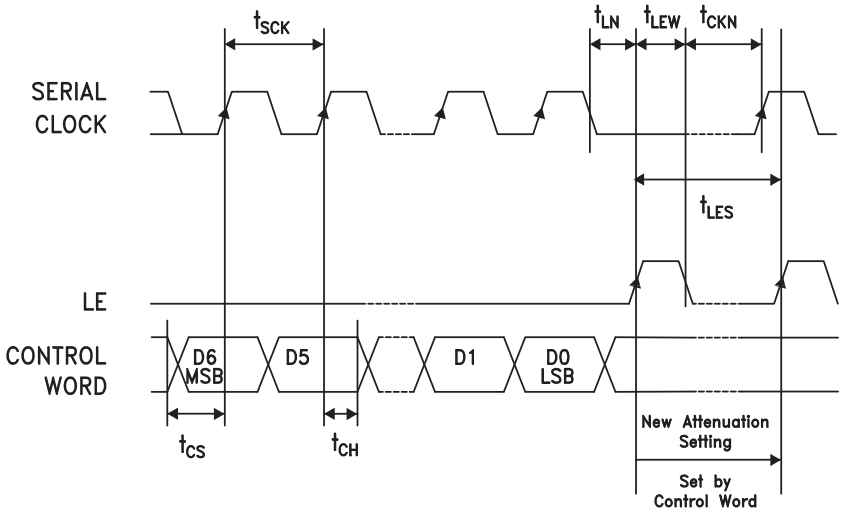
Input P1dB vs. Attenuation States [1][2]

(Only Major States are Shown)



Serial Control Interface

The HMC759LP3E contains a 3-wire SPI compatible digital interface (SERIN, CLK, LE). The 7-bit serial word must be loaded MSB first. The positive-edge sensitive CLK and LE requires clean transitions. If mechanical switches are used, sufficient debouncing should be provided. When LE is high, 7-bit data in the serial input register is transferred to the attenuator. When LE is high, CLK is masked to prevent data transition during output loading.



[1] C1, C2 = 10nF

[2] Part does not enter 1 dB compression at 31.75 dB max attenuation up to 25 dBm input power.

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Bias Voltage

Vdd (V)	Idd (Typ.) (µA)
4.5	580
5.0	650
5.5	710

Control Voltage Table

State	Vdd = +5V
Low	0 to 0.8V @ <1 µA
High	2 to 5V @ <1 µA

Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE setup-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	630 ns
Serial clock hold-time from LE, t_{CKN}	10 ns

Power-Up States

If LE is set to logic LOW at power-up, the logic state of PUP1 and PUP2 determines the power-up state of the part per PUP truth table. If the LE is kept high at power up, power up state will be indeterminate therefore is not recommended.

Power-On Sequence

The ideal power-up sequence is: GND, Vdd, digital inputs, RF inputs. The relative order of the digital inputs are not important as long as they are powered after Vdd / GND

PUP Truth Table

LE	PUP1	PUP2	Relative Attenuation
0	0	0	-31.75
0	1	0	-24
0	0	1	-16
0	1	1	Insertion Loss
1	X	X	Indeterminate

Truth Table

Control Voltage Input							Reference Insertion Loss (dB)
D6	D5	D4	D3	D2	D1	D0	
High	High	High	High	High	High	High	0
High	High	High	High	High	High	Low	0.25
High	High	High	High	High	Low	High	0.5
High	High	High	High	Low	High	High	1
High	High	High	Low	High	High	High	2
High	High	Low	High	High	High	High	4
High	Low	High	High	High	High	High	8
Low	High	High	High	High	High	High	16
Low	Low	Low	Low	Low	Low	Low	31.75

Any combination of the above states will provide an attenuation equal to the sum of the bits selected.

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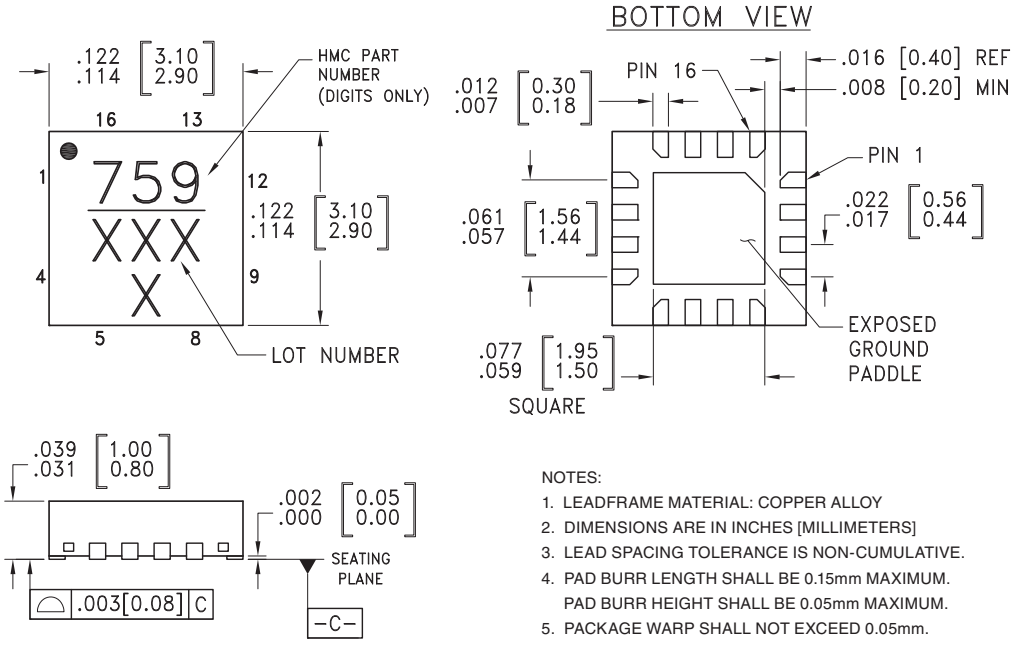
Absolute Maximum Ratings

RF Input Power (RF1, RF2)	20 dBm (T = +85 °C)
Digital Inputs (SERIN LE, CLK, PUP1, PUP2)	-0.5 to Vdd +0.5V
Bias Voltage (Vdd)	5.6V
Channel Temperature	125 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C)	0.29 W
Thermal Resistance (channel to ground paddle)	138 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC759LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	759 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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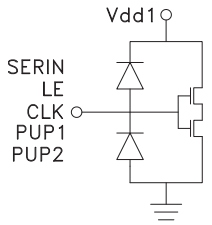
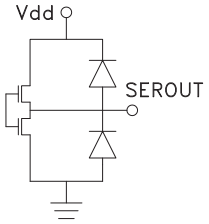
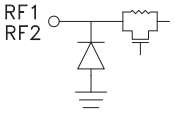
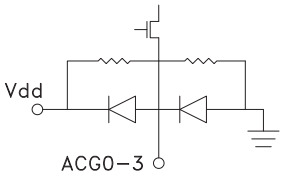
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd1	This pin should be pulled high to Vdd through a 39 kΩ resistor.	
2	SERIN	See Truth Table, Control Voltage Table and Timing Diagram.	
3	LE		
4	CLK		
5	PUP1		
6	PUP2		
7	SEROUT	Serial input data delayed by 7 clock cycles.	
8, 13	RF1, RF2	This pin is DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
9 - 12	ACG0 - 3	External capacitors to ground are required. Place these capacitors close to the package.	
14	GND	This pin and package bottom must be connected to RF/DC ground.	
15	Vdd2	Supply voltage.	
16	N/C	This pin is not connected internally; however, all data shown herein was measured with this pin connected to RF/DC ground externally.	

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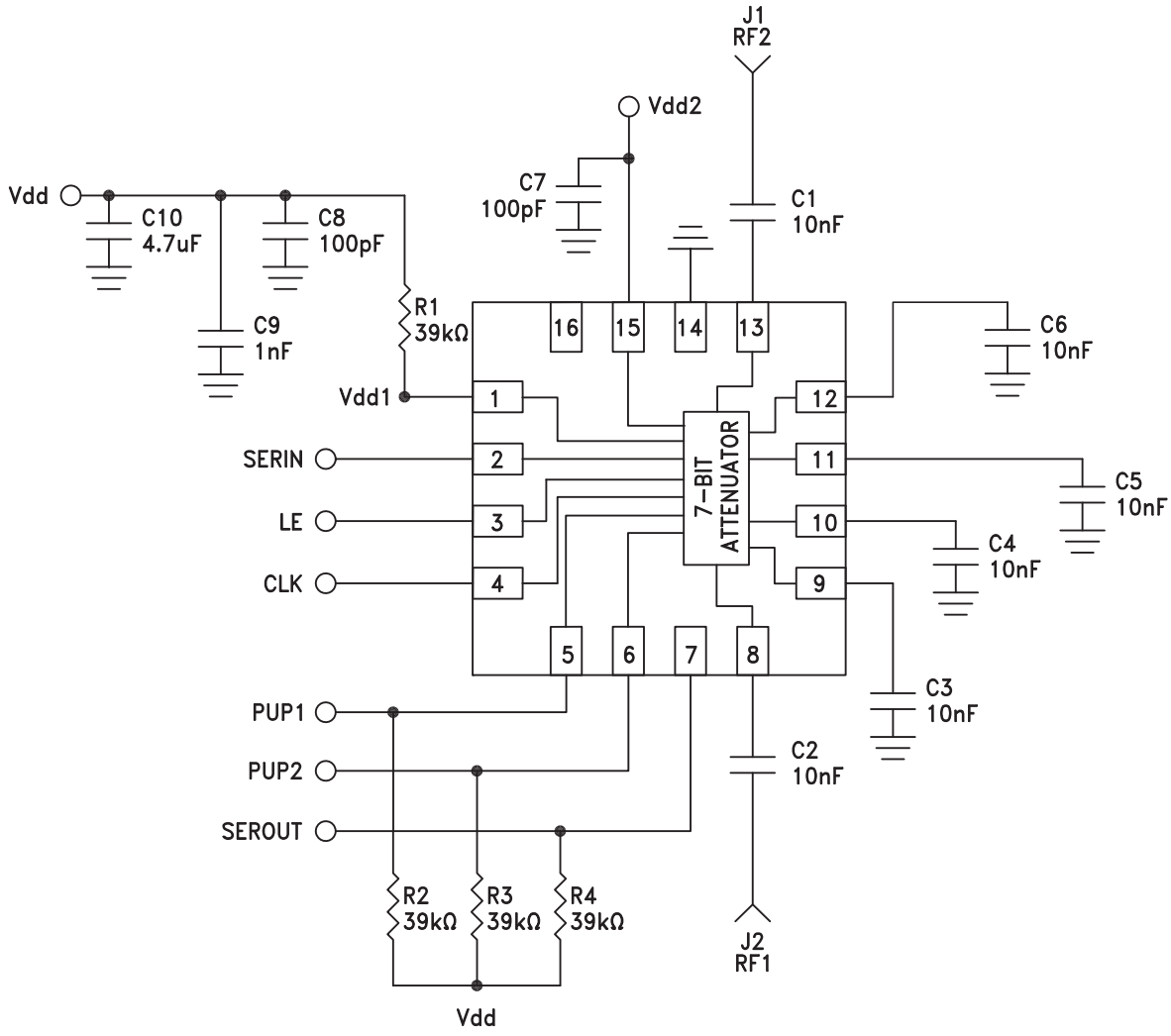
Application Circuit



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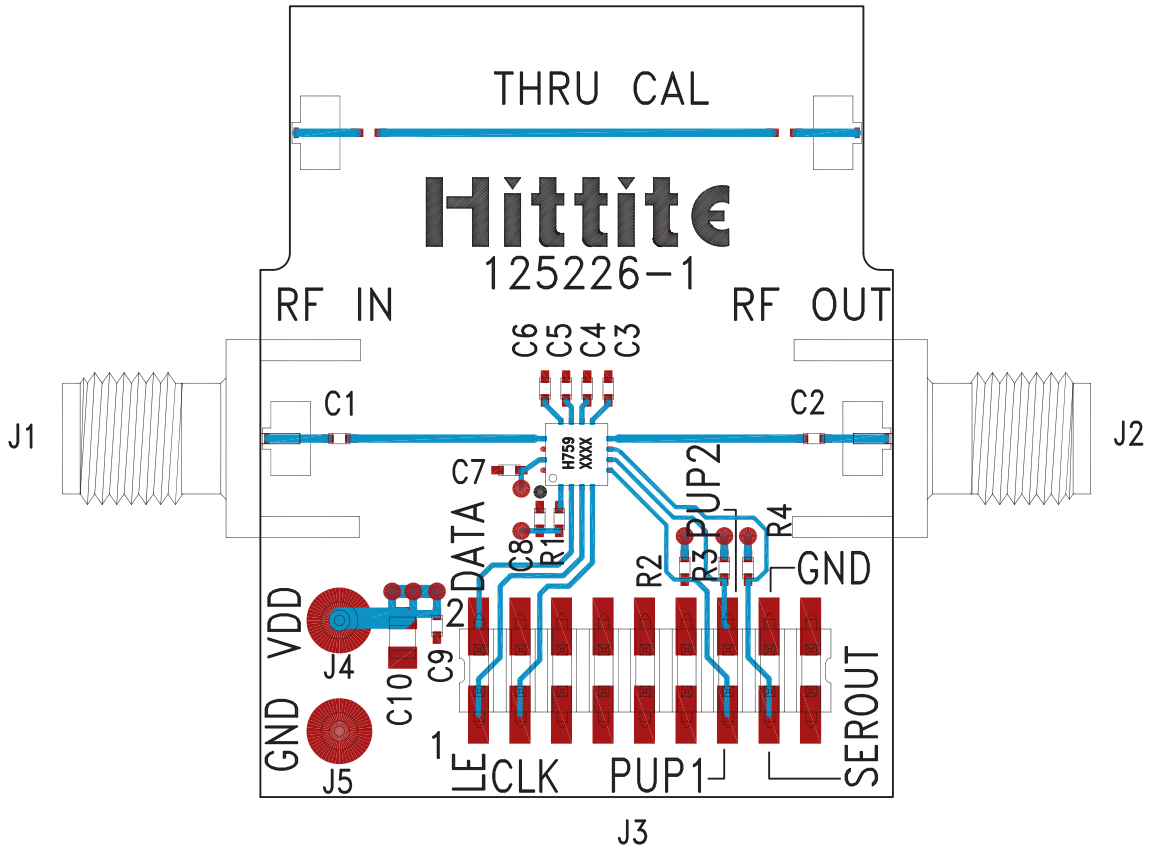
Evaluation PCB



List of Materials for Evaluation PCB 125228 [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3	18 Pin DC Connector
J4, J5	DC Pin
C1 - C6	10 nF Capacitor, 0402 Pkg.
C7, C8	100 pF Capacitor, 0402 Pkg.
C9	1 nF Capacitor, 0402 Pkg.
C10	4.7 µF Capacitor, 0805 Pkg.
R1 - R4	39K Ohm Resistor, 0402 Pkg.
U1	HMC759LP3E Digital Attenuator
PCB [2]	125226 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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