HI-506A, HI-507A, HI-508A, HI-509A

16-Channel, 8-Channel, Differential 8-Channel and Differential 4-Channel, CMOS Analog MUXs with Active Overvoltage Protection

FN3143
Rev.6.00
October 30, 2007

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16-channel multiplexer, the HI-507A is an 8-channel differential multiplexer, the HI-508A is a single 8-channel multiplexer and the HI-509A is a differential 4-channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Note AN520.

Features

- Analog Overvoltage . . . . . $70V_{P-P}$
- No Channel Interaction During Overvoltage
- Maximum Power Supply 44V
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range . . . . . ±15V
- Access Time 500ns
- Power Dissipation 7.5mW
- Pb-Free Available (RoHS Compliant)

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Ordering Information

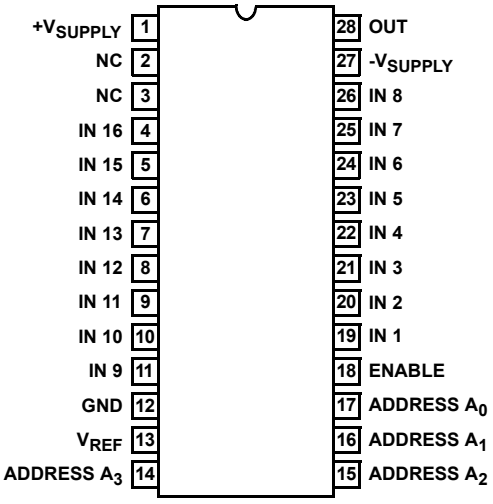
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI1-0506A-2	HI1-506A-2	-55 to +125	28 Ld CERDIP	F28.6
HI1-0506A-5	HI1-506A-5	0 to +75	28 Ld CERDIP	F28.6
HI1-0506A-8	HI1-506A-8	-55 to +125 + 160 Hour Burn-In	28 Ld CERDIP	F28.6
HI3-0506A-5	HI3-506A-5	0 to +75	28 Ld PDIP	E28.6
HI3-0506A-5Z (Note 1)	HI3-506A-5Z	0 to +75	28 Ld PDIP (Note 2) (Pb-free)	E28.6
HI3-0507A-5	HI3-507A-5	0 to +75	28 Ld PDIP	E28.6
HI3-0507A-5Z (Note 1)	HI3-507A-5Z	0 to +75	28 Ld PDIP (Note 2) (Pb-free)	E28.6
HI1-0508A-8	HI1-508A-8	-55 to +125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0508A-5	HI3-508A-5	0 to +75	16 Ld PDIP	E16.3
HI3-0508A-5Z (Note 1)	HI3-508A-5Z	0 to +75	16 Ld PDIP (Note 2) (Pb-free)	E16.3
HI1-0509A-2	HI1-509A-2	-55 to +125	16 Ld CERDIP	F16.3
HI1-0509A-5	HI1-509A-5	0 to +75	16 Ld CERDIP	F16.3
HI1-0509A-8	HI1-509A-8	-55 to +125 + 160 Hour Burn-In	16 Ld CERDIP	F16.3
HI3-0509A-5	HI3-509A-5	0 to +75	16 Ld PDIP	E16.3
HI3-0509A-5Z (Note 1)	HI3-509A-5Z	0 to +75	16 Ld PDIP (Note 2) (Pb-free)	E16.3

NOTES:

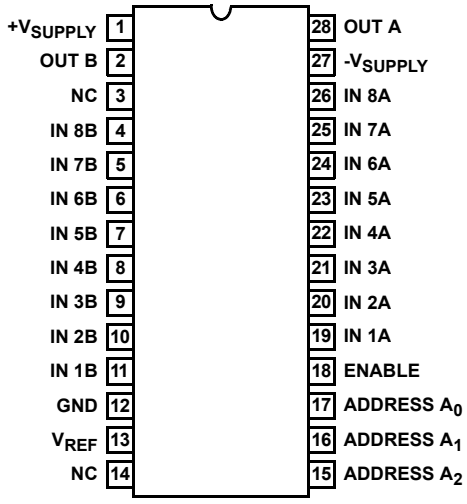
1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

Pinouts

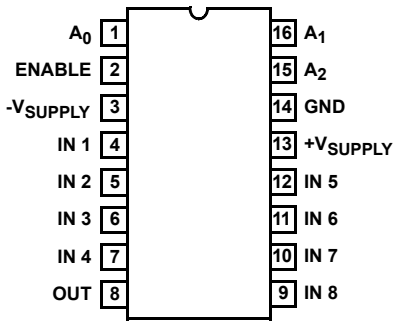
HI-506A (CERDIP, PDIP)
TOP VIEW



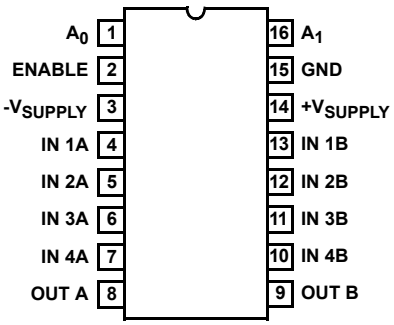
HI-507A (PDIP)
TOP VIEW



HI-508A (CERDIP, PDIP)
TOP VIEW



HI-509A (CERDIP, PDIP)
TOP VIEW



Truth Tables

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508A

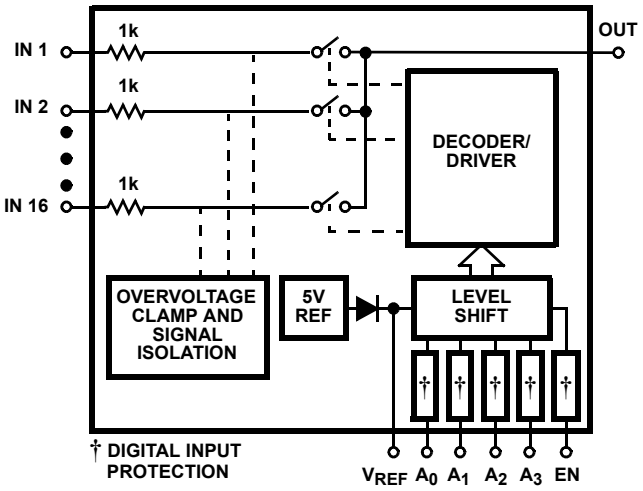
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

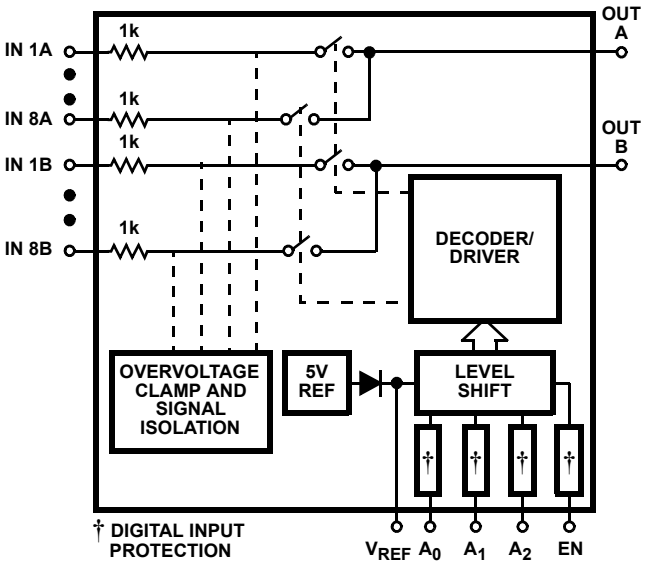
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Functional Diagrams

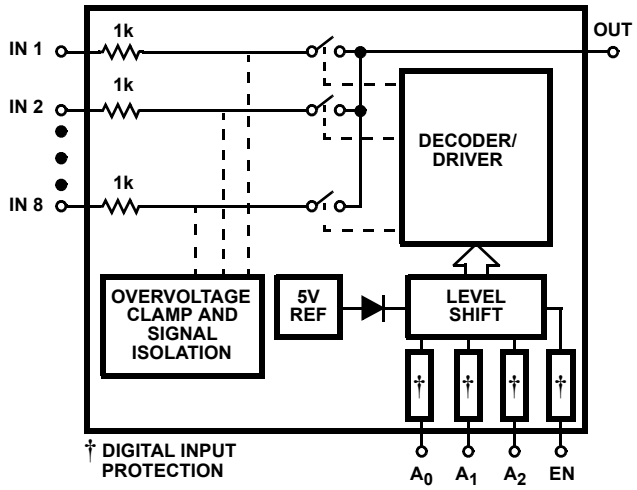
HI-506A



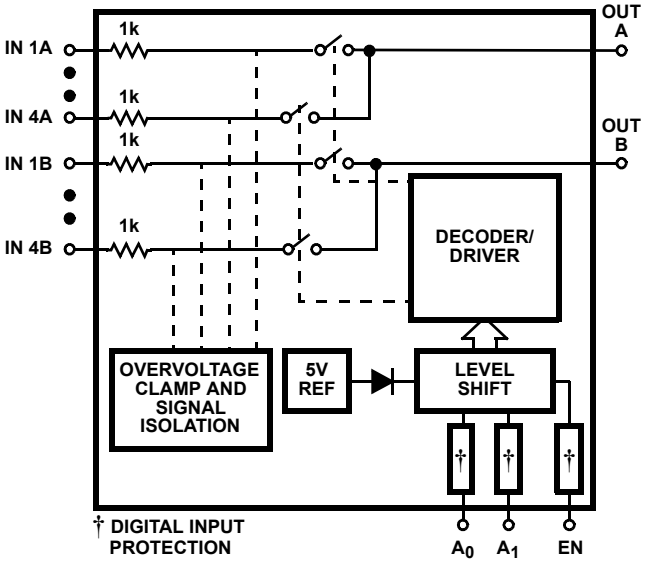
HI-507A



HI-508A

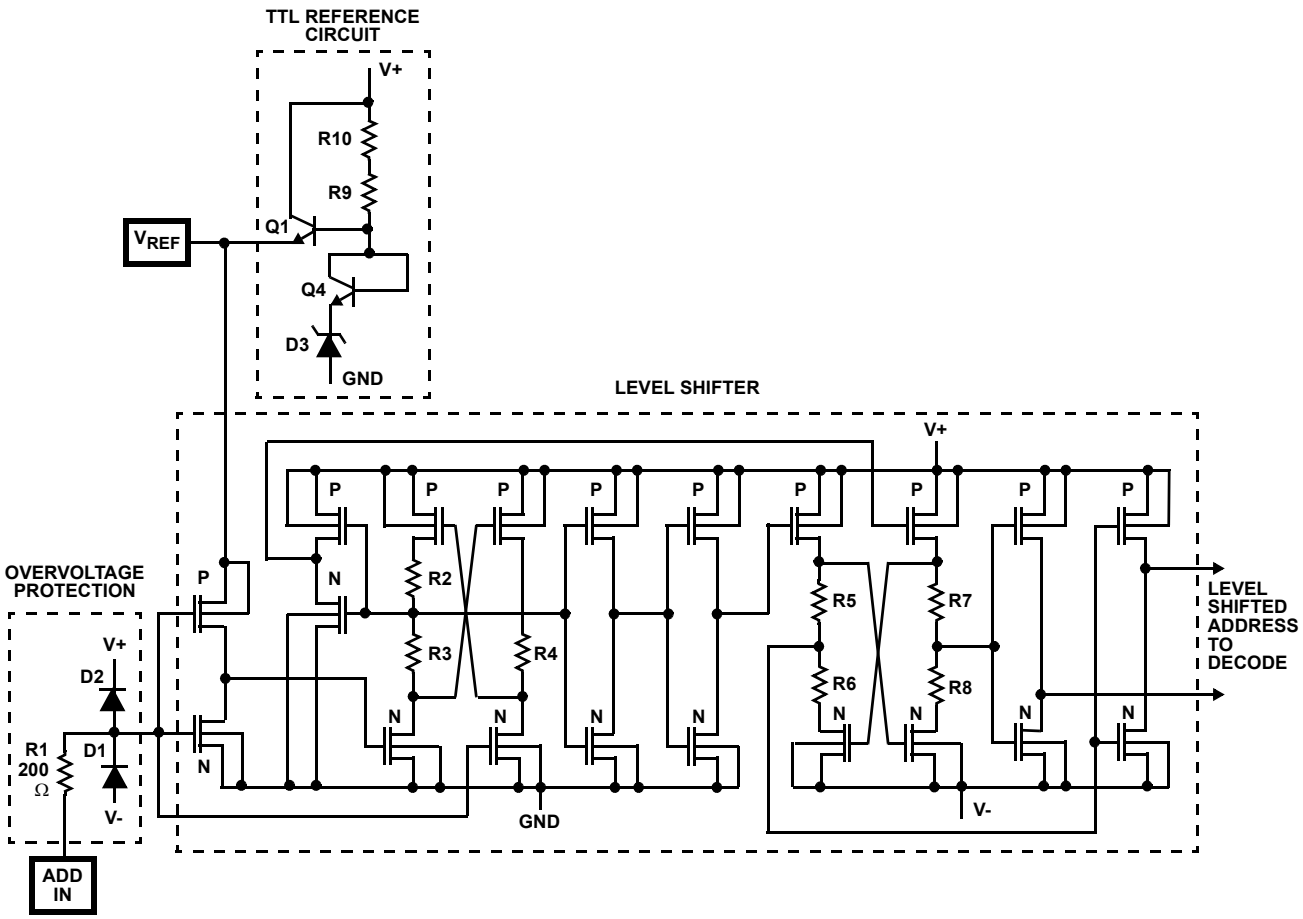


HI-509A

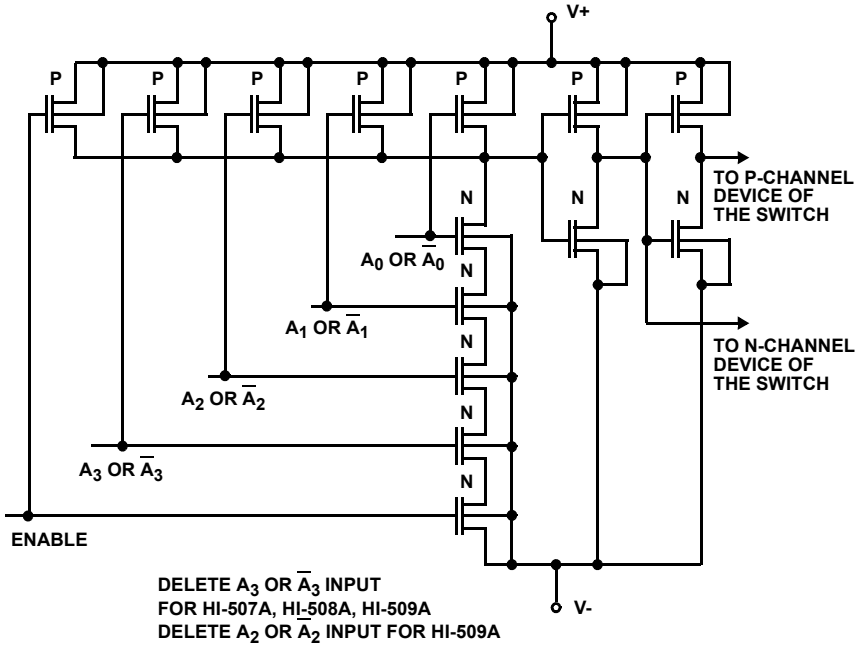


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

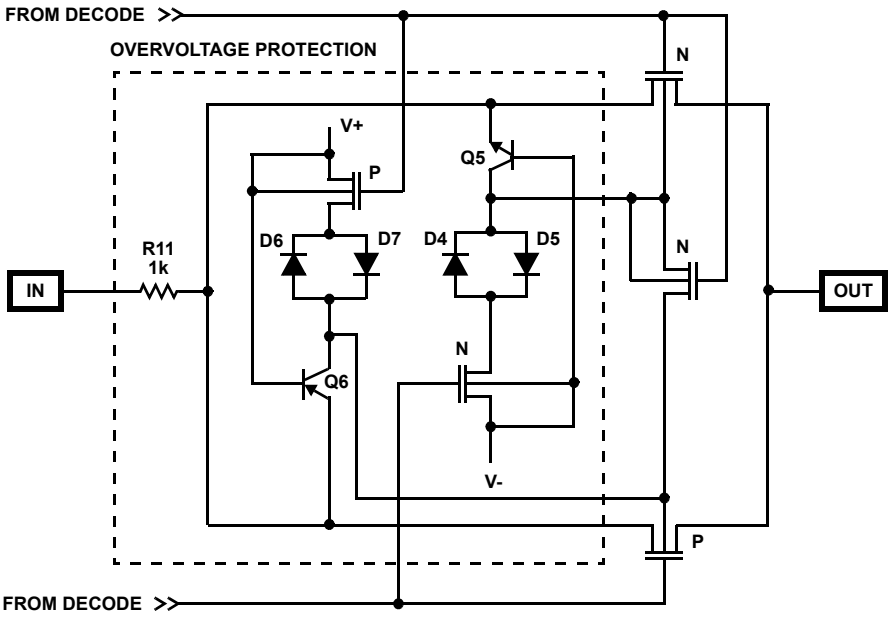


ADDRESS DECODER



Schematic Diagrams (Continued)

MULTIPLEX SWITCH



Absolute Maximum Ratings

V+ to V- . . . . . +44V
V+ to GND . . . . . +22V
V- to GND. . . . . -25V
Digital Input Voltage (V_{EN}, V_A) . . . . . (V-) -4V to (V+) +4V
or 20mA, Whichever Occurs First
Analog Signal (V_{IN}, V_{OUT}) . . . . . (V-) -20V to (V+) +20V
Continuous Current, IN or OUT 20mA
Peak Current, IN or OUT, Pulsed 1ms, 10% Duty Cycle (Max) . . 40mA

Operating Conditions

Temperature Ranges
HI-506A/507A/508A/509A-2, -8 . . . . . -55°C to +125°C
HI-506A/507A/508A/509A-5. . . . . 0°C to +75°C

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
28 Ld CERDIP Package	55	18
16 Ld CERDIP Package	75	22
28 Ld PDIP Package	60	N/A
16 Ld PDIP Package	90	N/A

Maximum Junction Temperature
CERDIP Packages . . . . . +175°C
PDIP Packages . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section.

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2, -8			-5			UNITS
			MIN (Note 12)	TYP	MAX (Note 12)	MIN (Note 12)	TYP	MAX (Note 12)	
DYNAMIC CHARACTERISTICS									
Access Time, t_A	Note 4	25	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before-Make Delay, t_{OPEN}	Note 4	25	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$	Note 4	25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$	Note 4	25	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time, t_S									
HI-506A and HI-507A	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	3.5	-	-	3.5	-	µs
HI-508A and HI-509A	To 0.1%	25	-	1.2	-	-	1.2	-	µs
	To 0.01%	25	-	3.5	-	-	3.5	-	µs
Off Isolation	Note 9	25	-	68	-	-	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		25	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$									
HI-506A		25	-	52	-	-	52	-	pF
HI-507A		25	-	30	-	-	30	-	pF
HI-508A		25	-	25	-	-	25	-	pF
HI-509A		25	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A		25	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		25	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}	Note 4	Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (Note 11)	Note 4	Full	4.0	-	-	4.0	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = 4V; V_{AL} (Logic Level Low) = 0.8V, Unless Otherwise Specified. For Test Conditions, Consult Test Circuits Section. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-2, -8			-5			UNITS
			MIN (Note 12)	TYP	MAX (Note 12)	MIN (Note 12)	TYP	MAX (Note 12)	
Input Leakage Current (High or Low), I_A	Notes 4, 8	Full	-	-	1.0	-	-	1.0	µA
MOS Drive, V_{AL}, HI-506A/HI-507A	V_{REF} = +10V	25	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH}, HI-506A/HI-507A	V_{REF} = +10V	25	6.0	-	-	6.0	-	-	V
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}	Note 4	Full	-15	-	+15	-15	-	+15	V
On Resistance, r_{ON}	Notes 4, 5	25	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
Off Input Leakage Current, $I_{S(OFF)}$	Notes 4, 6	25	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Notes 4, 6	25	-	0.1	-	-	0.1	-	nA
HI-506A		Full	-	-	300	-	-	300	nA
HI-507A		Full	-	-	200	-	-	200	nA
HI-508A		Full	-	-	200	-	-	200	nA
HI-509A		Full	-	-	100	-	-	100	nA
$I_{D(OFF)}$ With Input Overvoltage Applied	Note 7	25	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Notes 4, 6	25	-	0.1	-	-	0.1	-	nA
HI-506A		Full	-	-	300	-	-	300	nA
HI-507A		Full	-	-	200	-	-	200	nA
HI-508A		Full	-	-	200	-	-	200	nA
HI-509A		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF}, (HI-507A, HI-509A Only)		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Current, I+	Notes 4, 10	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Notes 4, 10	Full	-	0.02	1.0	-	0.02	1.0	mA
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW

NOTES:

4. 100% tested for Dash 8. Leakage currents not tested at -55°C.
5. V_{OUT} = ±10V, I_{OUT} = ∓100µA.
6. 10nA is the practical lower limit for high speed measurement in the production test environment.
7. Analog Overvoltage = ±33V.
8. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
9. V_{EN} = 0.8V, R_L = 1k, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
10. V_{EN}, V_A = 0V or 4V.
11. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5V supply are recommended.
12. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified

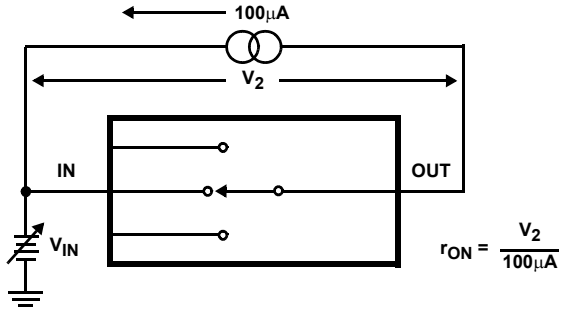


FIGURE 1A. TEST CIRCUIT

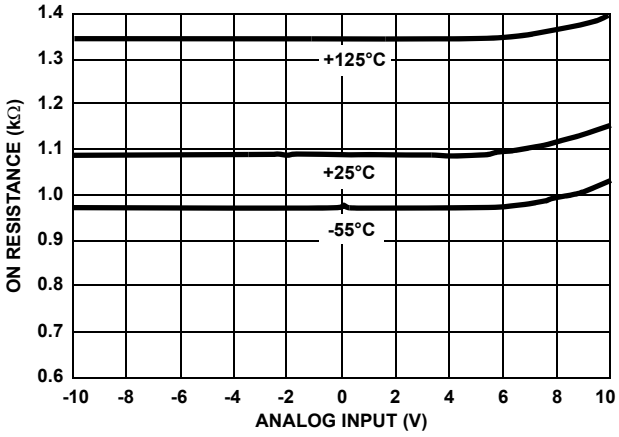


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

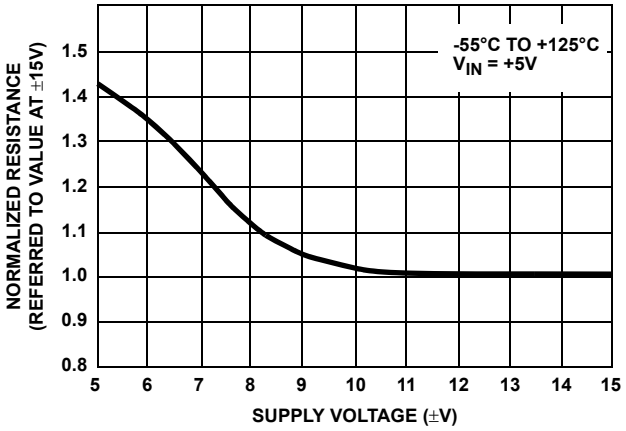


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

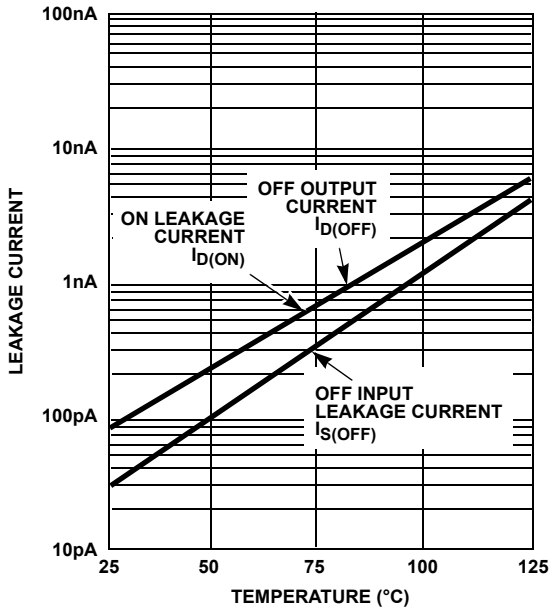


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

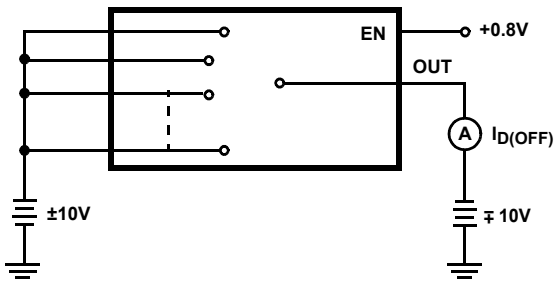


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 13)

Test Circuits and Waveforms

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

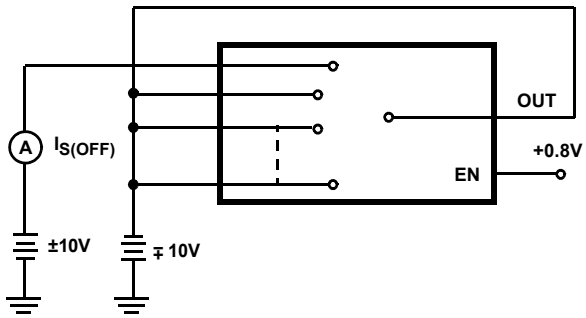


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 13)

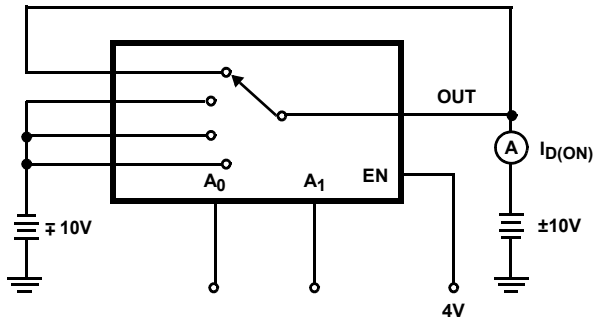


FIGURE 2D. $I_{D(On)}$ TEST CIRCUIT (NOTE 13)

NOTE:

13. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V.)

FIGURE 2. LEAKAGE CURRENTS

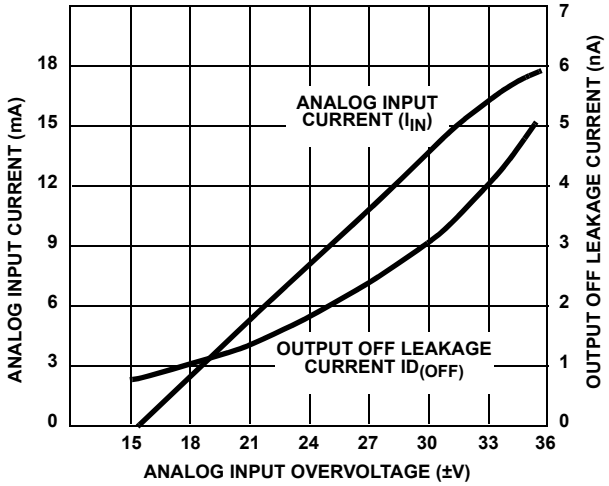


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

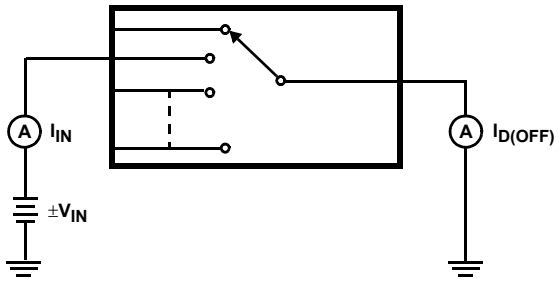


FIGURE 3B. TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

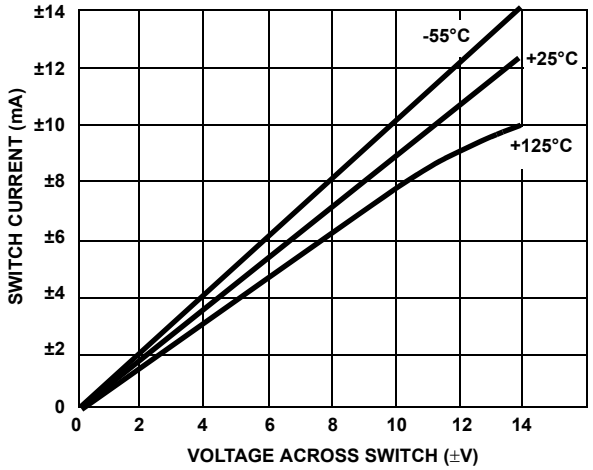


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

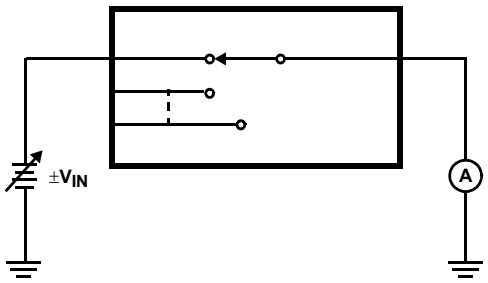


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Test Circuits and Waveforms

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

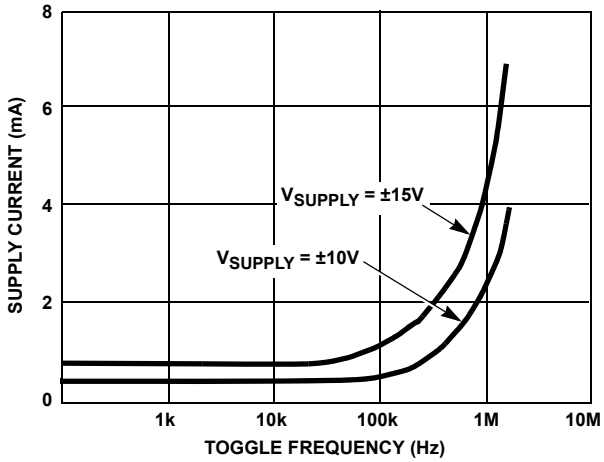
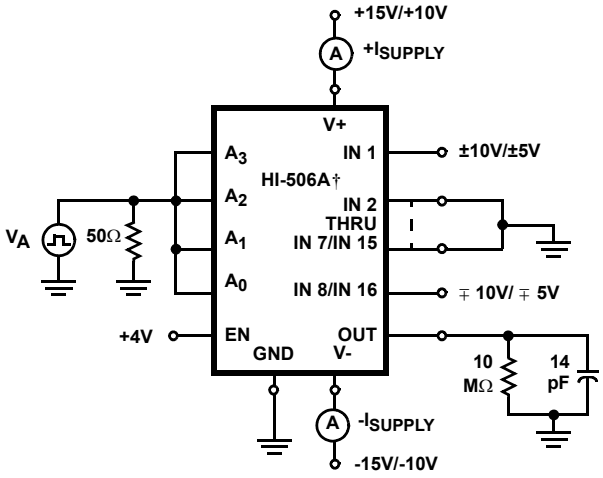


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 5B. TEST CIRCUIT

FIGURE 5. DYNAMIC SUPPLY CURRENT

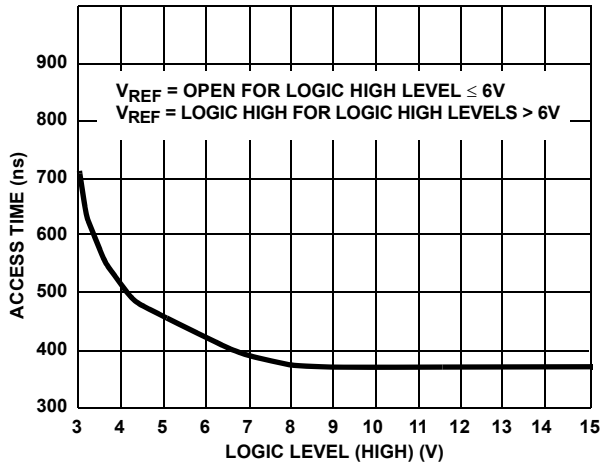
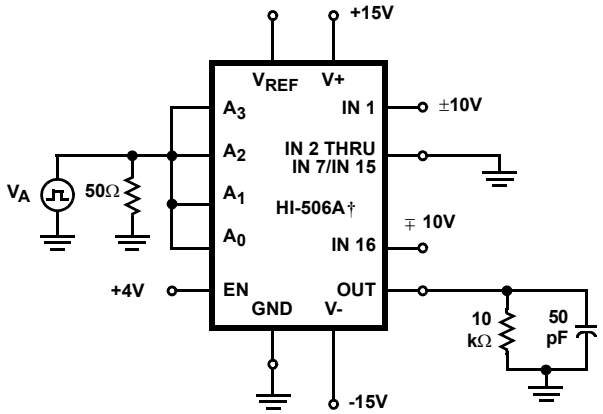


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-507A/HI-580A/HI-509A

FIGURE 6B. TEST CIRCUIT

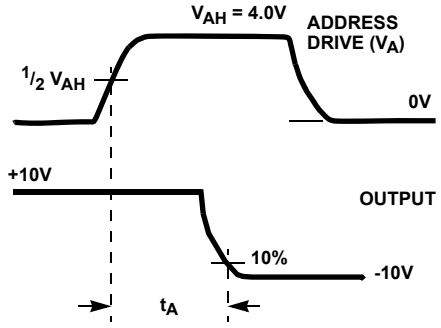


FIGURE 6C. MEASUREMENT POINTS

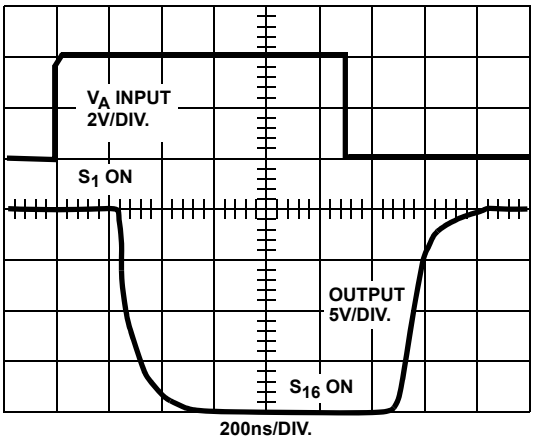
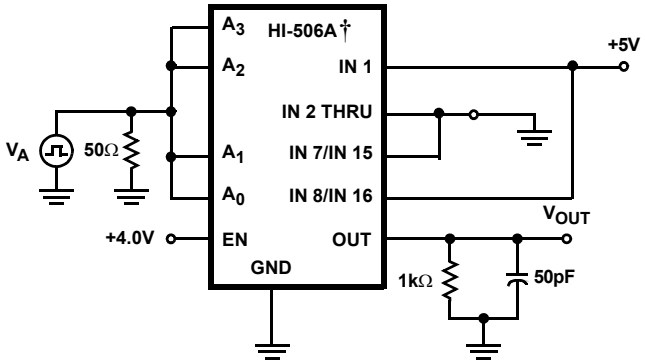


FIGURE 6D. WAVEFORMS

FIGURE 6. ACCESS TIME

Test Circuits and Waveforms

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 7A. TEST CIRCUIT

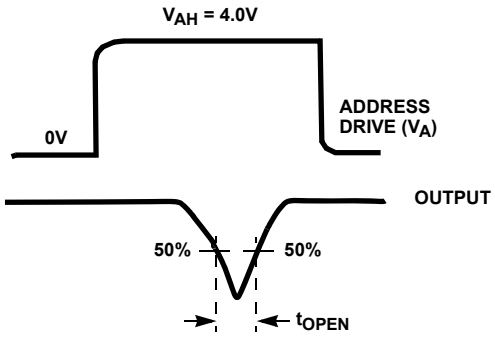


FIGURE 7B. MEASUREMENT POINTS

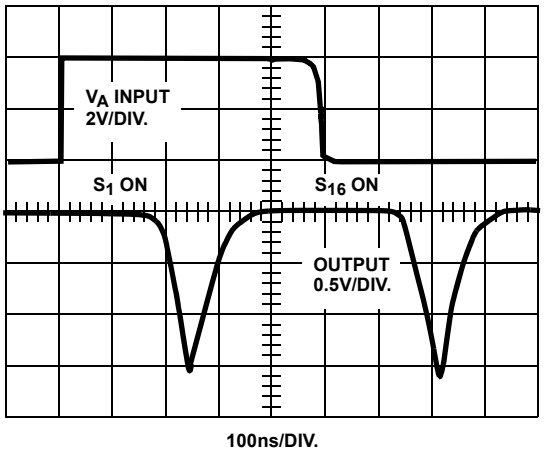
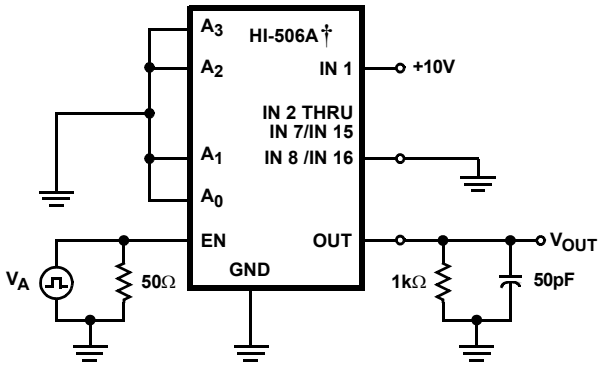


FIGURE 7C. WAVEFORMS

FIGURE 7. BREAK-BEFORE-MAKE DELAY

Test Circuits and Waveforms

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**



†Similar connection for HI-507A//HI-508A/HI-509A

FIGURE 8A. TEST CIRCUIT

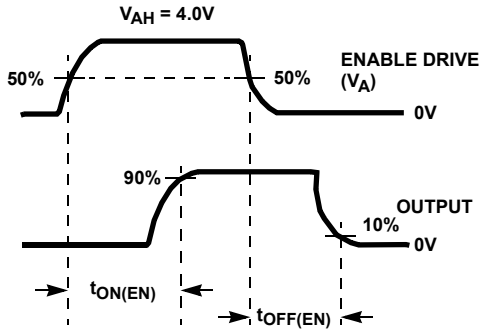


FIGURE 8B. MEASUREMENT POINTS

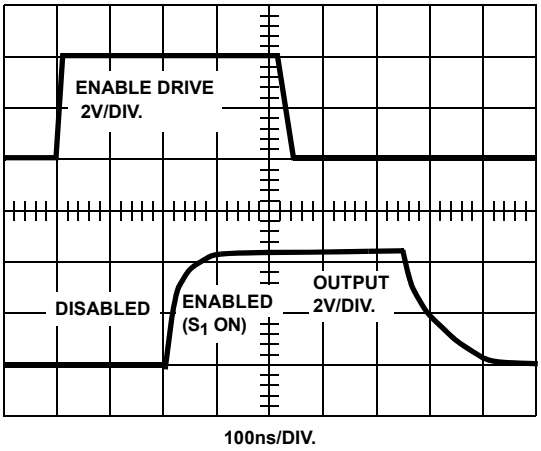


FIGURE 8C. WAVEFORMS

FIGURE 8. ENABLE DELAYS

Die Characteristics

DIE DIMENSIONS:

159 mils x 83.9 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

485

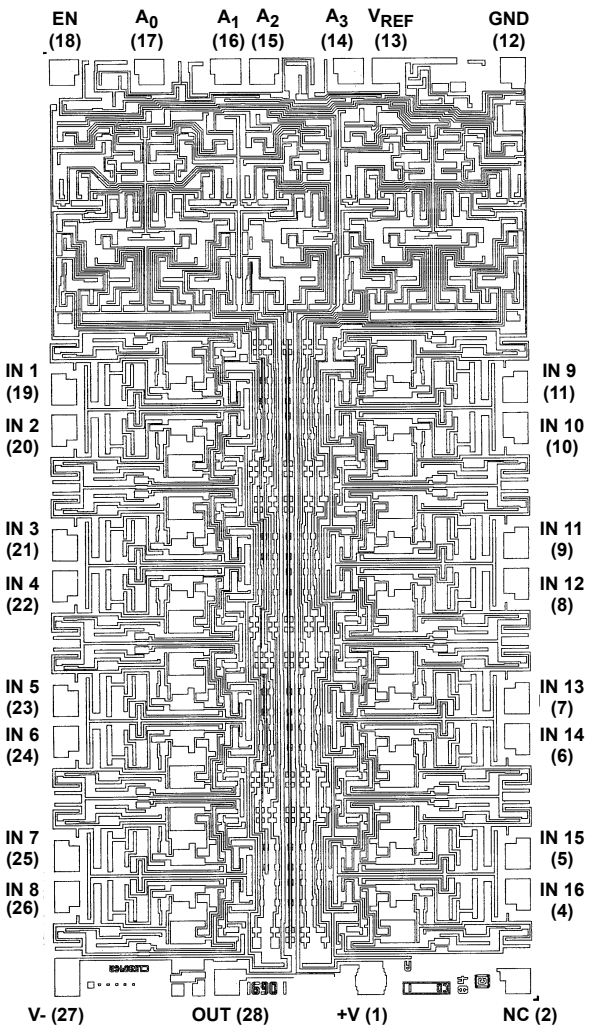
PROCESS:

CMOS-DI

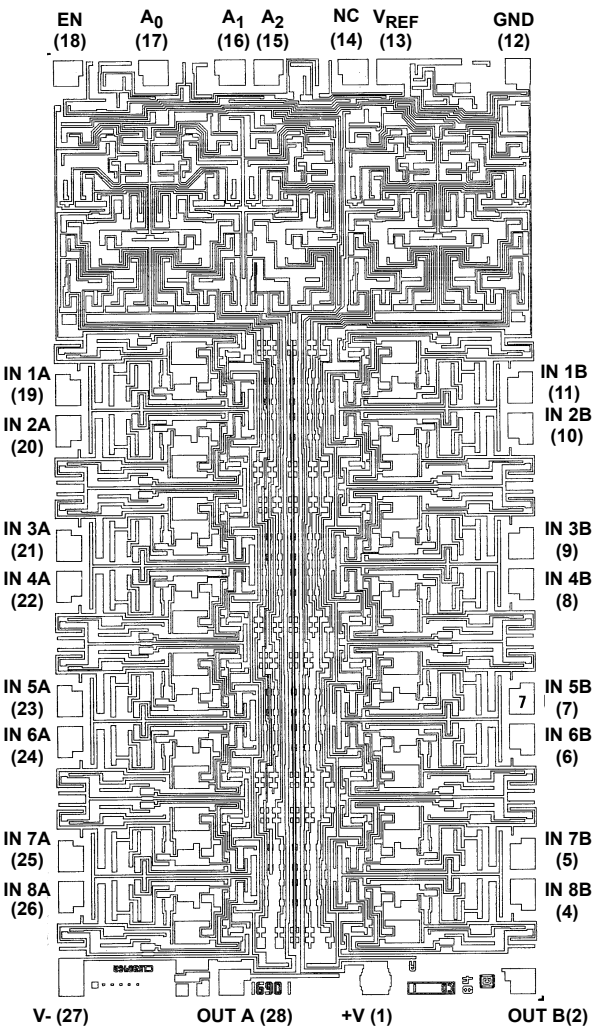
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

HI-506A



HI-507A



Die Characteristics

DIE DIMENSIONS:

108 mils x 83 mils

METALLIZATION:

Type: CuAl
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL (NOTE):

$-V_{SUPPLY}$

PASSIVATION:

Silox: 12kÅ ±2kÅ
Nitride: 3.5kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

1.4×10^5 A/cm^2

TRANSISTOR COUNT:

253

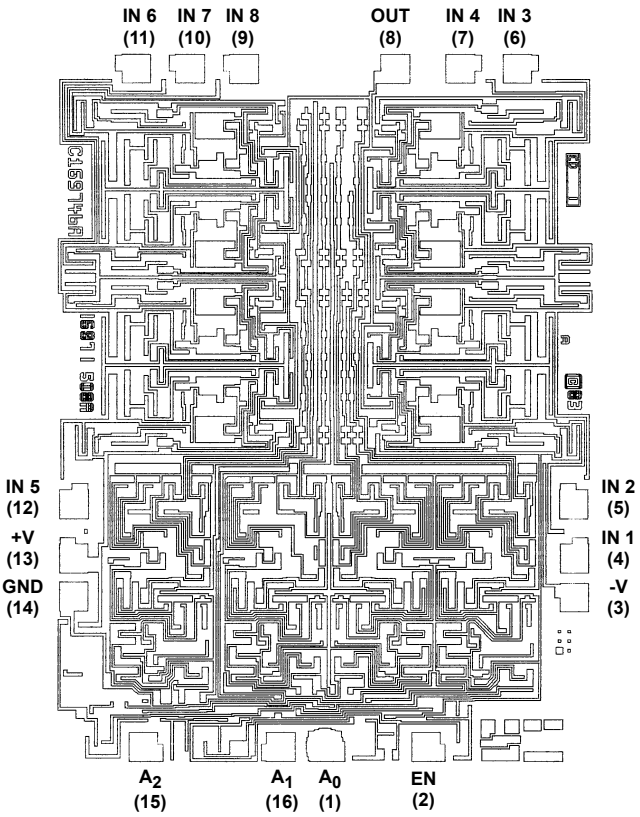
PROCESS:

CMOS-DI

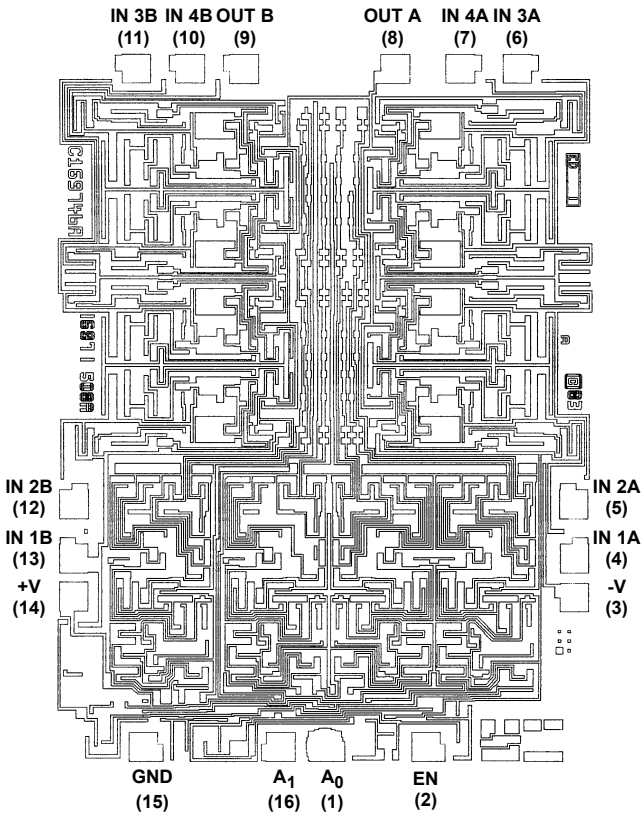
NOTE: The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layouts

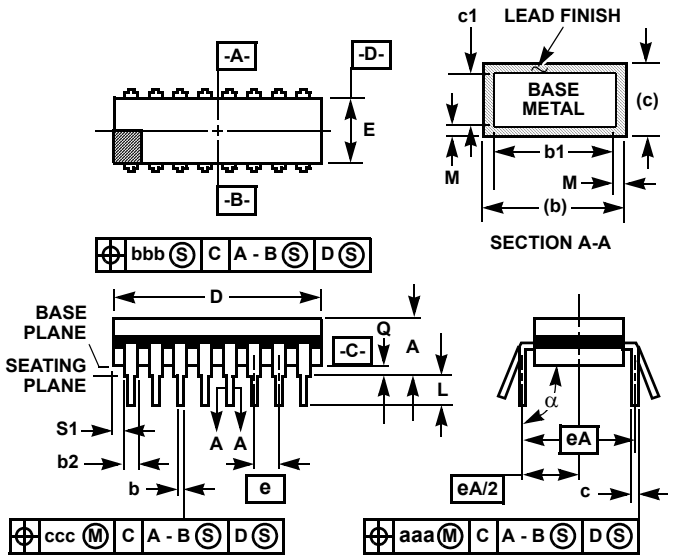
HI-508A



HI-509A



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

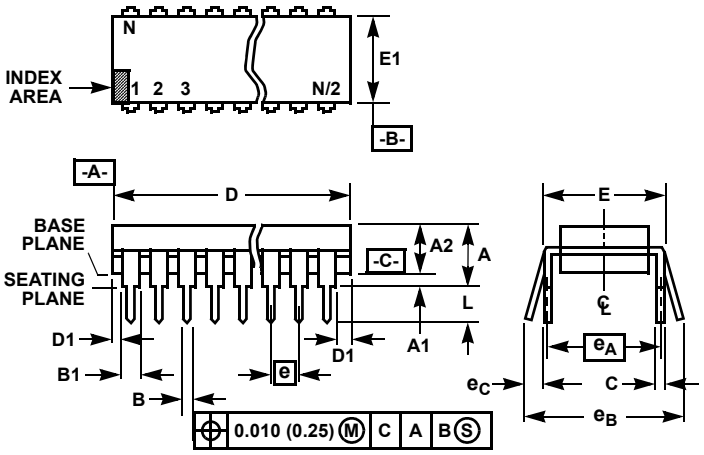
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	28		28		8

Rev. 0 4/94

Dual-In-Line Plastic Packages (PDIP)



NOTES:

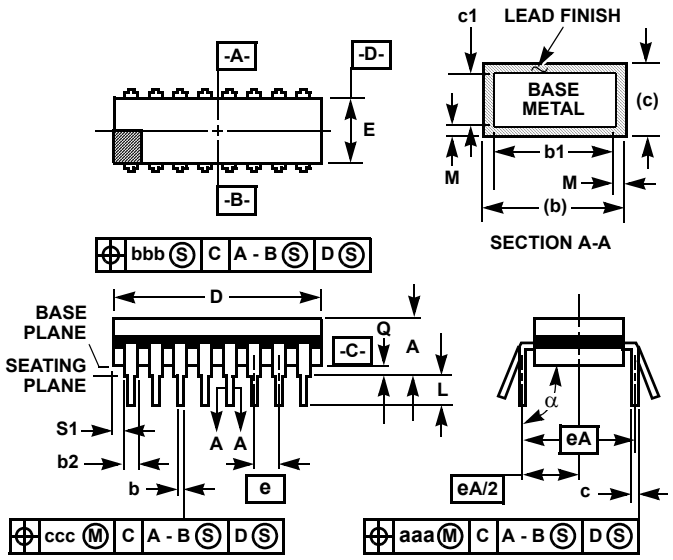
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 1 12/00

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

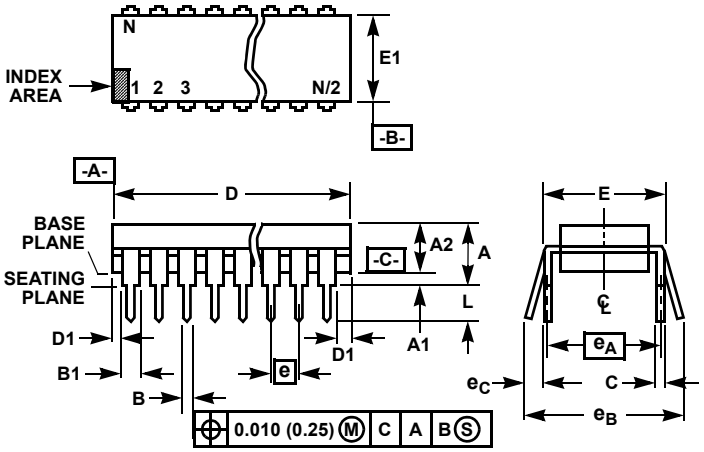
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93