HA-4741

Quad, 3.5MHz, Operational Amplifier

FN2922
Rev 5.00
July 2004

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/$\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (69dB at 10kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

HA-4741/883 product and data sheets available upon request.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA1-4741-2	-55 to 125	14 Ld CERDIP	F14.3
HA3-4741-5	0 to 75	14 Ld PDIP	E14.3

Features

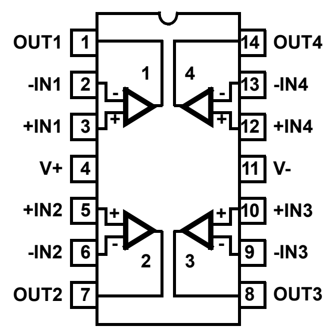
- Slew Rate 1.6V/µs
- Bandwidth 3.5MHz
- Input Voltage Noise . . . . 9nV/$\sqrt{Hz}$
- Input Offset Voltage 0.5mV
- Input Bias Current 60nA
- Supply Range. . . . . ±2V to ±20V
- No Crossover Distortion
- Standard Quad Pinout

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

Pinout

HA-4741 (PDIP, CERDIP)
TOP VIEW



Absolute Maximum Ratings

T_A = 25°C Unless Otherwise Stated
Supply Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 30V
Input Voltage . . . . V_{SUPPLY}
Output Short Circuit Duration (Note 3). . . . . Indefinite

Operating Conditions

Temperature Range:
HA-4741-2 . . . . -55°C to 125°C
HA-4741-5 . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package.	90	35
PDIP Package	107	N/A

Maximum Junction Temperature (Ceramic Package, Note 1) . . . . 175°C
Maximum Junction Temperature (Plastic Packages, Note 1) . . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175°C for the ceramic package, and below 150°C for the plastic packages.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. One amplifier may be shorted to ground indefinitely.

Electrical Specifications

V_{SUPPLY} = ±15V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-4741-2			HA-4741-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	0.5	3	-	1	5	mV
		Full	-	4	5	-	4	6.5	mV
Average Offset Voltage Drift		Full	-	5	-	-	5	-	μV/°C
Bias Current		25	-	60	200	-	60	300	nA
		Full	-	-	325	-	-	400	nA
Offset Current		25	-	15	30	-	30	50	nA
		Full	-	-	75	-	-	100	nA
Common Mode Range		Full	±12	-	-	±12	-	-	V
Differential Input Resistance		25	-	0.5	-	-	0.5	-	MΩ
Input Voltage Noise	f = 1kHz	25	-	9	-	-	9	-	nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 2kΩ	25	50	100	-	25	50	-	kV/V
		Full	25	-	-	15	-	-	kV/V
Common Mode Rejection Ratio		25	80	95	-	80	95	-	dB
		Full	74	-	-	74	-	-	dB
Channel Separation (Note 4)		25	66	69	-	66	69	-	dB
Small Signal Bandwidth		25	2.5	3.5	-	2.5	3.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 10kΩ	Full	±12	±13.7	-	±12	±13.7	-	V
Output Voltage Swing	R_L = 2kΩ	Full	±10	±12.5	-	±10	±12.5	-	V
Full Power Bandwidth (Notes 5, 6)		25	-	25	-	-	25	-	kHz
Output Current	V_{OUT} = ±10V	Full	±5	±15	-	±5	±15	-	mA
Output Resistance		25	-	300	-	-	300	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-4741-2			HA-4741-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE $R_L = 2k\Omega$, $C_L = 50pF$									
Rise / Fall Time	V_{OUT} = 0 to ±200mV	25	-	75	140	-	75	140	ns
Overshoot		25	-	25	40	-	25	40	%
Slew Rate	$V_{OUT} = \pm5V$	25	-	±1.6	-	-	±1.6	-	V/µs
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	4.5	5	-	5	7	mA
Power Supply Rejection Ratio	$\Delta V_S = \pm5V$	Full	80	95	-	80	95	-	dB

NOTES:

4. Referred to input; f = 10kHz, $R_S = 1k\Omega$, $V_{IN} = 100mV_{PEAK}$.
5. $V_{OUT} = \pm10V$, $R_L = 2k\Omega$.
6. Full power bandwidth guaranteed based upon slew rate measurement: FPBW = S.R./2π V_{PEAK}.

Test Circuit and Waveforms

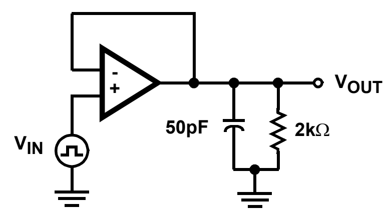
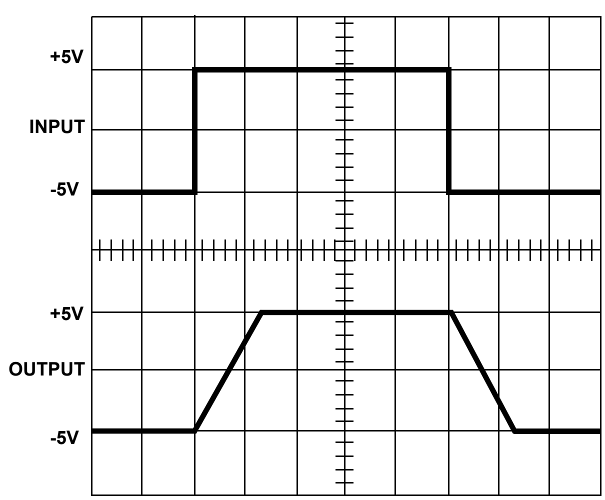
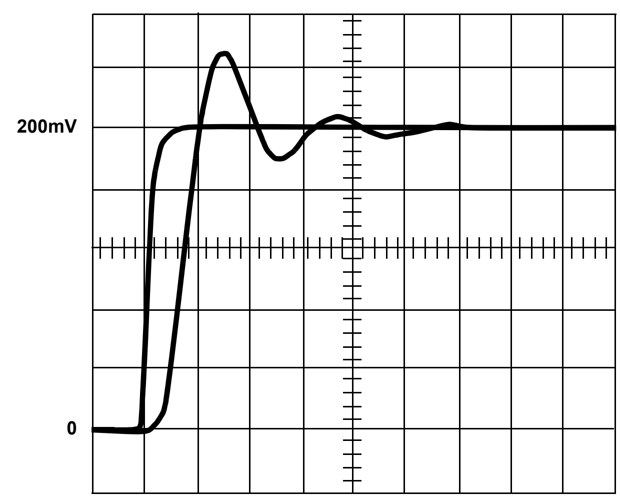


FIGURE 1. SMALL AND LARGE SIGNAL TEST CIRCUIT



Volts = 5V/Div., Time = 5µs/Div.

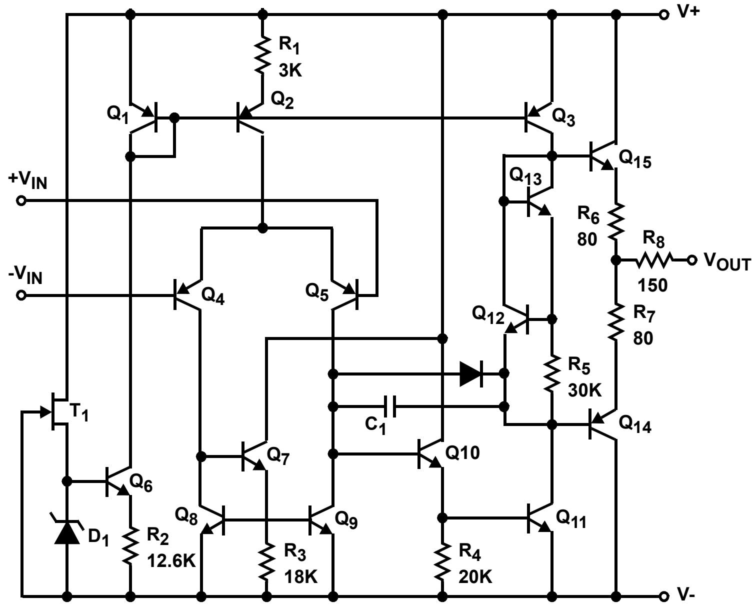
FIGURE 2. LARGE SIGNAL RESPONSE



Volts = 40mV/Div., Time = 100ns/Div.

FIGURE 3. SMALL SIGNAL RESPONSE

Schematic Diagram



Typical Performance Curves

V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified

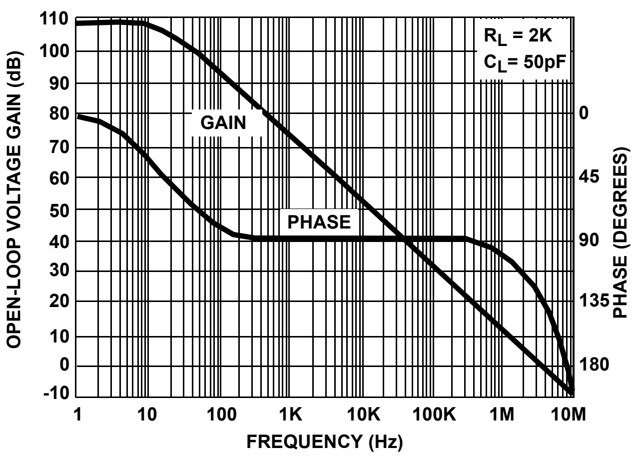


FIGURE 4. OPEN LOOP FREQUENCY RESPONSE

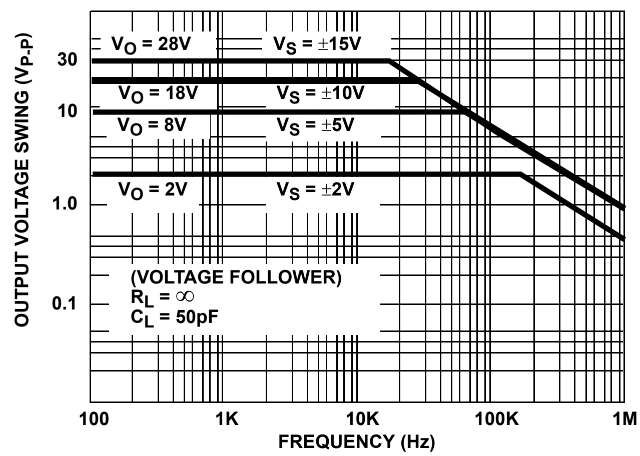


FIGURE 5. OUTPUT VOLTAGE SWING vs FREQUENCY

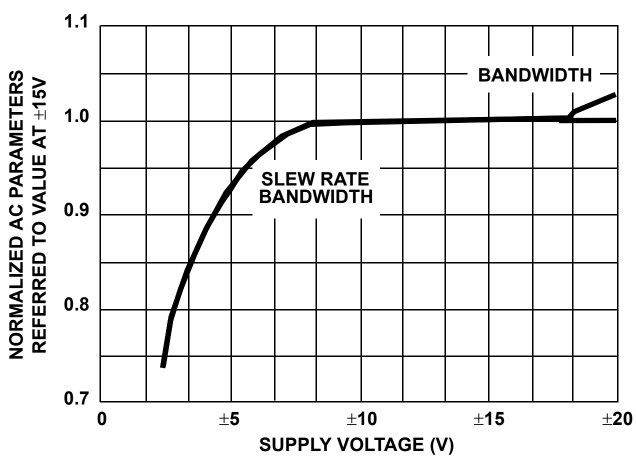


FIGURE 6. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

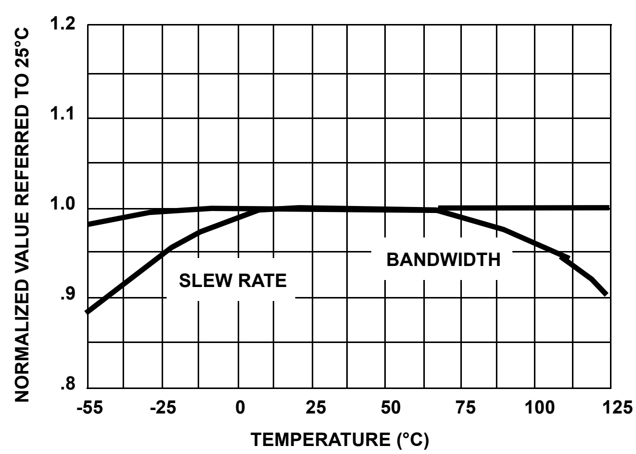


FIGURE 7. NORMALIZED AC PARAMETERS vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

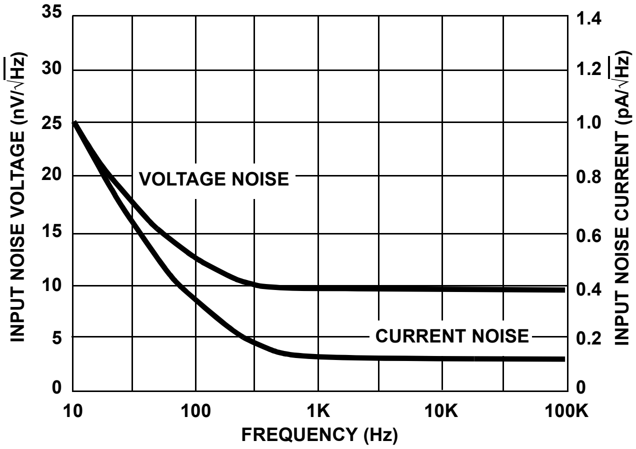


FIGURE 8. INPUT NOISE vs FREQUENCY

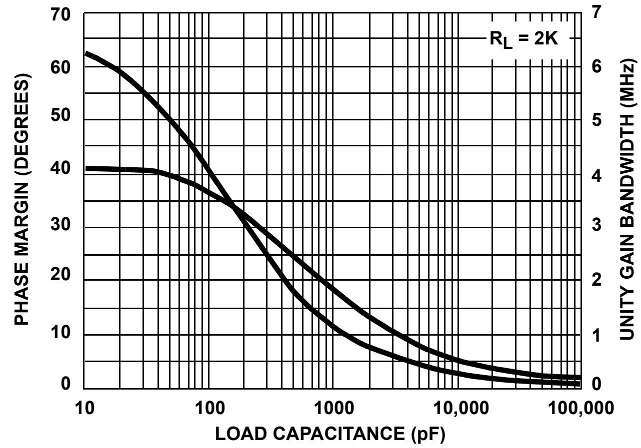


FIGURE 9. SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE

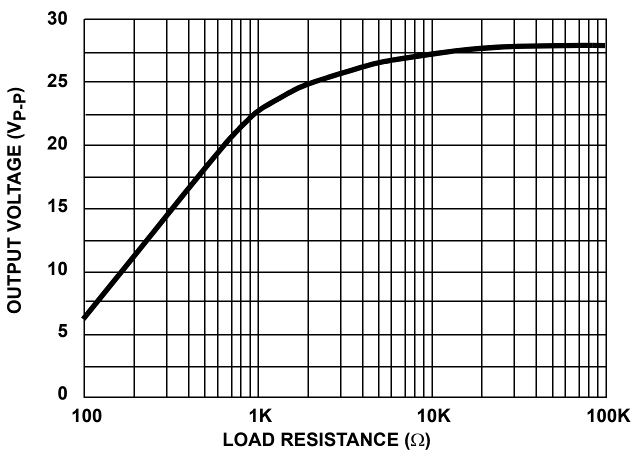


FIGURE 10. MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

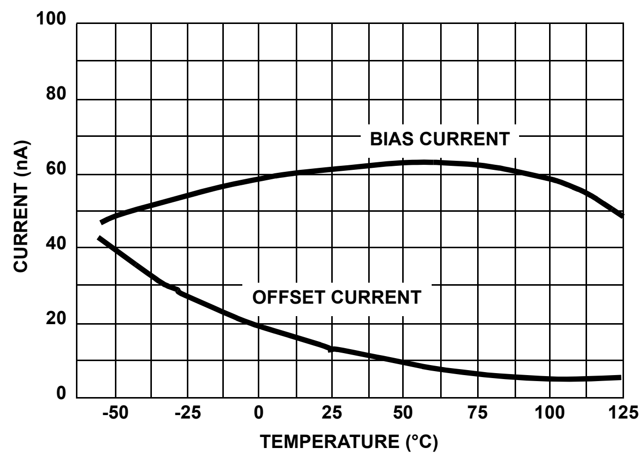


FIGURE 11. INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

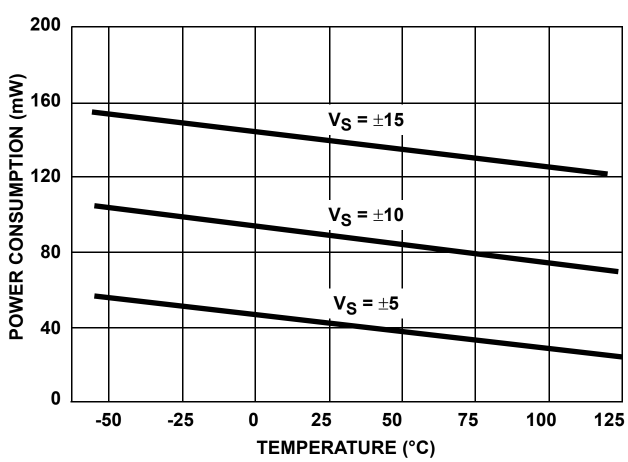


FIGURE 12. POWER CONSUMPTION vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

87 mils x 75 mils x 19 mils
2210µm x 1910µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (POWERED UP):

V-

TRANSISTOR COUNT:

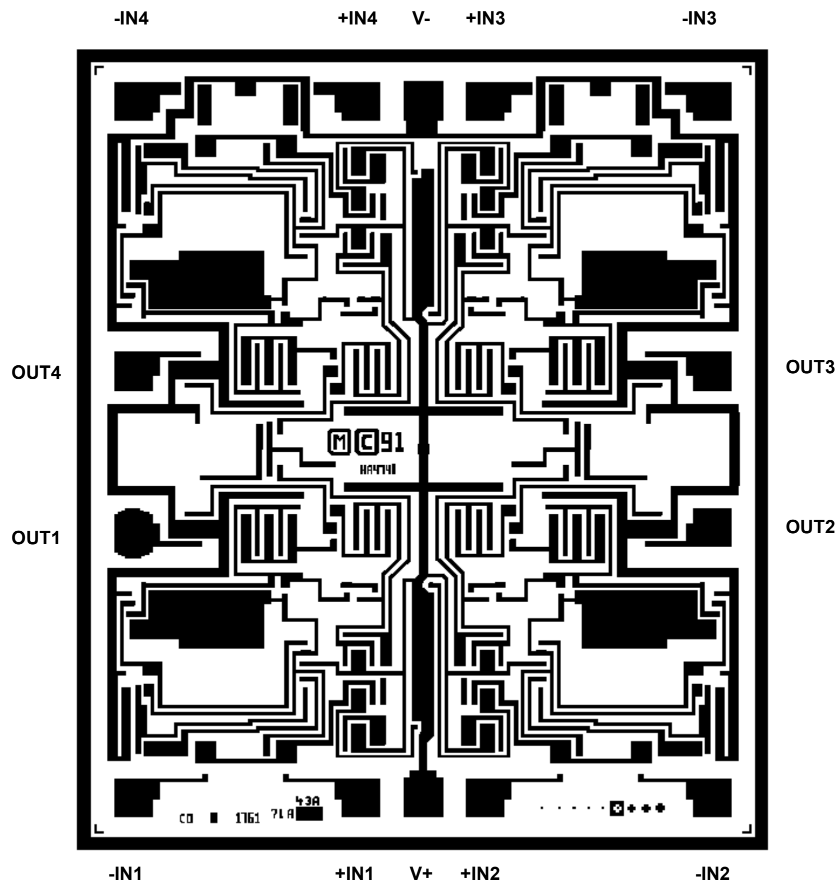
72

PROCESS:

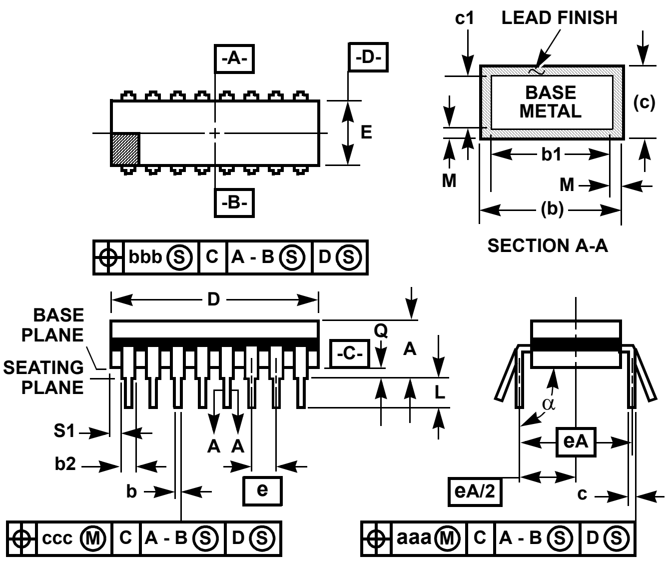
Junction Isolated Bipolar/JFET

Metallization Mask Layout

HA-4741



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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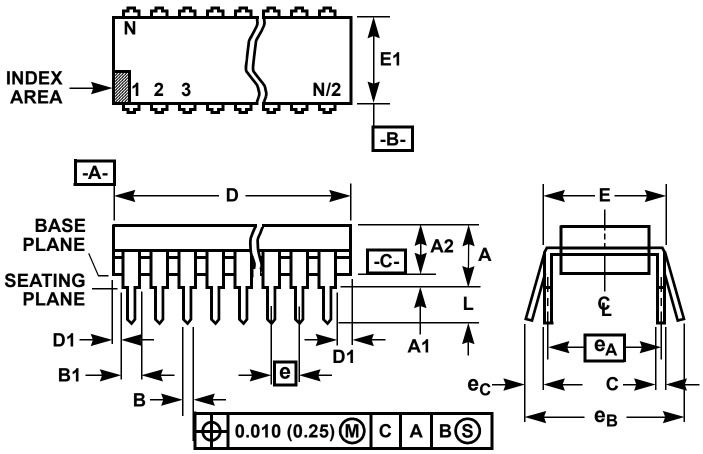
Dual-In-Line Plastic Packages (PDIP)



E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{\text{-C-}}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).