EL4093

300MHz DC-Restored Video Amplifier

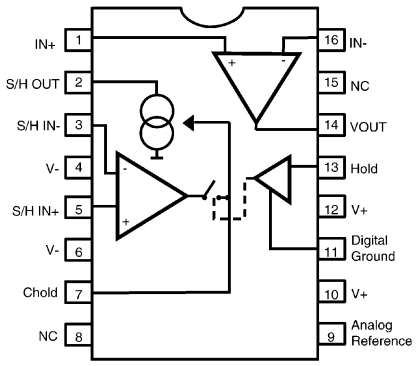
FN7159
Rev 0.00
January 1996

The EL4093 is a complete DC-restored video amplifier subsystem, featuring low power consumption and high slew rate. It contains a current feedback amplifier and a sample and hold amplifier designed to stabilize video performance. When the HOLD logic input is low, the sample and hold may be used as a general purpose op amp to null the DC offset of the video amplifier. When the HOLD input goes high the sample and hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent video scan line.

The sample and hold amplifier contains a current output stage that greatly simplifies its connection to the video amplifier. Its high output impedance also helps to preserve video linearity at low supply voltages. For ease of interfacing, the HOLD input is TTL-compatible. This device has an operational temperature of -40°C to +85°C and is packaged in plastic 16-pin DIP and 16-pin SOIC.

Pinout

EL4093
(16-PIN PDIP, SO)
TOP VIEW



Features

- High accuracy DC restoration for video
- Low supply current of 9.5mA typ.
- 300MHz bandwidth
- 1500V/µs slew rate
- 0.04% differential gain and 0.02° differential phase into 150Ω for NTSC
- 1.5mV max. restored DC offset
- Sample and hold amplifier with fast enable and low leakage
- TTL-compatible HOLD logic input

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE	PKG. NO.
EL4093CN	-40°C to +85°C	16-Pin PDIP	MDP0031
EL4093CS	-40°C to +85°C	16-Pin SOIC	MDP0027

Demo Board

A demo PCB is available for this product. Request “EL4093 Demo Board.”

Absolute Maximum Ratings (T_A = 25°C)

V_S V+ to V- Supply Voltage 12.6V
V_{HOLD} Voltage at HOLD input (DGND-0.7) to (DGND+5.5V)
V_{IN} Voltage at any other input . . . . . V+ to V-
ΔV_{IN} Difference between Sample and Hold inputs . . . . . .±8V
I_{OUT1} Video amplifier output current . . . . . ±30mA
I_{OUT2} S/H amplifier output current . . . . . ±10mA
I_{IN} Maximum current into other pins. . . . . ±6mA
P_D Maximum Power Dissipation. . . . . See Curves
T_A Operating Ambient Temperature Range. . . . . -40°C to +85°C
T_J Operating Junction Temperature . . . . . 150°C
T_{ST} Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Open-Loop DC Electrical Specifications

Power supplies at ±5V, T_A = 25°C

Sample and Hold

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
$I_{S,HOLD}$	Total Supply current in HOLD mode		9.5	11.5	mA
$I_{S,SAMPLE}$	Total Supply current in SAMPLE mode		8.5	10.5	mA

Video Amplifier Section (Not Restored)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		10	110	mV
I_B+	Non-Inverting Input Bias Current		10	25	µA
I_B-	Inverting Input Bias Current		15	50	µA
R_{OL}	Transimpedance, V_{OUT} = ±2.5V, R_L = 150Ω	150	400		kΩ
V_O	Output Voltage Swing, R_L = 150Ω	±3	±3.5		V
I_{SC}	Output Short-Circuit Current	60	100		mA

Open-Loop DC Electrical Specifications

Power supplies at ±5V, T_A = 25°C

Sample and Hold Section

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		0.5	1.5	mV
TCV_{OS}	Average Offset Voltage Drift		6		µV/°C
I_B	Input Bias Current		1	2	µA
I_{OS}	Input Offset Current		10	200	nA
TCI_{OS}	Average Offset Current Drift		0.1		nA/°C
V_{CM}	Common Mode Input Range	±2.5	±2.8		V
g_M	Transconductance (R_L = 500Ω)	5	15		A/V
CMRR	Common Mode Rejection Ratio (V_{CM} -2.5V to +2.5V)	70	90		dB
V_{IL}	HOLD Logic Input Low (referenced to Digital GND)			0.8	V
V_{IH}	HOLD Logic Input High (referenced to Digital GND)	2.0			V
V_{GND}	Digital GND Reference Voltage	(V-)		(V+) - 4.0	V
I_{DROOP}	Hold Mode Droop Current		10	70	nA
I_{CHARGE}	Charge Current Available to C_{HOLD}	±5.5	±8.5		mA
V_O	Output Voltage Swing (R_L = 10kΩ)	±3	±3.5		V
I_O	Output Current Swing (R_L = 0Ω)	±4.5	±5.5		mA

Closed-Loop AC Electrical Specifications

Power supplies at ±5V, T_A = 25°C, R_F = R_G = 750Ω, R_L = 150Ω, C_L = 5pF, C_{IN}- (parasitic) = 1.8pF

Video Amplifier Section

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
BW, -3dB	-3dB Small-Signal Bandwidth		300		MHz
BW, ±0.1dB	0.1dB Flatness Bandwidth		50		MHz
Peaking	Frequency Response Peaking		0		dB
SR	Slew rate, V_{OUT} between -2V and +2V		1500		V/µs
dG	Differential Gain Error, Voffset between -714mV and +714mV		0.04		%
dθ	Differential Phase Error, Voffset between -714mV and +714mV		0.02		°

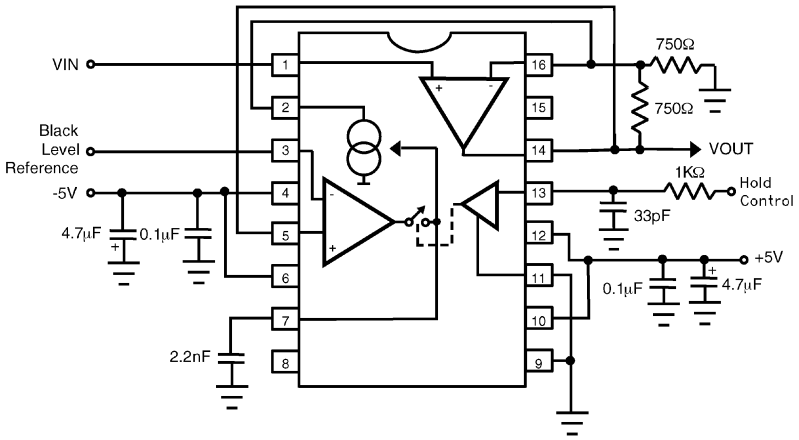
Closed-Loop AC Electrical Specifications

Power supplies at ±5V, T_A = 25°C, R_F = R_G = 750Ω, R_L = 150Ω, C_L = 5pF, C_{HOLD} = 2.2nF

Sample and Hold Section

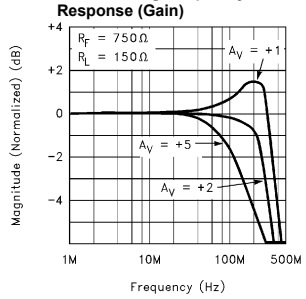
PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
ΔI_{STEP}	Change in Sample to Hold Output Current Due to Hold Step		0.1		µA
ΔT_{SH}	Sample to Hold Delay Time		15		ns
ΔT_{HS}	Hold to Sample Delay Time		40		ns
T_{AC}	Settling Time to 1% (DC Restored Amplifier Output) Video Amplifier Input from 0 to 1V		2.2		µs

Typical Application

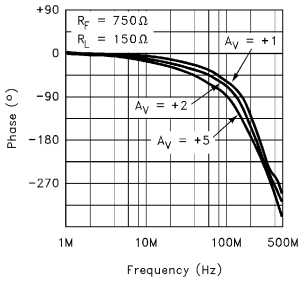


Typical Performance Curves

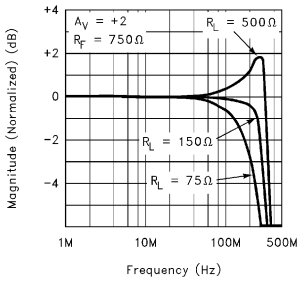
Non-inverting Frequency Response (Gain)



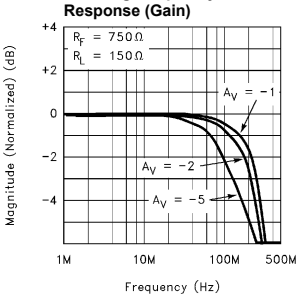
Non-inverting Frequency Response (Phase)



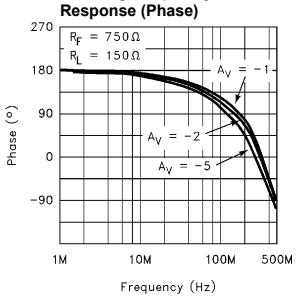
Frequency Response for Various R_L



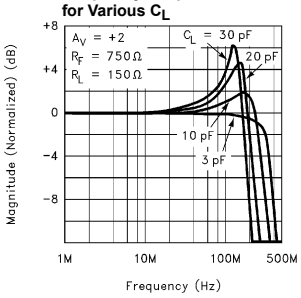
Inverting Frequency Response (Gain)



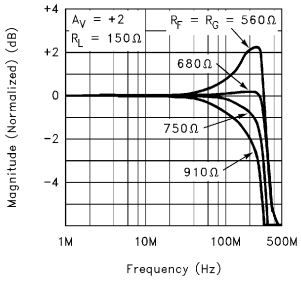
Inverting Frequency Response (Phase)



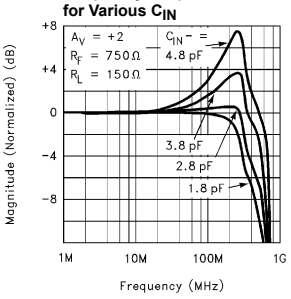
Frequency Response for Various C_L



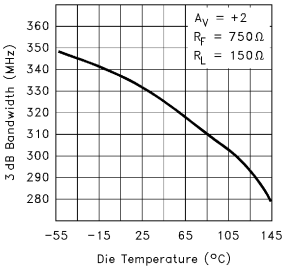
Frequency Response for Various R_F and R_G



Frequency Response for Various C_{IN}

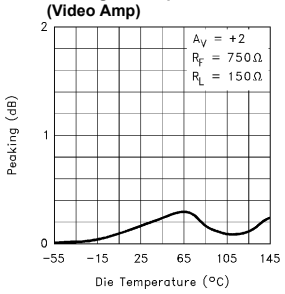


3dB Bandwidth vs Temperature (Video Amp)

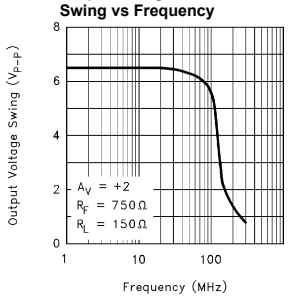


Typical Performance Curves (Continued)

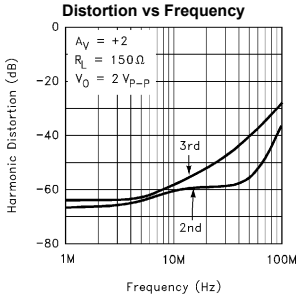
Peaking vs Temperature (Video Amp)



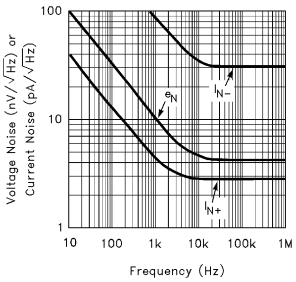
Output Voltage Swing vs Frequency



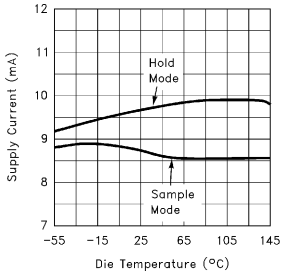
2nd and 3rd Harmonic Distortion vs Frequency



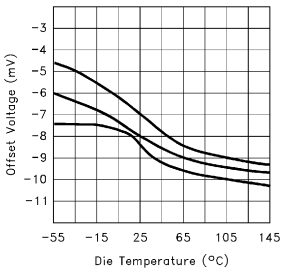
Voltage and Current Noise vs Frequency



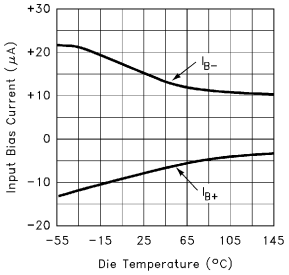
Supply Current vs Temperature



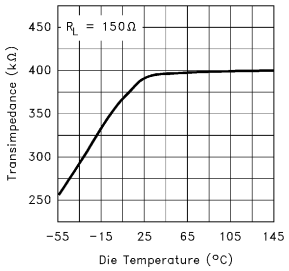
Input Offset Voltage vs Die Temperature (Video Amp, 3 Sample)



Input Bias Current vs Temperature (Video Amp)

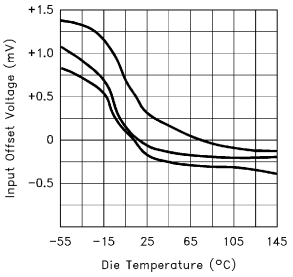


Transimpedance vs Temperature (Video Amp)

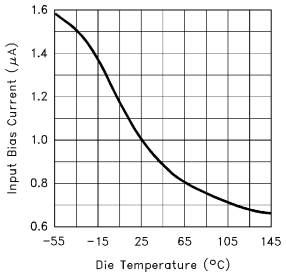


Typical Performance Curves (Continued)

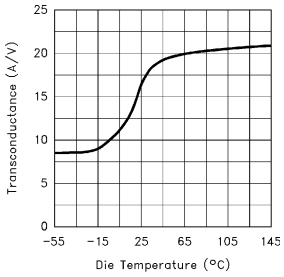
Input Offset Voltage vs Die Temperature (Sample & Hold, 3 Samples)



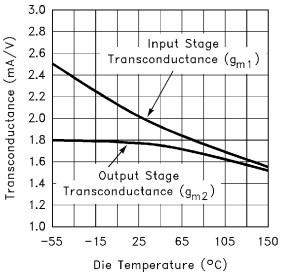
Input Bias Current vs Die Temperature (Sample & Hold)



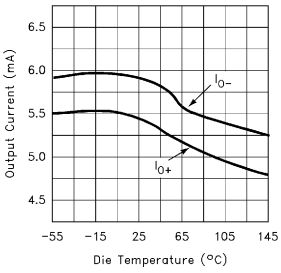
Transconductance vs Temperature (Sample & Hold)



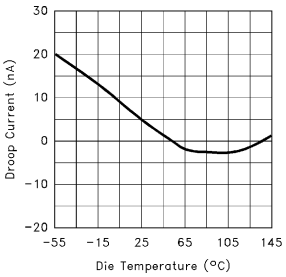
Transconductance vs Die Temperature (Sample & Hold)



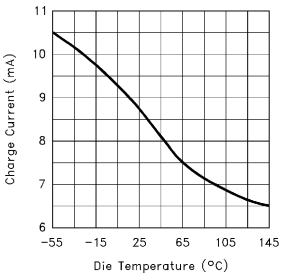
Output Current Swing vs Temperature (Sample & Hold)



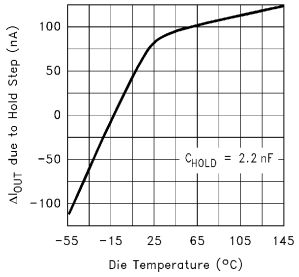
Droop Current vs Temperature (Sample & Hold)



Charge Current vs Temperature (Sample & Hold)

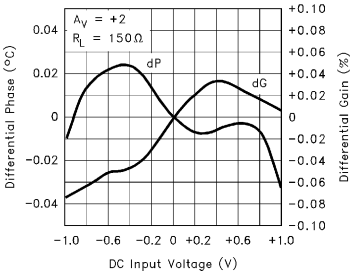


Hold Step (ΔI_{OUT}) vs Temperature



Typical Performance Curves (Continued)

Differential Gain and Phase vs DC Input Voltage at 3.58MHz



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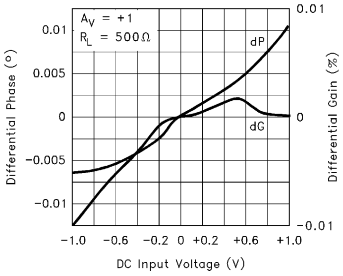
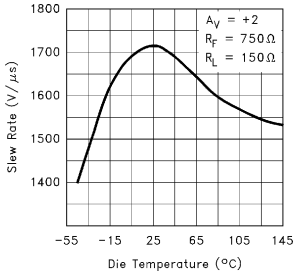
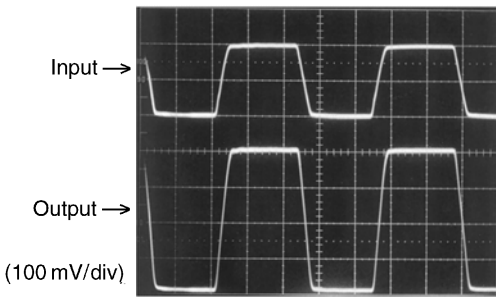


Slew Rate vs Die Temperature (Video Amp)

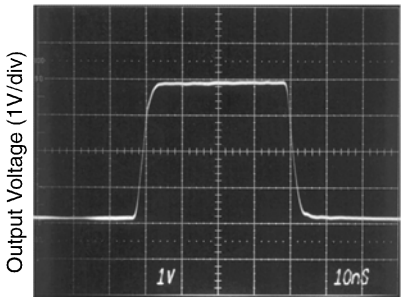


Small-Signal Step Response



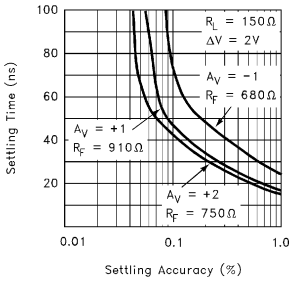
$A_V = +2,\ R_F = R_G = 750\Omega,\ R_L = 150\Omega$

Large-Signal Step Response

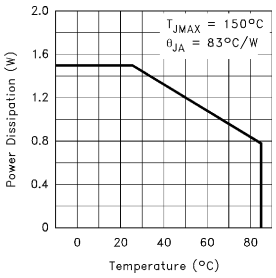


$A_V = +2,\ R_F = R_G = 750\Omega,\ R_L = 150\Omega$

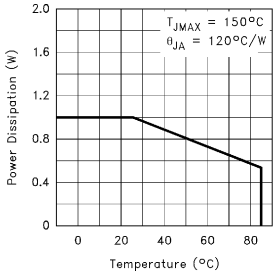
Settling Time vs Settling Accuracy (Video Amp)



Maximum Power Dissipation vs Ambient Temperature, 16-Pin PDIP Package



Maximum Power Dissipation vs Ambient Temperature, 16-Pin SO Package



Applications Information

Product Description

The EL4093 is a high speed DC-restore system containing a current feedback amplifier (CFA) and a sample & hold (S/H) amplifier. The CFA offers a wide 3dB bandwidth of 300MHz and a slew rate of 1500V/µs, making it ideal for high speed video applications such as SVGA. The CFA's excellent differential gain and phase at 3.58MHz also makes it suitable for NTSC applications. Drawing only 9.5mA on ±5V supplies, the EL4093 serves as an excellent choice for those applications requiring both low power and high bandwidth.

The connection between the CFA and sample & hold (the Autozero interface) has been greatly simplified. The output of the sample & hold is a high impedance current source, allowing direct connection to the CFA inverting input for autozero purposes. In addition, special circuitry within the sample & hold provides a charge current of 8.5mA in sample mode, resulting in a sample hold current ratio (ratio of charging current to droop current) of approx. 1,000,000.

Theory of Operation

In video applications, DC restoration moves the backporch or black level to a fixed DC reference. The EL4093 uses a CFA in feedback with a sample & hold to provide DC restoration.

Figure 1 shows how the two are connected to provide this function; the S/H compares the output of the CFA to a DC reference, and any difference between them causes an output current from the S/H. This “autozero” current is fed to the CFA inverting input, the effect of which is to move the CFA output towards the reference voltage. This autozero mechanism settles when the CFA output is one V_{OS} away from the reference (the V_{OS} here refers to the S/H offset voltage).

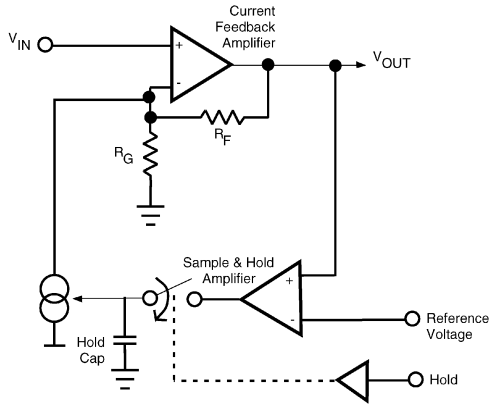


FIGURE 1.

The autozero mechanism is typically active for only a short period of each video line. Figure 2 shows a NTSC video signal along with the EL4581 back porch output. The back porch signal is used to drive the HOLD input of the EL4093, and we see that the EL4093 is in sample mode for only 3.5µs of each line. It is during this time that the autozero mechanism attempts to drive the CFA output towards the reference voltage, at the same time putting a correction voltage onto the hold capacitor C_{HOLD}. During the rest of the line (60µs) the EL4093 is in hold mode, but DC correction is maintained by the voltage on C_{HOLD}.

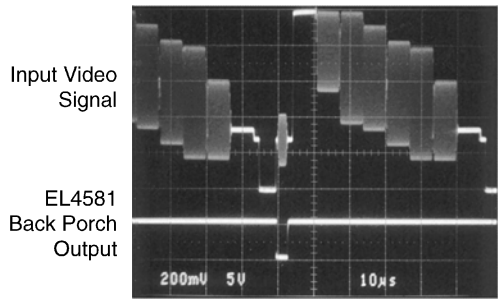


FIGURE 2.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. The power supply pins must be well bypassed to reduce the risk of oscillation. In the EL4093 there are two sets of supply pins: V+1/V-1 provide power for the CFA, and V+2/V-2 are for the S/H amplifier. Good performance can be achieved using only one set of bypass capacitors, although they must be close to the V+1/V-1 pins since that is where the high frequency currents flow. The combination of a 4.7µF tantalum capacitor in parallel with a 0.01µF capacitor has been shown to work well. Chip capacitors are recommended for the 0.01µF bypass to minimize lead inductance.

For good AC performance, parasitic capacitance should be kept to a minimum, especially at the CFA inverting input. Ground plane construction should be used, but it should be removed from the area near the inverting input to minimize any stray capacitance at that node. Chip resistors are recommended for R_F and R_G, and use of sockets should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in some additional peaking and overshoot.

If the CFA is configured for non-inverting gain, then one should also pay attention to the trace leading to the +input. The inductance of a long trace (> 3’) can form a resonant network with the amplifier input, resulting in high frequency oscillations around 700MHz. In such cases a 50Ω–100Ω series resistor placed close to the +input would isolate this inductance and damp out the resonance.

Capacitance at the Inverting Input

Any manufacturer’s high-speed voltage or current feedback amplifier can be affected by stray capacitance at the inverting input. For inverting gains this parasitic capacitance has little effect because the inverting input is a virtual ground, but for non-inverting gains this capacitance (in conjunction with the feedback and gain resistors) creates a pole in the feedback path of the amplifier. This pole, if low enough in frequency, has the same destabilizing effect as a zero in the forward open-loop response. Hence it is important to minimize the stray capacitance at this node by removing the nearby ground plane. In addition, since the S/H output connects to this node, it is important to minimize the trace capacitance. Good practice here would be to connect the two pins with a short trace directly underneath the chip.

Feedback Resistor Values

The EL4093 has been optimized for a gain of +2 with R_F = 750Ω. This value of feedback resistor gives a 3dB bandwidth of 300MHz at a gain of +2 driving a 150Ω load. Since the amplifier inside the EL4093 uses current mode feedback, it is possible to change the value of R_F to adjust the bandwidth. Shown in the table below are optimum feedback resistor values for different closed loop gains.

GAIN	OPTIMUM RF	BW (MHz)	PEAKING (dB)
+1	910	314	0.2

GAIN	OPTIMUM RF	BW (MHz)	PEAKING (dB)
+2	750	300	0
+5	470	294	0.2
-1	680	300	0

Autozero Interface

The autozero interface refers to the connection between the S/H output and the CFA inverting input. This interface has been greatly simplified compared to that of the EL2090, in that the S/H output is a high impedance current source. The S/H output can be connected directly to the inverting input, and its high impedance greatly reduces the interaction between the sample & hold and the gain setting resistors. Another virtue of this interface is better gain linearity as the autozero current changes. For example, at an autozero current of 0mA the output impedance is about 5MΩ, dropping to 1MΩ as the autozero current increases to 3mA. Using $R_F = R_G = 750\Omega$, the closed loop gain changes only by 0.025% in this interval.

Autozero Range

The autozero range is defined as the difference between the input DC level and the reference voltage to restore to. The size of this range is a function of the gain setting resistors used and the S/H output current swing. For a gain of +2 the optimum feedback resistor is 750Ω, and the available S/H output current is ±5.5mA minimum. To determine the autozero range for this case, we refer to Figure 3 below.

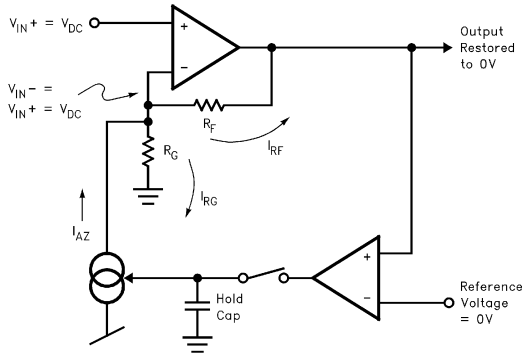


FIGURE 3.

Suppose that the input DC level is $+V_{DC}$, and that the reference voltage is 0V. We know that in feedback, the following two conditions will exist on the CFA: first, its output will be equal to 0V (due to autozero), and second, its V_{IN}- voltage is equal to the V_{IN}+ voltage (i.e. $V_{IN}- = +V_{DC}$). So we have a potential difference of $+V_{DC}$ across both R_F and R_G, resulting in a current $I_{RF} = I_{RG} = V_{DC}/750\Omega$ that must flow into each of them. This current $I_{AZ} = (I_{RF} + I_{RG})$ must come from the S/H output. Since the maximum that I_{AZ} can be is 5.5mA, we can solve for V_{DC} using the following:

$$I_{AZ} = \pm 5.5mA = 2\left(\frac{V_{DC}}{750\Omega}\right)$$

and see that $V_{DC} = \pm 2V$. This range can easily accommodate most video signals.

As another example, consider the case where we are restoring to a reference voltage of +0.75V. Using the same reasoning as above, a current $I_{RF} = (V_{DC} - 0.75V)/R_F$ must flow through R_F, and a current $I_{RG} = V_{DC}/R_G$ must go into R_G. Again, our boundary condition is that $I_{RF} + I_{RG} \leq \pm 5.5mA$, and we can solve for the allowable V_{DC} values using the following:

$$\pm 5.5mA = \frac{V_{DC} - 0.75V}{750\Omega} + \frac{V_{DC}}{750\Omega}$$

Hence V_{DC} must be between +2.4V to -1.7V. This example illustrates that when the reference changes, the autozero range also changes. In general, the user should determine the autozero range for his/her application, and ensure that the input signal is within this range during the autozero period.

Autozero Loop Bandwidth

The gain-bandwidth product (GBWP) of the autozero loop is determined by the size of the hold capacitor, the value of R_F, and the transconductances (gm's) of the S/H amplifier. To begin, the S/H amplifier is modeled as in Figure 4. First, the input stage transconductance is represented by gm1, with the compensation capacitor given by C_{HOLD}. This stage's GBWP is thus $gm1/(2\pi \bullet C_{HOLD}) = 1/(2\pi \bullet (350\Omega)(2.2nF)) = 207kHz$. Next, since the S/H has a current output, its output stage can be modeled as a transconductance gm2, in this case having a value of 1/(500Ω). The current from gm2 then flows through the I to V converter made up of the CFA and R_F to produce a voltage gain. Thus the GBWP of the overall loop is given by:

$$GBWP = \frac{gm1}{2\pi \times C_{HOLD}}(gm2 \times R_F)$$

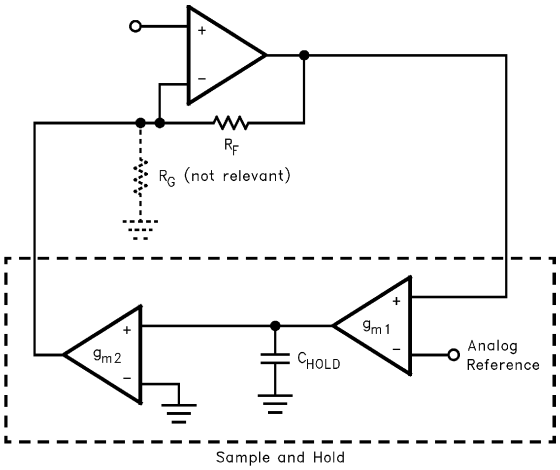


FIGURE 4.

With R_F = 750Ω, a GBWP of 310kHz is obtained. Note however that this is the small signal GBWP. As mentioned earlier, the sample and hold has special boost circuits built in which provides ±8.5mA of charge current during full slew. These boost circuits turn on when the S/H input differential voltage exceeds ±50mV. When the boosters are turned on, gm1 greatly increases and the circuit becomes nonlinear. Thus some stability issues are associated with the boosters, and they will be addressed in a later section.

Charge Injection and Hold Step

Charge injection refers to the charge transferred to the hold capacitor when switching to the HOLD mode. The charge should ideally be 0, but due to stray capacitive coupling and other effects, is typically 0.1pC in the EL4093. This charge changes the hold capacitor voltage by $\Delta V = \Delta Q/C_{HOLD}$, and this ΔV is multiplied by the output stage transconductance (gm2) to produce a change in S/H output current. This last quantity is listed as the spec ΔI_{STEP}, and is calculated using the following:

$$\Delta I_{SEP} = \left(\frac{\Delta Q}{C_{HOLD}}\right) \times gm2$$

For C_{HOLD} = 2.2nF and gm2 = 1/(500Ω), ΔI_{STEP} has a typical value of 100nA. This change in S/H output current flows through R_F, shifting the CFA output voltage. However, as we shall soon see, this shift is negligible. Assuming R_F = 750Ω, ΔI_{STEP} is impressed across R_F to give (750Ω)(100nA) = 0.08mV of change at the CFA output.

Droop Rate

When the S/H amplifier is in HOLD mode, there is a small current that leaks from the switch into the hold capacitor. This quantity is termed the droop current, and is typically 10nA in the EL4093. This droop current produces a ramp in the hold capacitor voltage, which in turn produces a similar effect at the CFA output. The Droop Rate at the CFA output can be found using the equation below:

$$Droop = \frac{I_{DROOP}}{C_{HOLD}}(gm2 \times R_F)$$

Assuming R_F = 750Ω and C_{HOLD} = 2.2nF, the drift in the CFA output due to droop current is about 7µV/µs. Recall that in NTSC applications, there is about 60µs between autozero periods. Thus there is 7µV/µs(60µs) = 0.4mV, or less than 0.1 IRE, of drift over each NTSC scan line. This drift is negligible in most applications.

Choice of Hold Capacitor

The EL4093 has been designed to work with a hold capacitor of 2.2nF. With this value of C_{HOLD}, the droop rate and hold step are negligibly small for most applications. In addition, with the special boost circuits inside the S/H, fast acquisition is possible even using a hold capacitor of this size. Figure 5 shows the input and output of the DC-restored amplifier while the S/H is in sample mode. Applying a +1V step to the non-inverting input of the CFA, the output of the CFA jumps to +2V. The S/H, however, then tries to autozero the system by driving the CFA output back to the reference voltage. Since the input differential across the S/H is initially +2V, the boost circuits turn on and supply 8.5mA of charge current to the hold capacitor. The boost circuit remains on until the CFA output has come to within 50mV of the reference. Note that this event took only 320ns; settling to within 1% of the final value takes another 2µs. Thus for a 1V input step, acquisition takes only one to two NTSC scan lines.

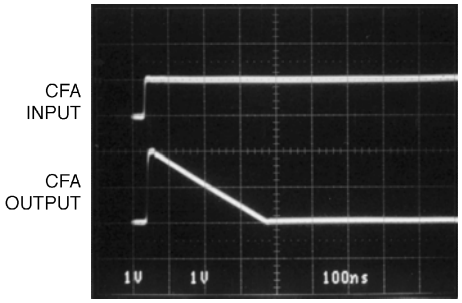


FIGURE 5. AUTOZERO MECHANISM RESTORES AMPLIFIER OUTPUT TO GROUND AFTER +1V STEP AT INPUT

A natural question arises as to whether there are other C_{HOLD} values that can be used. In one direction, increasing C_{HOLD} will further reduce the droop and hold step, but lengthen the acquisition time. Since the droop and hold step are already small to begin with, there is no apparent advantage to increasing C_{HOLD}.

In the other direction, decreasing C_{HOLD} would increase the droop and hold step but shorten the acquisition time. There is, however, a caveat to reducing C_{HOLD}: too small a C_{HOLD} would cause the autozero loop to oscillate. The reason is that when the S/H boost circuit turns on, the input stage gm increases drastically and the circuit becomes nonlinear. A sufficiently large C_{HOLD} must be used to suppress the non-linearity and force the loop to settle. For example, it has been found that a C_{HOLD} of 470pF results in $1V_{P-P}$ oscillation around 10MHz at the CFA output.

The minimum recommended value for C_{HOLD} is 2.2nF. With this value the loop remains stable over the entire operating temperature range (-40°C to +85°C). The greatest instability occurs at low temperatures, where we observe from the performance curves that the S/H gm's, and hence the GBWP, are at their maximum. If the operating range is restricted to room temperature or above, then 1.5nF is sufficient to keep the loop stable. At this value of C_{HOLD} the acquisition time reduces to about 1.5µs.

Video Performance and Application

Although the EL4093 is intended for high speed video applications such as SVGA, it also offers excellent performance for NTSC, with 0.04% dG and 0.02° dP at 3.58MHz. Some application considerations, however, are required for handling NTSC signals.

Referring back to Figure 2, recall that typically, the autozero interval lies in the back porch portion of video containing the colorburst pulse. When the S/H compares the video to the reference voltage during this period, the colorburst ($40\ IRE_{P-P}$) triggers the S/H boost circuit and prevents the autozero loop from settling.

A remedy for this situation is to attenuate the colorburst before applying it to the S/H input. Figure 6 below shows a 3.58MHz chroma trap which would notch out the colorburst while preserving the video DC level.

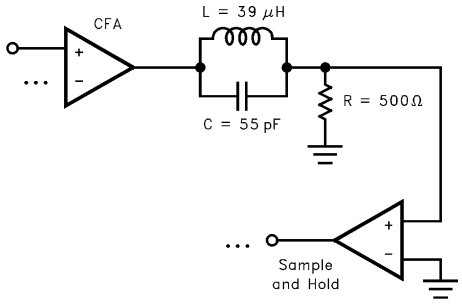


FIGURE 6. COLORBURST TRAP FOR NTSC APPLICATIONS

One may be tempted to use a RC lowpass filter to suppress the colorburst, as shown in Figure 7 below. This technique, however, poses several problems. First, to obtain enough attenuation, we need to set the pole frequency 10 to 20 times lower than 3.58MHz. This pole, being close to the auto zero loop pole, would destabilize the system and cause the loop to oscillate.

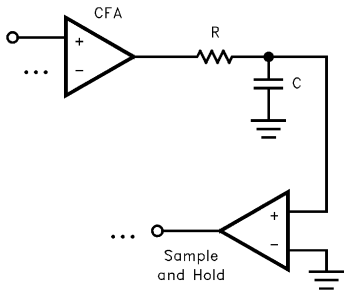


FIGURE 7. CAUTION: LOWPASS FILTER DOES NOT WORK IN NTSC APPLICATIONS

Although we can cancel this pole by introducing a zero, the RC network introduces a time delay between the CFA output and the S/H input. This has undesirable effects in some NTSC applications, as Figure 8 illustrates. There is only 0.6µs from the rising edge of sync to the colorburst. If we are autozeroing over the back porch, the autozero period would begin somewhere in this 0.6µs interval. Since the edge of sync is now delayed by the RC network, autozero begins before the video back porch reaches its final value. Consequently, the autozero loop performs a correction on every line and never settles.

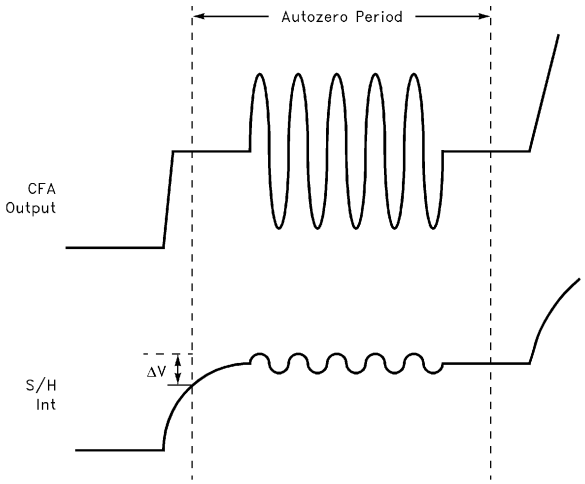


FIGURE 8. LOWPASS FILTER DELAYS INPUT TO SAMPLE AND HOLD

If the video does not contain any AC components during the autozero level (e.g. RGB video), then the above networks are not needed and the CFA output can be connected directly to the S/H input.

Power Dissipation

The EL4093 current feedback amplifier has an absolute maximum of ±30mA output current drive. This is slightly more than the current required to drive ±2V into 75Ω. To see how much the junction temperature is raised in this worst case, we refer to the equations below:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \bullet PD_{MAX})$$

where:

T_{MAX} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PD_{MAX} = Maximum Power Dissipation of the CFA and S/H amplifier in the Package

PD_{MAX} for either the CFA or the S/H amplifier can be calculated as follows:

$$PD_{MAX} = (2 \bullet V_S \bullet I_{SMAX}) + (V_S - V_{OUTMAX}) \bullet (V_{OUTMAX}/R_L)$$

where:

V_S = Supply Voltage

I_{SMAX} = Maximum Supply Current of Amplifier

V_{OUTMAX} = Maximum Output Voltage of Application

R_L = Load Resistance

For the EL4093, the maximum supply current is 11.5mA on V_S = ±5V. Assume that in the worst case, the CFA output swings ±2V into 75Ω. Since the S/H has a current output, we assume that it is at maximum current swing (±5.5mA) but at a mid-rail output voltage (0V). With the above assumptions, PD_{MAX} for the EL4093 is 223mW, and using the thermal resistance of a narrow SO package (120°C/W), this yields a temperature increase of 27°C. Since the maximum ambient temperature is 85°C, the resulting junction temperature of 112°C is still below the maximum.

Please note that this in addition to metal migration problems.