CA3054

Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

FN388
Rev.6.00
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The CA3054 consists of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300MHz. These feature make the CA3054 useful from DC to 120MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
CA3054M96 (3054)	0 to 85	14 Ld SOIC Tape and Reel	M14.15
CA3054MZ (CA3054MZ)	0 to 85	14 Ld SOIC (Pb-free)	M14.15
CA3054MZ96 (CA3054MZ)	0 to 85	14 Ld SOIC Tape and Reel (Pb-free)	M14.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

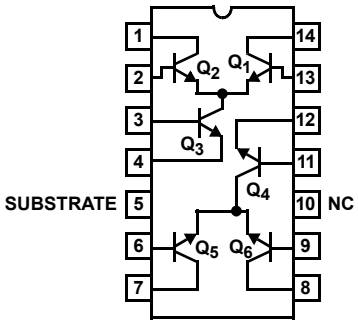
- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage . . . . . ±5mV
- Temperature Range . . . . . 0°C to 85°C
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations
  - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

Pinout

CA3054 (SOIC)
TOP VIEW



Absolute Maximum Ratings $T_A = 25°C$

Collector-to-Emitter Voltage, V_{CEO} 15V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} (Note 1) 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 50mA

Operating Conditions

Temperature Range . . . . . 0°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	140

Maximum Junction Temperature (Die) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)
Maximum Power Dissipation (Any One Transistor) 300mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical Terminal 2 with respect to Terminal 4 is +15V to -5V.

(NOTE 4) TERM NO.	13	14	1	2	3	4	6	7	8	9	11	12	5
13		0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
14			Note 3	Note 3	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
1				+20, 0	Note 3	+20, 0	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	+20, 0
2					Note 3	+15, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
3						+1, -5	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
4							Note 3	Note 3	Note 3	Note 3	Note 3	Note 3	Note 3
6								0, -20	Note 3	+5, -5	Note 3	+15, -5	Note 3
7									Note 3	Note 3	Note 3	Note 3	+20, 0
8										+20, 0	Note 3	Note 3	+20, 0
9											Note 3	+15, -5	Note 3
11												-1, -5	Note 3
12													Note 3
5													Ref. Substrate

Maximum Current Ratings

(NOTE 4) TERM NO.	I_{IN} mA	I_{OUT} mA
13	5	0.1
14	50	0.1
1	50	0.1
2	5	0.1
3	5	0.1
4	0.1	50
6	5	0.1
7	50	0.1
8	50	0.1
9	5	0.1
11	5	0.1
12	0.1	50

NOTES:

3. Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.
4. Terminal No. 10 of CA3054 is not used.

Electrical Specifications $T_A = 25°C$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS For Each Differential Amplifier						
Input Offset Voltage (Figure 8)	V_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.45	5	mV
Input Offset Current (Figure 9)	I_{IO}	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.3	2	µA
Input Bias Current (Figure 5)	I_I	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	10	24	µA
Quiescent Operating Current Ratio (Figure 5)	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	0.98 to 1.02	-	-
Temperature Coefficient Magnitude of Input Offset Voltage (Figure 7)	$\fr\|\Delta V_{IO}\|}{\Delta T}$	V_{CB} = 3V, $I_{E(Q3)} = I_{E(Q4)}$ = 2mA	-	1.1	-	µV/°C

Electrical Specifications $T_A = 25°C$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
FOR EACH TRANSISTOR							
DC Forward Base-to-Emitter Voltage (Figure 8)	V_{BE}	V_{CB} = 3V	I_C = 50µA	-	0.630	0.700	V
			I_C = 1mA	-	0.715	0.800	V
			I_C = 3mA	-	0.750	0.850	V
			I_C = 10mA	-	0.800	0.900	V
Temperature Coefficient of Base-to-Emitter Voltage (Figure 6)	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3V, I_C = 1mA		-	-1.9	-	µV/°C
Collector Cutoff Current (Figure 4)	I_{CBO}	V_{CB} = 10V, I_E = 0		-	0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		15	24	-	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10µA, I_E = 0		20	60	-	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10µA, I_{CI} = 0		20	60	-	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10µA, I_C = 0		5	7	-	V
DYNAMIC CHARACTERISTICS							
Common Mode Rejection Ratio for each Amplifier (Figures 1, 10)	CMRR	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	100	-	dB
AGC Range, One Stage (Figures 2, 11)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	75	-	dB
Voltage Gain, Single Stage Double-Ended Output (Figures 2, 11)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	32	-	dB
AGC Range, Two Stage (Figures 3, 12)	AGC	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	105	-	dB
Voltage Gain, Two Stage Double-Ended Output (Figures 3, 12)	A	V_{CC} = 12V, V_{EE} = -6V, V_X = -3.3V, f = 1kHz		-	60	-	dB
Low Frequency, Small Signal Equivalent Circuit Characteristics (For Single Transistor)							
Forward Current Transfer Ratio (Figure 13)	h_{FE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	110	-	-
Short Circuit Input Impedance (Figure 13)	h_{IE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	3.5	-	kΩ
Open Circuit Output Impedance (Figure 13)	h_{OE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	15.6	-	µS
Open Circuit Reverse Voltage Transfer Ratio (Figure 13)	h_{RE}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		-	1.8×10^{-4}	-	-
1/f Noise Figure for Single Transistor	NF	f = 1kHz, V_{CE} = 3V		-	3.25	-	dB
Gain Bandwidth Product for Single Transistor (Figure 14)	f_T	V_{CE} = 3V, I_C = 3mA		-	550	-	MHz
Admittance Characteristics; Differential Circuit Configuration (For Each Amplifier)							
Forward Transfer Admittance (Figure 15)	Y_{21}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-20 + j0	-	mS
Input Admittance (Figure 16)	Y_{11}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.22 + j0.1	-	mS
Output Admittance (Figure 17)	Y_{22}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	0.01 + j0	-	mS
Reverse Transfer Admittance (Figure 18)	Y_{12}	V_{CB} = 3V, f = 1MHz Each Collector $I_C \approx$ 1.25mA		-	-0.003 + j0	-	mS

Electrical Specifications $T_A = 25°C$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Admittance Characteristics; Cascode Circuit Configuration (For Each Amplifier)						
Forward Transfer Admittance (Figure 19)	Y_{21}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	68 - j0	-	mS
Input Admittance (Figure 20)	Y_{11}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.55 + j0	-	mS
Output Admittance (Figure 21)	Y_{22}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0 + j0.02	-	mS
Reverse Transfer Admittance (Figure 22)	Y_{12}	V_{CB} = 3V, f = 1MHz Total Stage $I_C \approx$ 2.5 mA	-	0.004 - j0.005	-	µS
Noise Figure	NF	f = 100MHz	-	8	-	dB

Test Circuits

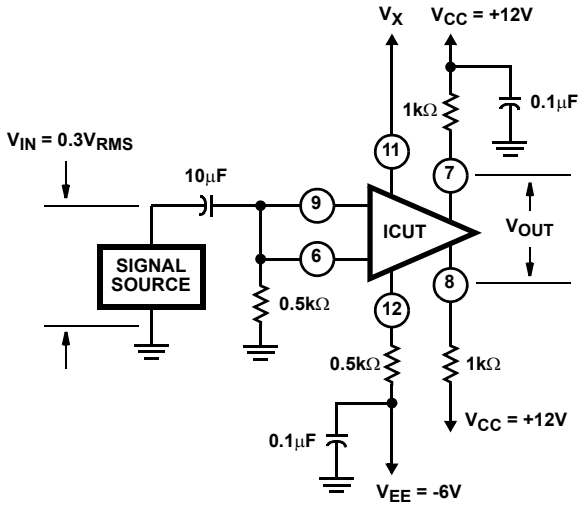


FIGURE 1. COMMON MODE REJECTION RATIO TEST SETUP

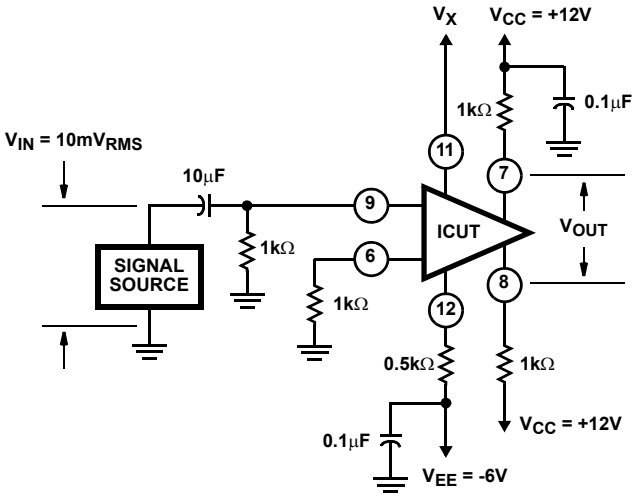


FIGURE 2. SINGLE STAGE VOLTAGE GAIN TEST SETUP

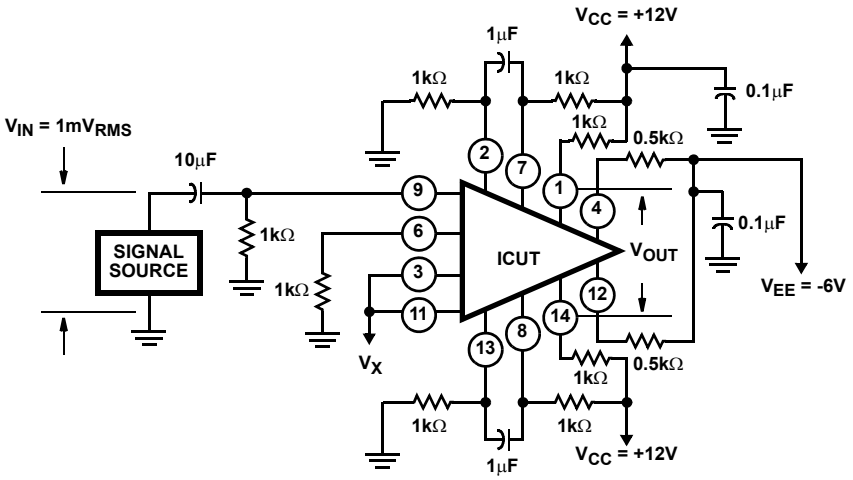
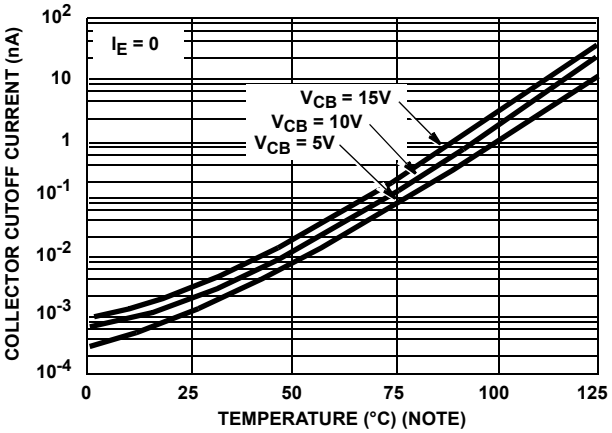


FIGURE 3. TWO STAGE VOLTAGE GAIN TEST SETUP

Typical Performance Curves



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 4. COLLECTOR-TO-BASE CUTOFF CURRENT vs TEMPERATURE FOR EACH TRANSISTOR

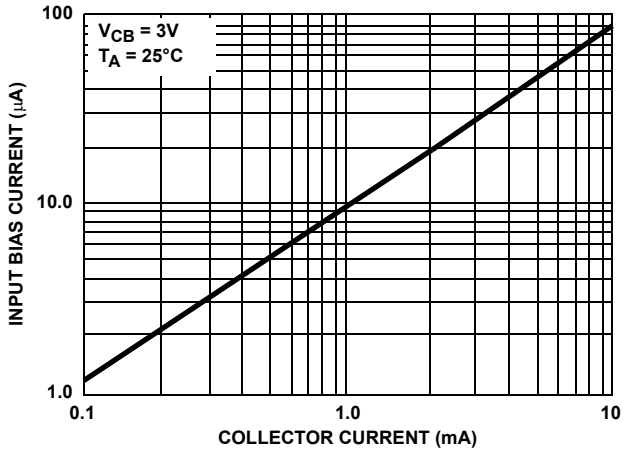
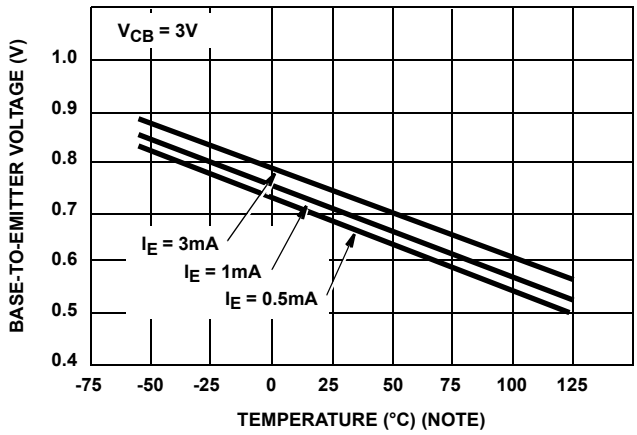
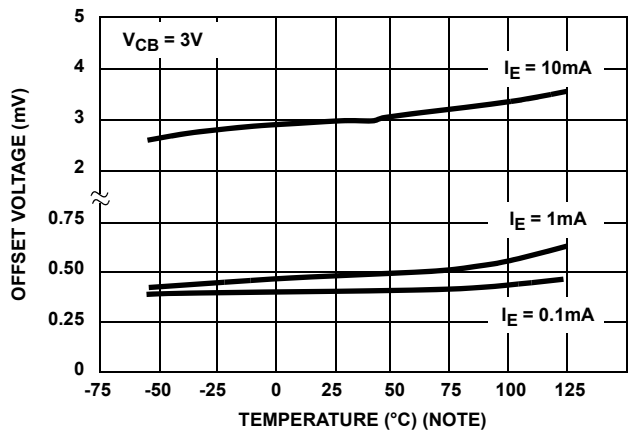


FIGURE 5. INPUT BIAS CURRENT vs COLLECTOR CURRENT FOR EACH TRANSISTOR



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 6. BASE-TO-EMITTER VOLTAGE FOR EACH TRANSISTOR vs TEMPERATURE



NOTE: For CA3054 use data from 0°C to 85°C only.

FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE FOR DIFFERENTIAL PAIRS

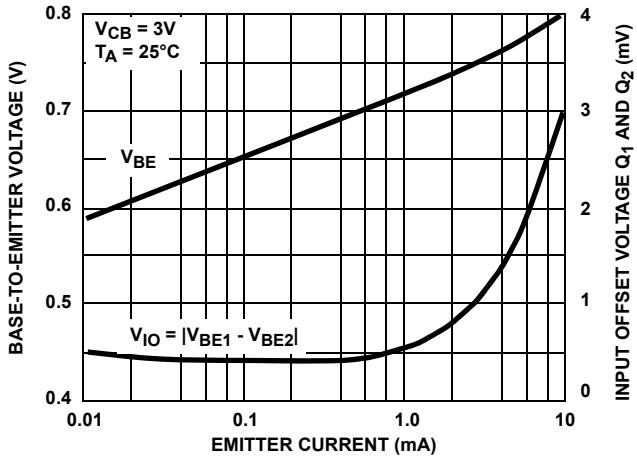


FIGURE 8. STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS vs EMITTER CURRENT

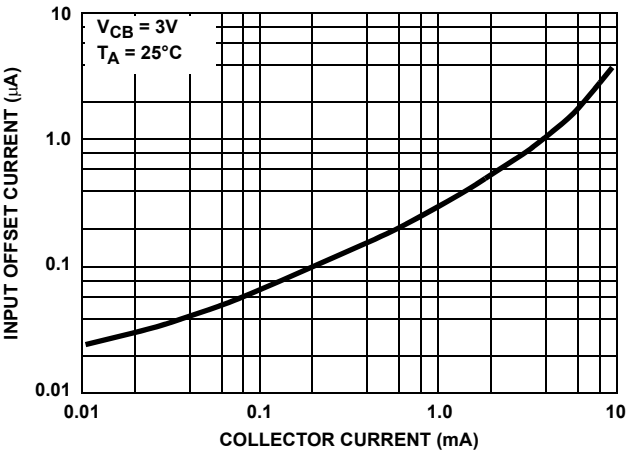


FIGURE 9. INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS vs COLLECTOR CURRENT

Typical Performance Curves (Continued)

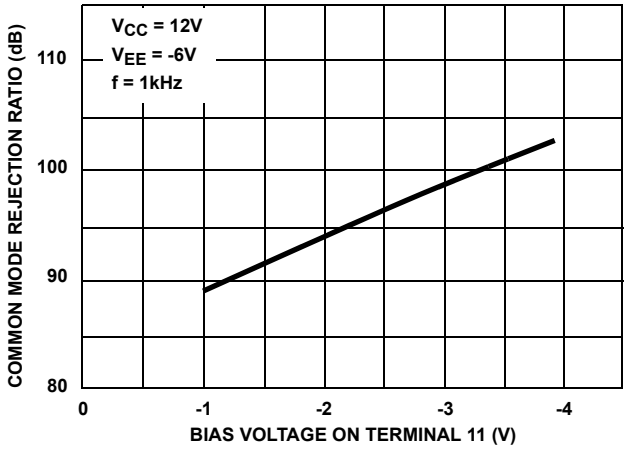


FIGURE 10. COMMON MODE REJECTION RATIO CHARACTERISTIC

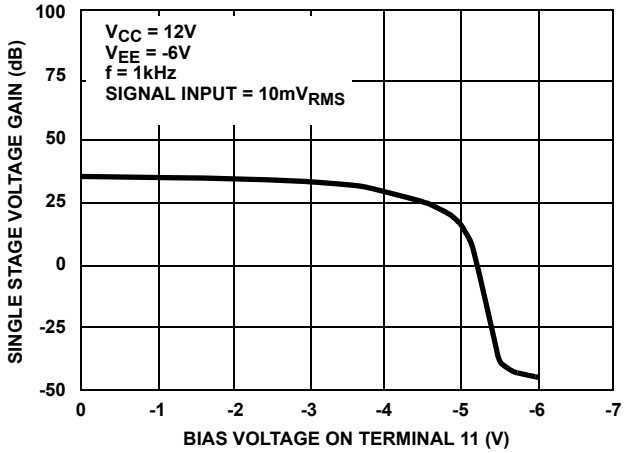


FIGURE 11. SINGLE STAGE VOLTAGE GAIN CHARACTERISTIC

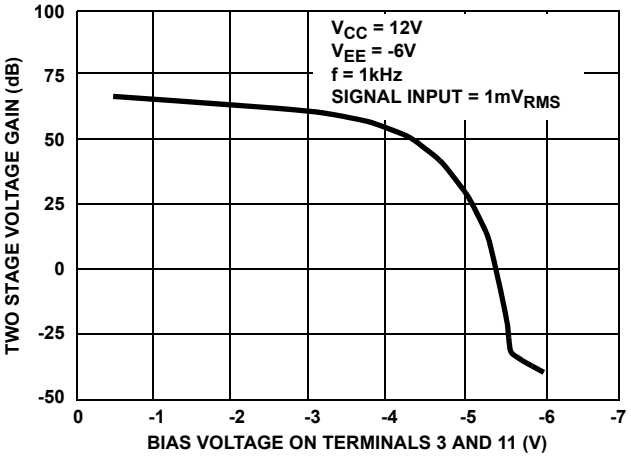


FIGURE 12. TWO STAGE VOLTAGE GAIN CHARACTERISTIC

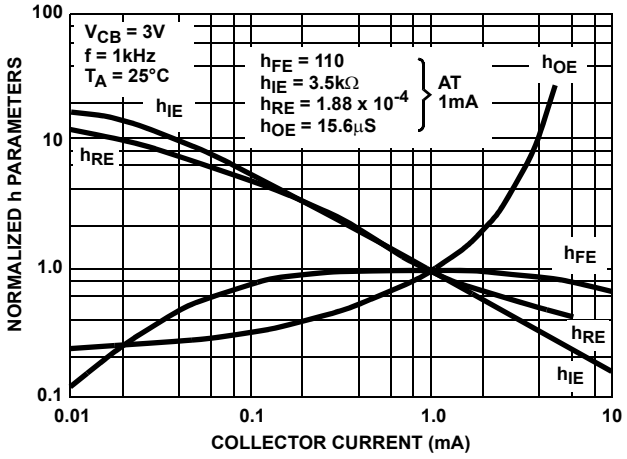


FIGURE 13. FORWARD CURRENT TRANSFER RATIO (h_{FE}), SHORT CIRCUIT INPUT IMPEDANCE (h_{IE}), OPEN CIRCUIT OUTPUT IMPEDANCE (h_{OE}), AND OPEN CIRCUIT REVERSE VOLTAGE TRANSFER RATIO (h_{RE}) vs COLLECTOR CURRENT FOR EACH TRANSISTOR

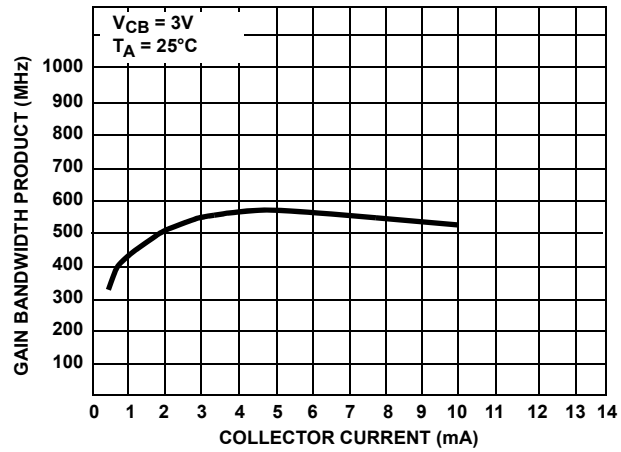


FIGURE 14. GAIN BANDWIDTH PRODUCT (f_T) vs COLLECTOR CURRENT

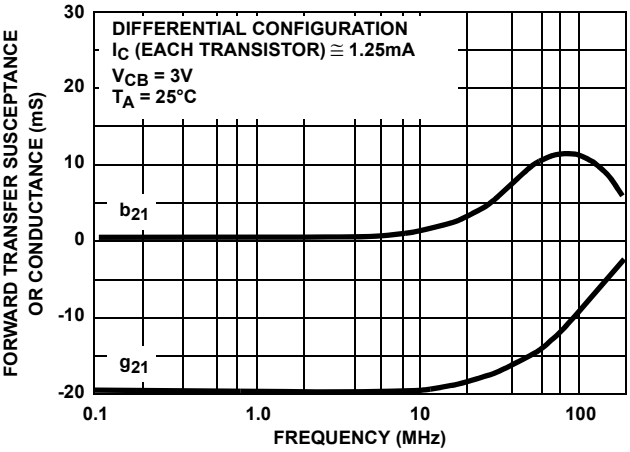


FIGURE 15. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

Typical Performance Curves (Continued)

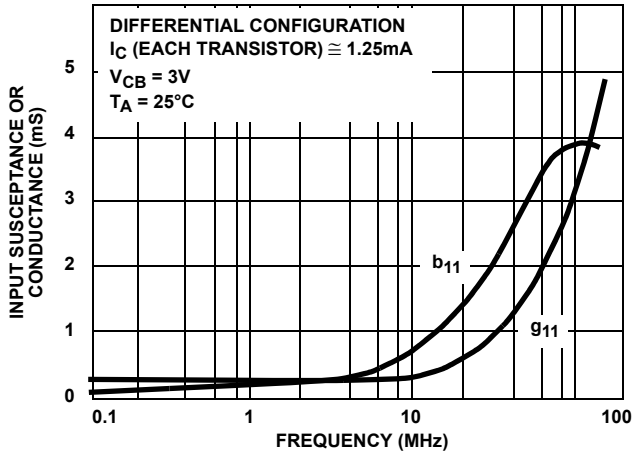


FIGURE 16. INPUT ADMITTANCE (Y_{11})

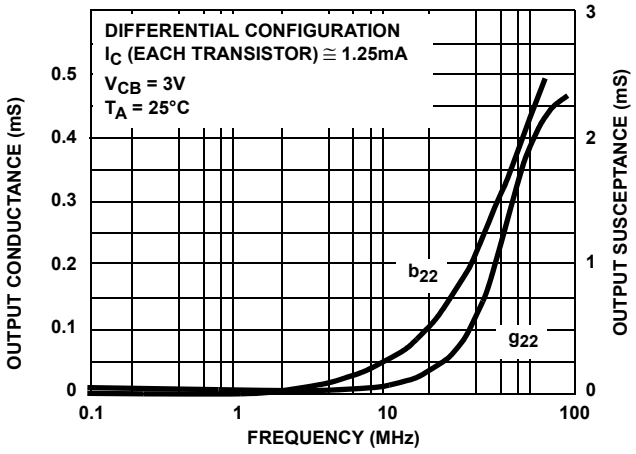


FIGURE 17. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

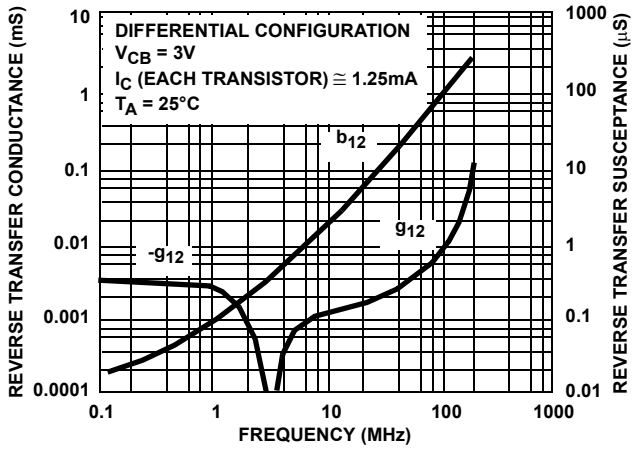


FIGURE 18. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY

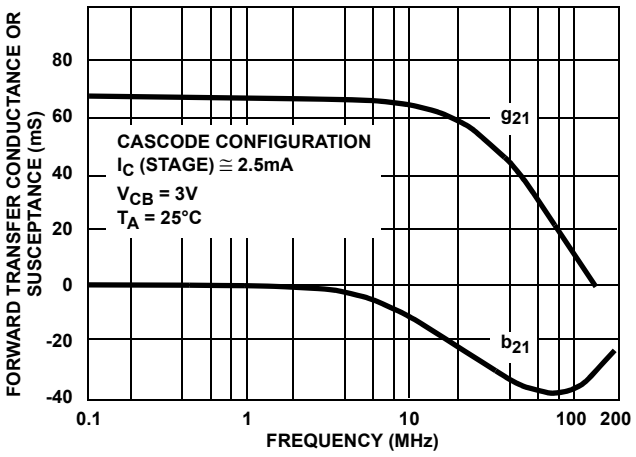


FIGURE 19. FORWARD TRANSFER ADMITTANCE (Y_{21}) vs FREQUENCY

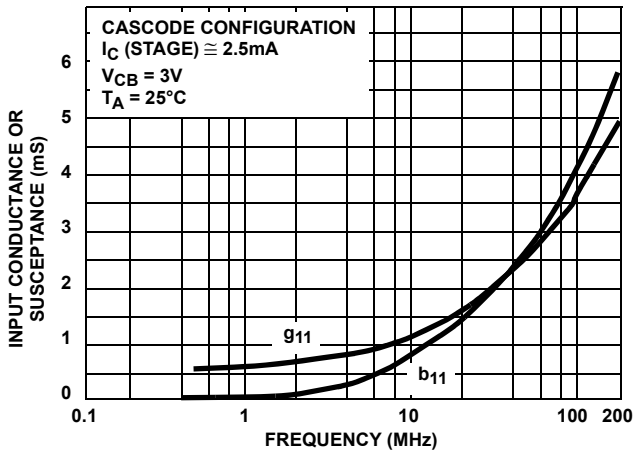


FIGURE 20. INPUT ADMITTANCE (Y_{11}) vs FREQUENCY

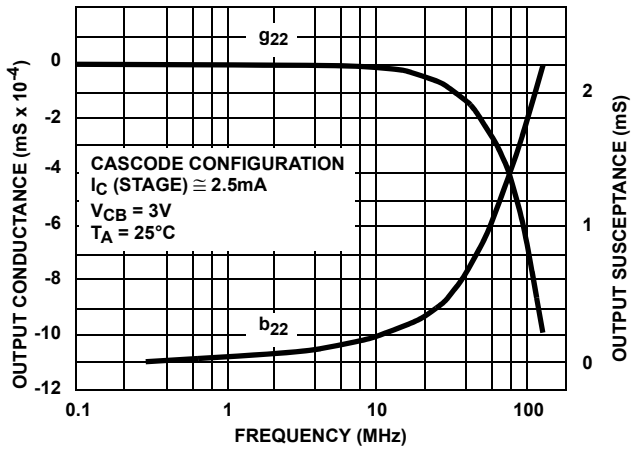


FIGURE 21. OUTPUT ADMITTANCE (Y_{22}) vs FREQUENCY

Typical Performance Curves (Continued)

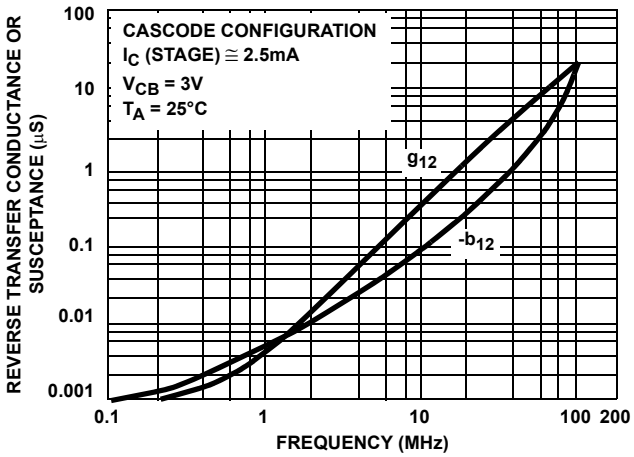


FIGURE 22. REVERSE TRANSFER ADMITTANCE (Y_{12}) vs FREQUENCY