MAX 108 segments (SEG27×COM4)

Standard LCD Segment Drivers

BU9795AFV-LB

This is the product guarantees long time support in Industrial market.

Features

- Long Time Support Product for Industrial Applications.
- Integrated RAM for Display Data (DDRAM) : 35 × 4bit
- LCD Drive Output : 4 Common Output, 27Segment Output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator Circuit
- No External Components
- Low Power Consumption Design

Applications

- Industrial Equipment
- Telephone
- FAX
- Portable Equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car Audio
- Home Electrical appliance
- Meter Equipment

Etc.

Key Specifications

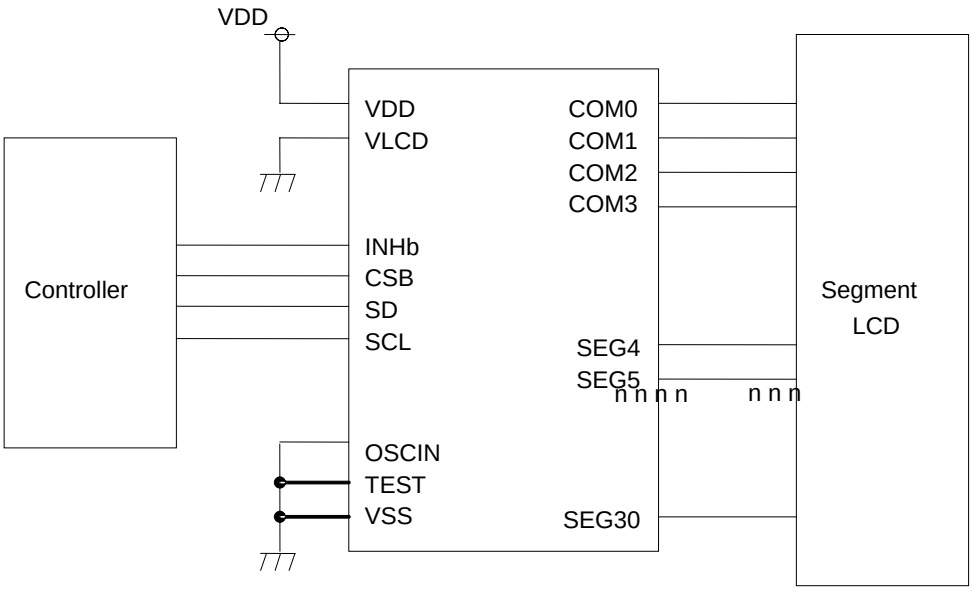
- Supply Voltage Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments:BU9795AFV-LB 108 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

Package

W (Typ.) x D (Typ.) x H (Max.)

SSOP-B40
13.60mm x 7.80mm x 2.00mm

Typical Application Circuit



Internal Oscillator Circuit Mode

Figure 1. Typical application circuit

d Product structure9æSilicon monolithic integrated circuit T This product has no designed protection against radioactive rays.

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Block Diagrams / Pin Configurations / Pin Descriptions

BU9795AFV-LB

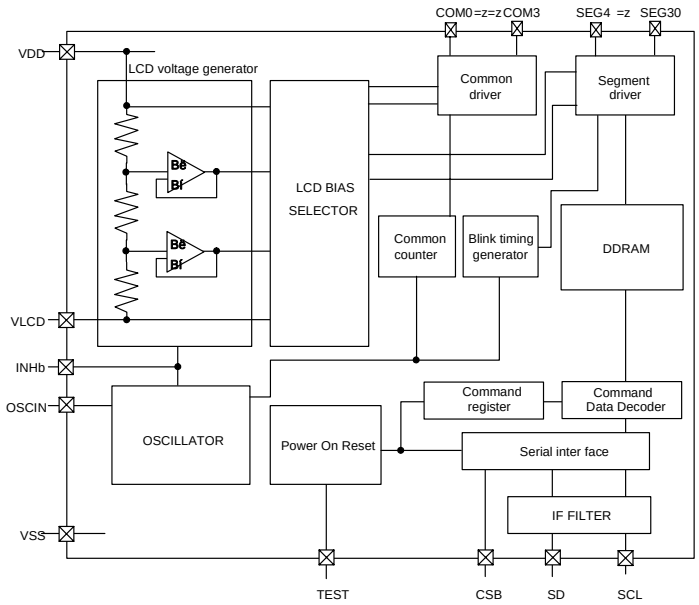

Figure 2. Block Diagram

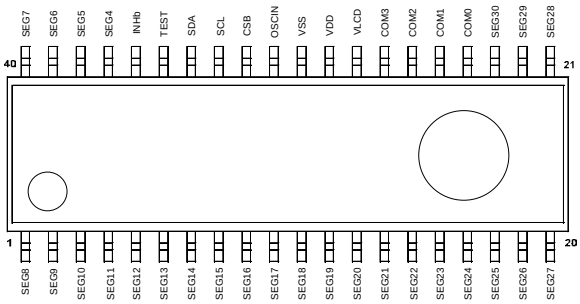

Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Pin Name	Pin No.	I/O	Function
INHb	36	I	Input terminal for turn off display H : turn on display L : turn off display
TEST	35	I	Test input (ROHM use only) Must be connected to VSS
OSCIN	31	I	External clock input Ext. clock and Int. clock can be changed by command. Must be connected to VSS when using internal oscillation circuit.
SD	34	I	Serial data input
SCL	33	I	Serial data transfer clock
CSB	32	I	Chip select : ”L” active
VSS	30		GND
VDD	29		Power supply
VLCD	28	I	Power supply for LCD driving
SEG4 to 30	1 to 23, 37 to 40	O	SEGMENT output for LCD driving
COM0 to 3	24 to 27	O	COMMON output for LCD driving

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Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remark
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 to VDD	V	LCD drive voltage
Power Dissipation	Pd	0.7	W	When use more than Ta=25°C, subtract 7mW per degree (BU9795AFV-LB) (Package only)
Input Voltage Range	VIN	-0.5 to VDD+0.5	V	
Operational Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	

Caution :Operating the IC over the absolute maximum ratings may damage the IC.The damage can either be a short circui between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +85°C, VSS=0V)

Parameter	Symbol	Ratings			Unit	Remark
		Min	Typ	Max		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	0	-	VDD -2.4	V	LCD drive voltage

(Note) Please use VDD-VLCD≥2.4V condition.

Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
“H” Level Input Voltage		VIH	0.7VDD	-	VDD	V	
“L” Level Input Voltage		VIL	VSS	-	0.3VDD	V	
“H” Level Input Current		IIH	-	-	1	µA	
“L” Level Input Current		IIL	-1	-	-	µA	
LCD Driver on Resistance	SEG	RON	-	3.5	-	k	Iload=±10µA
	COM	RON	-	3.5	-	k	
VLCD Supply Voltage		VLCD	0	-	VDD -2.4	V	VDD-VLCD≥2.4V
Standby Current		Ist	-	-	5	µA	Display off, Oscillator off
Power Consumption1		IDD1	-	12.5	30	µA	VDD=3.3V, Ta=25°C, Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power Consumption2		IDD2	-	20	40	µA	VDD=3.3V, Ta=25°C, Normal mode, FR=80Hz 1/3 bias, Line inverse

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Electrical Characteristics - continued

Oscillation Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency	f_{CLK}	56	80	104	Hz	FR = 80Hz setting
Frame Frequency1	f_{CLK1}	70	80	90	Hz	VDD=3.5V, 25°C

MPU interface Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	tr	-	-	80	ns	
Input Fall Time	tf	-	-	80	ns	
SCL Cycle Time	tSCYC	400	-	-	ns	
“H” SCL Pulse Width	tSHW	100	-	-	ns	
“L” SCL Pulse Width	tSLW	100	-	-	ns	
SD Setup Time	tSDS	20	-	-	ns	
SD Hold Time	tSDH	50	-	-	ns	
CSB Setup Time	tCSS	50	-	-	ns	
CSB Hold Time	tCSH	50	-	-	ns	
“H” CSB Pulse Width	tCHW	50	-	-	ns	

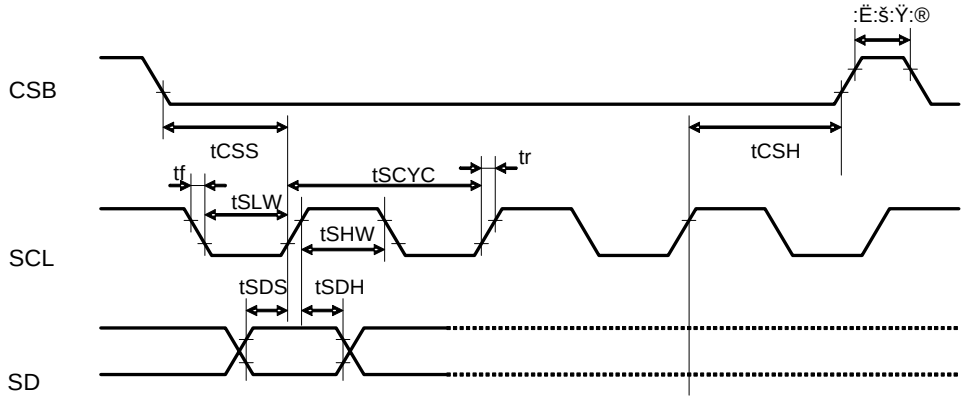

Figure 4. Interface Timing

I/O Equivalence Circuit

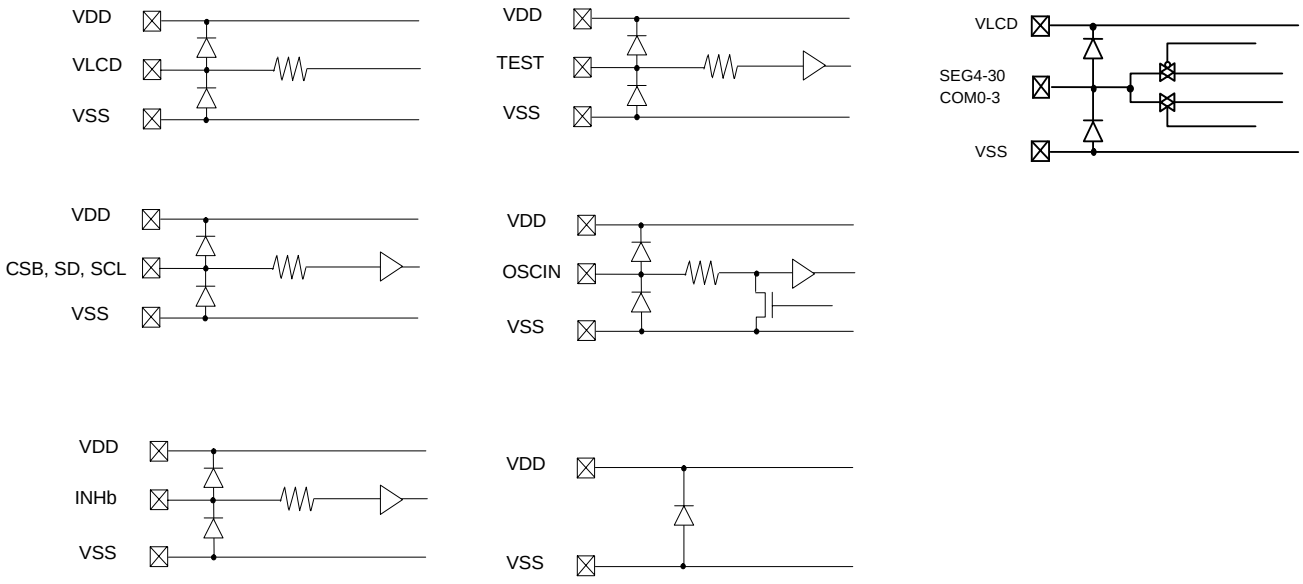

Figure 5. I/O equivalence circuit

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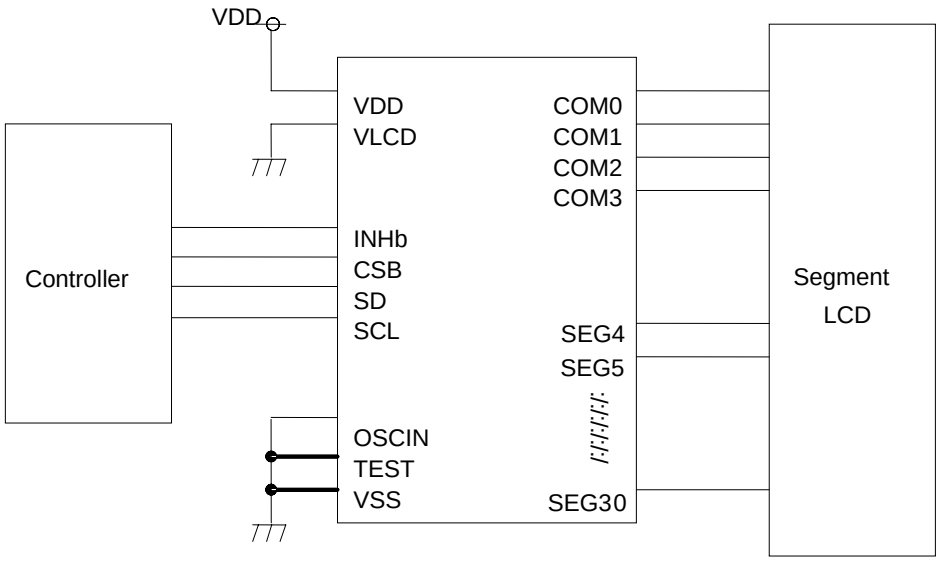
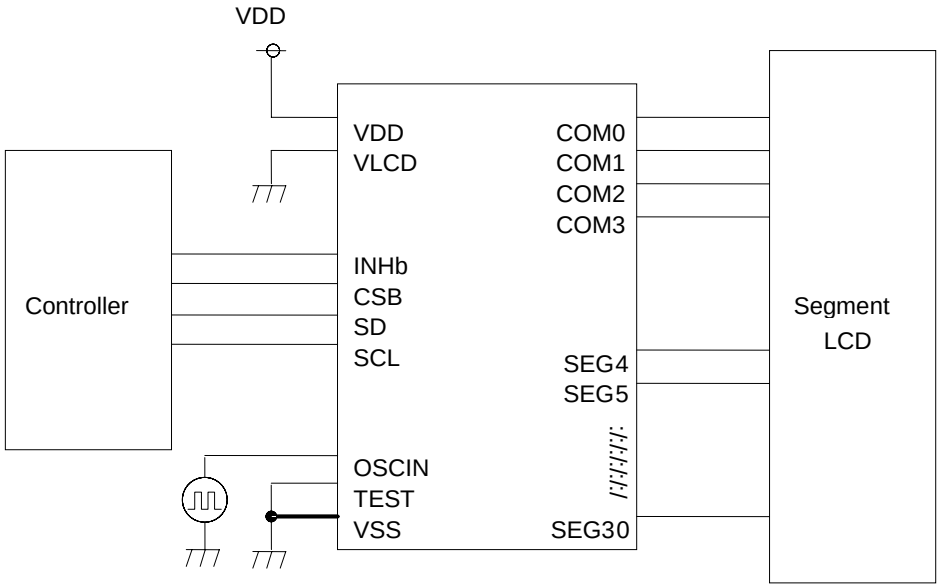
Example of Recommended Circuit

<BU9795AFV-LB>



Using internal oscillator circuit mode



Using external oscillator mode

Figure 6. BU9795AFV example recommended circuit

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Function Description

Command and data transfer method

3-SPI (3wire Serial interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H", and CSB="L" makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by D6 to D0 during CSB ="L".
(Internal data is latched at the rising edge of SCL, it is converted to 8bits parallel data at the falling edge of 8th CLK.)

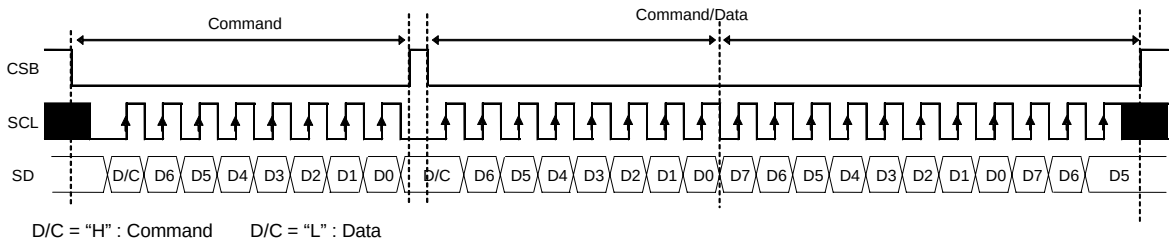
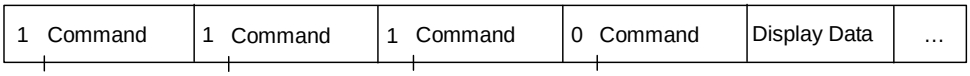


Figure 7. 3-SPI Command/Data transfer format

Command transfer method

After CSB="H" :"L", 1st byte is always a command input.
MSB of the command input data will be judged that the next byte data, it is a command or display data (This bit is called
"command or data judgment bit").
When set "command or data judge bit"='1', next byte will be (continuously) command.
When set "command or data judge bit"='0', next byte data is display data.



Once it becomes display data transfer condition, it will not be back to command input condition even if D/C=1.
So if you want to send command data again, please set CSB="L" :"H".
(CSB "L" :"H" will cancel data transfer condition.)
Command transfer is done by 8bits unit, so if CSB="L" :"H" with less than 8bits data transfer, command will be cancelled.
It will be able to transfer command with CSB="L" again.

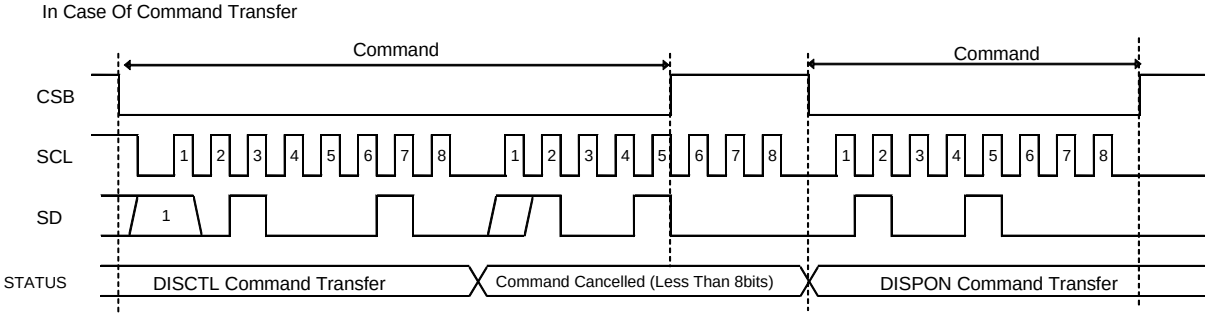


Figure 8. Command transfer format

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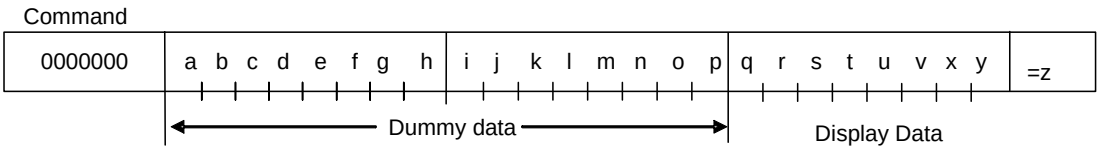
Write display data and transfer method

<BU9795AFV-LB>

This LSI has Display Data RAM (DDRAM) of 27×4=108bit.
As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, these address will be dummy address.
The relationship between data input and display data, DDRAM data and address are as follows.



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.
Data can be continuously written in DDRAM by transmitting Data continuously.
(When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.

DDRAM address

BIT	00h	01h	02h	03h	04h	05h	06h	07h	nnnnn nn	1Eh	1Fh	20h	21h	22h	
0	a	e	i	m	q	u									COM0
1	b	f	j	n	r	v									COM1
2	c	g	k	o	s	x									COM2
3	d	h	l	p	t	y									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	nnnnnnn	SEG30	SEG31	SEG32	SEG33	SEG34	

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L" :"H" before 4bits data transfer.

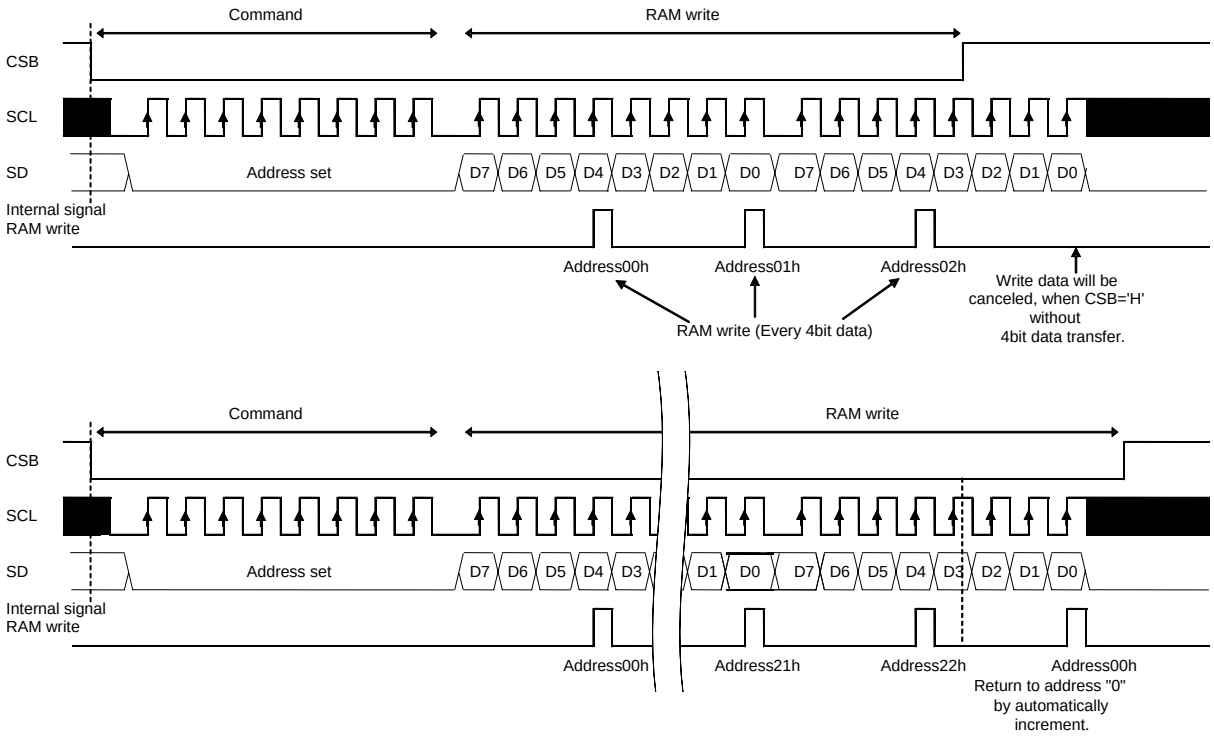


Figure 9. BU9795AFV-LB Data Transfer Format

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OSCILLATOR

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

(Note) When you use external clock, execute ICSET command and connect OSCIN to external clock.

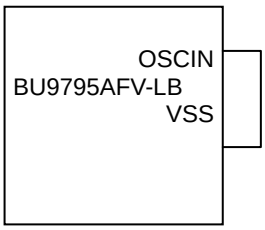

Figure 10. Internal oscillator circuit mode

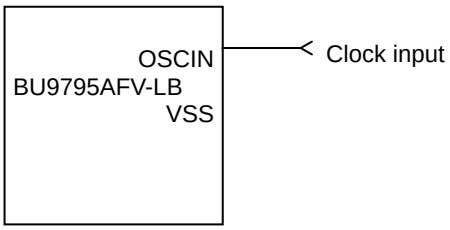

Figure 11. External clock mode

LCD Driver Bias Circuit

This LSI generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption.
1/3 and 1/2Bias can be set in MODESET command.
Line and frame inversion can be set in DISCTL command.
Refer to “LCD driving waveform” about each LCD driving waveform.

Blink timing generator

This device has Blinking function.
This LSI is able to set blink mode with BLKCTL command.
Blink frequency varies widely by characteristic of fCLK, when internal oscillation circuit.
Refer to Oscillation Characteristics for more details on fCLK.

Reset (initial) condition

Initial condition after execute SOFTWARE RESET is as follows.
nDisplay is OFF.
nDDRAM address is initialized (DDRAM Data is not initialized).
Refer to Command Description about initialize value of register.

Command / Function List

Description List of Command / Function

No.	Command	Function
1	Mode Set (MODESET)	Set LCD drive mode
2	Address Set (ADSET)	Set LCD display mode 1
3	Display Control (DISCTL)	Set LCD display mode 2
4	Set IC Operation (ICSET)	Set IC operation
5	Blink Control (BLKCTL)	Set blink mode
6	All Pixel Control (APCTL)	Set pixel condition

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Detailed Command Description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C : 0 : Next byte is RAM write data.
C : 1 : Next byte is command.

(1) Mode Set (MODE SET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(* : Don't care)

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF(DISPOFF)	0	d
Display ON(DISPON)	1	

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1 frame of data write. Display OFF mode will be finished by Display ON.
Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

(Note) It is not synchronize with display frame, when it will be controlled display ON/OFF with INHb terminal.

Set bias level

Setting	P2	Reset initialize condition
1/3 Bias	0	d
1/2 Bias	1	

Refer to LCD driving waveform.

(2) Address set (ADSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

Address data is specified in P [4:0] and P2 (ICSET command) as follows.

	MSB			LSB
Internal register	Address [5]	Address [4]	n n n	Address [0]
Bit of each command	ICSET [P2]	ADSET [P4]	n n n	ADSET [P0]

The address is 00h in reset condition. The valid address is 00h to 22h.
Another address is invalid, (otherwise address will be set to 00h.)
P2 of ICSET command is only to define either MSB of address is "1" or "0".
Address counter will be set only when ADSET command is executed.

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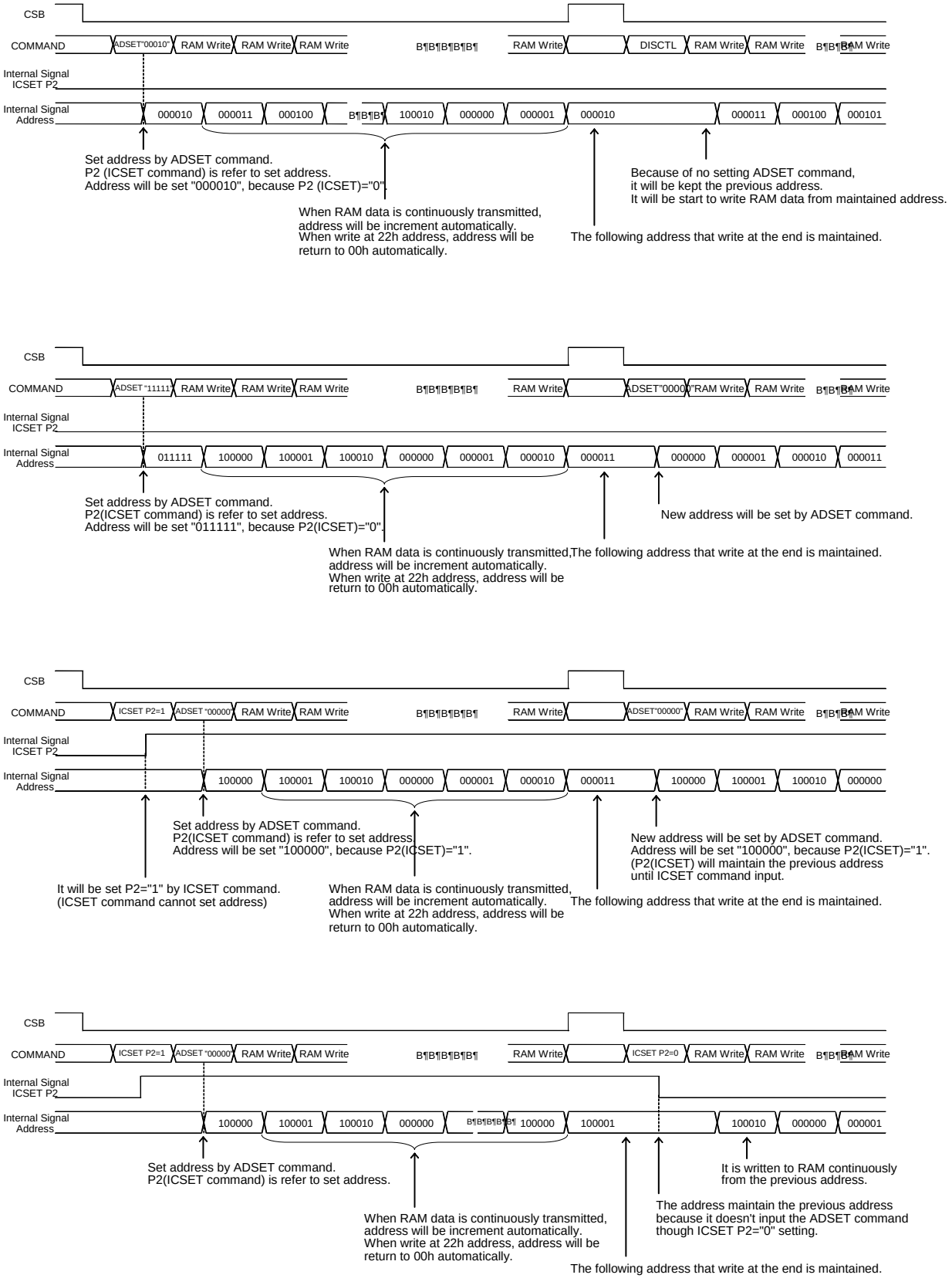

Figure 12. Address Set sequence

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(3) Display control (DISCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame frequency

Setting	P4	P3	Reset initialize condition
80Hz	0	0		
71Hz	0	1	
64Hz	1	0	
53Hz	1	1	

(Note) About the characteristics of FR, refer to Oscillation characteristics.

Set LCD drive waveform

Setting	P2	Reset initialize condition
Line inversion	0		
Frame inversion	1	

Set Power save mode

Setting	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0		
High power mode	1	1	

(Note) VDD-VLCD≥3.0V is required for High power mode.

(Reference current consumption data)

Setting	Reset initialize condition
Power save mode 1	×0.5
Power save mode 2	×0.67
Normal mode	×1.0
High power mode	×1.8

(Note) Above current consumption data is reference value. It depends on panel load.

(Note) Frame frequency / LCD drive waveform / Power save mode setting will affect display image.
Select the best value in point of current consumption and display image using LCD panel (under real application).

Mode	Screen flicker	Display image / contrast
Frame frequency			-
LCD drive waveform				
Power save mode	-		

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(4) Set IC Operation (ICSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2: MSB data of DDRAM address. Please refer to “ADSET” command.

Setting	P2	Reset initialize condition
Address MSB’0’	0		
Address MSB’1’	1	

Set Software Reset condition

Setting	P1
No operation	0
Software Reset	1

When “Software Reset” is executed, this LSI will be reset to initial condition.
If software reset is executed, the value of P2 and P1 will be ignored and they will be set initialized condition. (Refer to “Reset initial condition”)

Switch between internal clock and external clock.

Setting	P0	Reset initialize condition
Internal clock	0		
External clock input	1	

For internal clock : OSCIN is connected to VSS.
For external clock input: Input external clock into OSCIN.

<External Clock Frame frequency calculation>
DISCTL 80Hz select: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 71Hz select: Frame frequency [Hz] = external clock [Hz] / 576
DISCTL 64Hz select: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 53Hz select: Frame frequency [Hz] = external clock [Hz] / 768

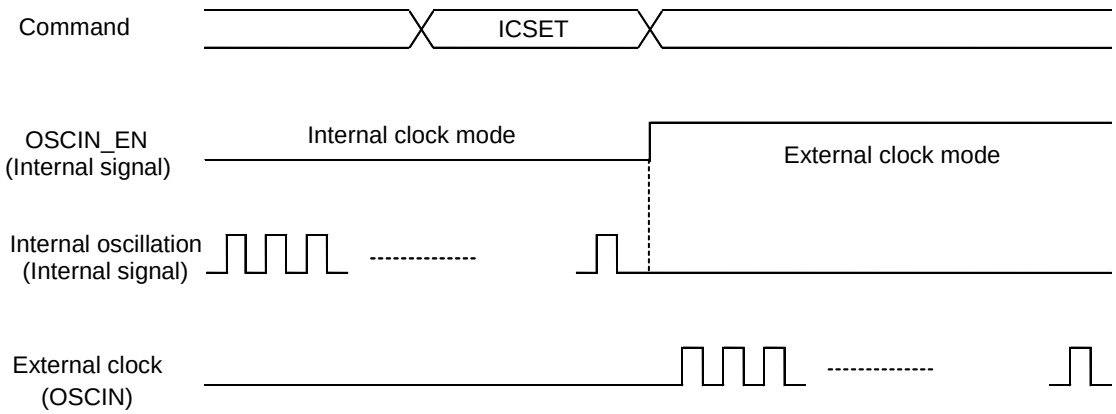

Figure 13. OSCMODE switching timing

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(5) Blink control (BLKCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

Set blink condition

Setting (Hz)	P1	P0	Reset initialize condition
OFF	0	0	|
0.5	0	1	
1	1	0	
2	1	1	

(6) All pixel control (APCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON. OFF

Setting	P1	Reset initialize condition
Normal	0	|
All pixel ON	1	

Setting	P0	Reset initialize condition
Normal	0	|
All pixel OFF	1	

All pixels ON: All pixels are ON regardless of DDRAM data.
All pixels OFF: All pixels are OFF regardless of DDRAM data.

(Note) All pixels ON/OFF is effective only at the time of “Display ON” status. The data of DDRAM do not change with this command.
If both P1 and P0=‘1’, APOFF is selected. APOFF has higher priority than APON.

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LCD Driving Waveform

(1/3bias)

Line inversion

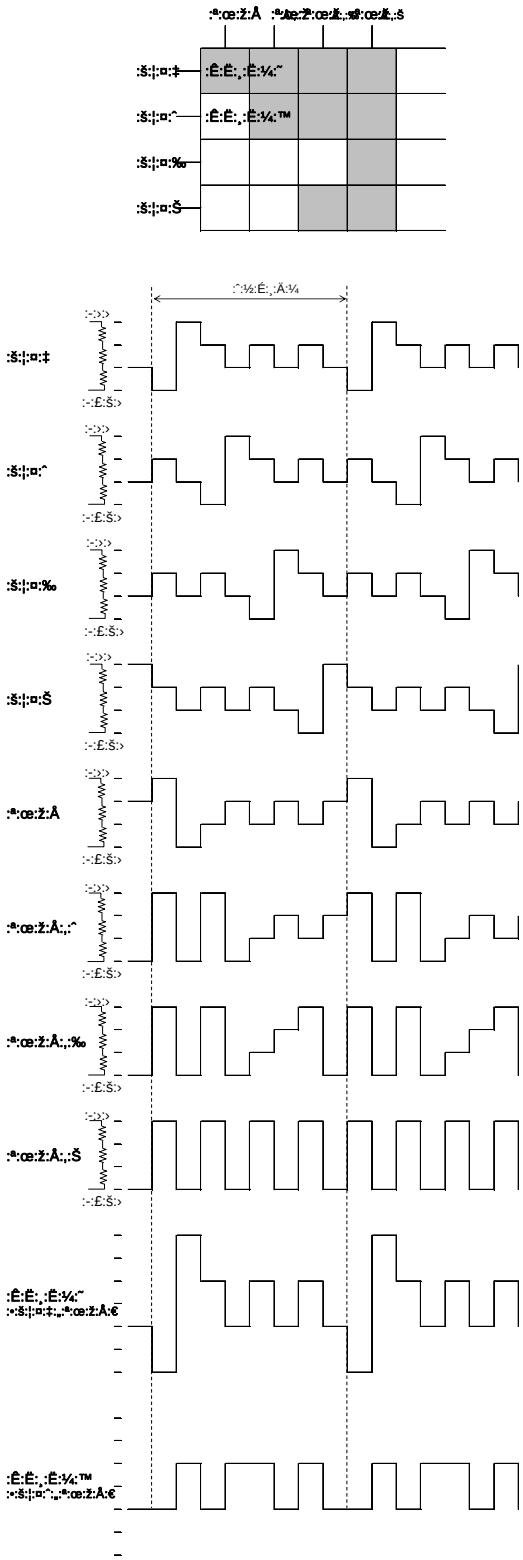

Figure 14. Line inversion waveform (1/3bias)

Frame inversion

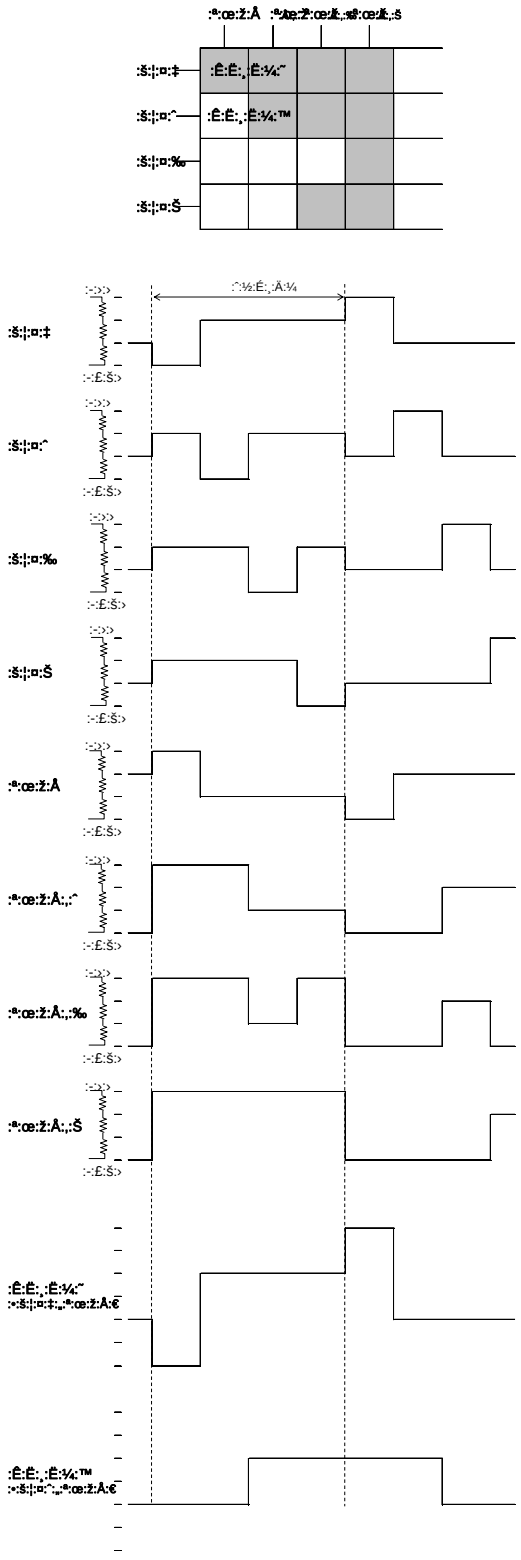

Figure 15. Frame inversion waveform (1/3bias)

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(1/2bias)

Line inversion

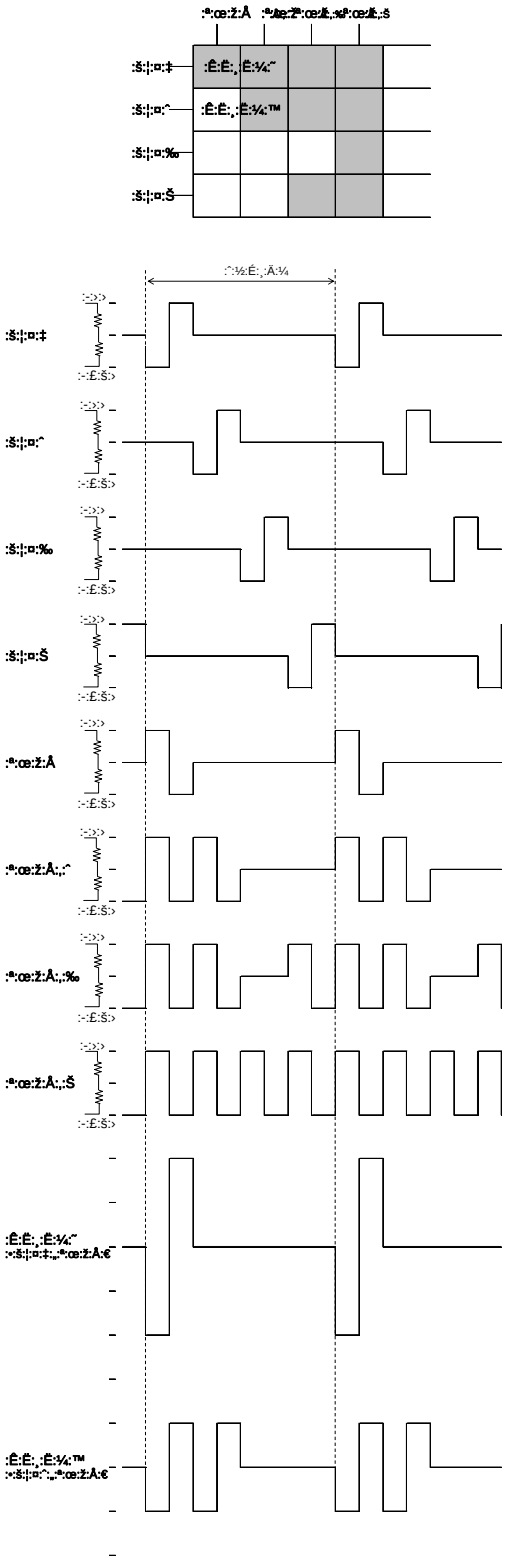

Figure 16. Line inversion waveform (1/2bias)

Frame inversion

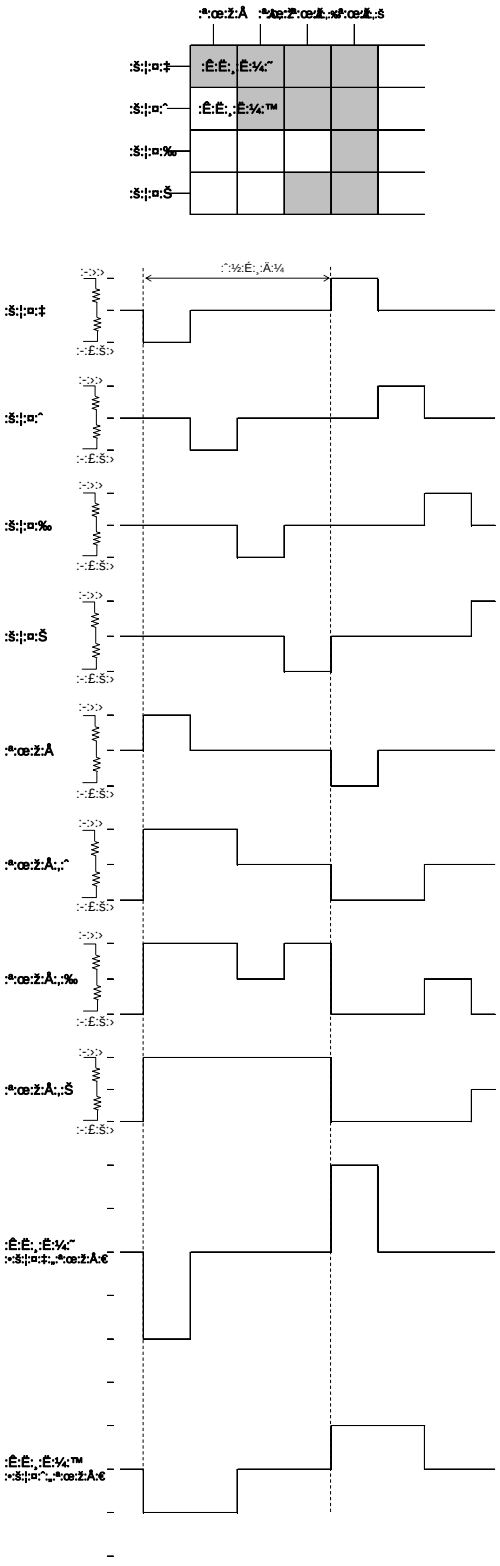

Figure 17. Frame inversion waveform (1/2bias)

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