SMBus-Controlled Level 2 Multi-Chemistry Battery Charger With Input Current Detect Comparator and Charge Enable Pin

Check for Samples :bq24747

FEATURES

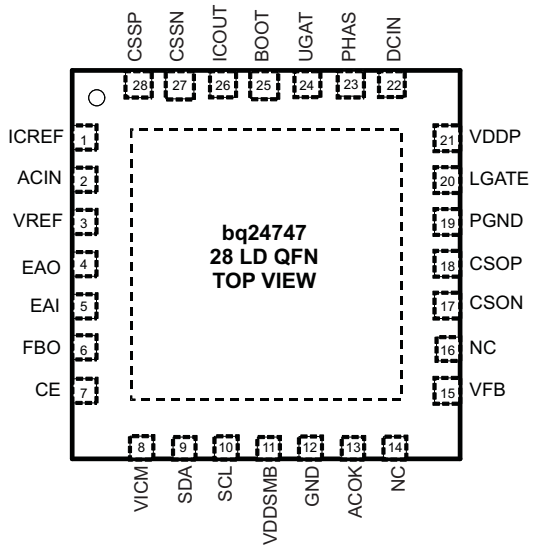
- NMOS-NMOS Synchronous Buck Converter with 300 kHz Frequency and >95% Efficiency
- 30-ns Minimum Driver Dead-time and 99.5% Maximum Effective Duty Cycle
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
  - ±2% Input Current Sense Amp Accuracy
- Integration
  - Input Current Comparator, With Adjustable Threshold and Hysteresis
  - Internal Soft-Start
- Safety
  - Input Overvoltage Protection (OVP)
  - Dynamic Power Management (DPM)
- Up to 19.2 V Battery Voltage
- 7 V–24 V AC/DC-Adapter Operating Range
- Simplified SMBus Control Interface
  - Charge Voltage DAC (1.024 V–19.2 V)
  - Charge Current DAC (128 mA–8.064 A)
  - Adapter Current Limit DPM DAC (256 mA–11.008 A)
- Status and Monitoring Outputs
  - AC/DC Adapter Present with Adjustable Voltage Threshold
  - Input Current Comparator, With Adjustable Threshold and Hysteresis
  - Current Sense Amplifier for Current Drawn From Input Source
- Charge Any Battery Chemistry: Li+, NiCd, NiMH, Lead Acid, etc.
- Charge Enable Pin
- < 10-µBattery Current with Adapter Removed
- < 1 mA Input DCIN Current with Adapter Present and Charge Disabled
- 28-pin, 5x5-mm^2 QFN Package

APPLICATIONS

- Notebook and Ultra-Mobile Computers
- Portable Data-Capture Terminals
- Portable Printers
- Medical Diagnostics Equipment
- Battery Bay Chargers
- Battery Back-up Systems

DESCRIPTION

The bq24747 is a high-efficiency, synchronous battery charger with an integrated input-current comparator, offering low component count for space-constrained, multi-chemistry battery-charging applications. The input-current, charge-current, and charge-voltage DACs allow very high regulation accuracies that can be easily programmed by the system power-management microcontroller using the SMBus interface. The bq24747 charges two, three, or four series Li+ cells, and is available in a 28-pin, 5x5 mm^2 QFN package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

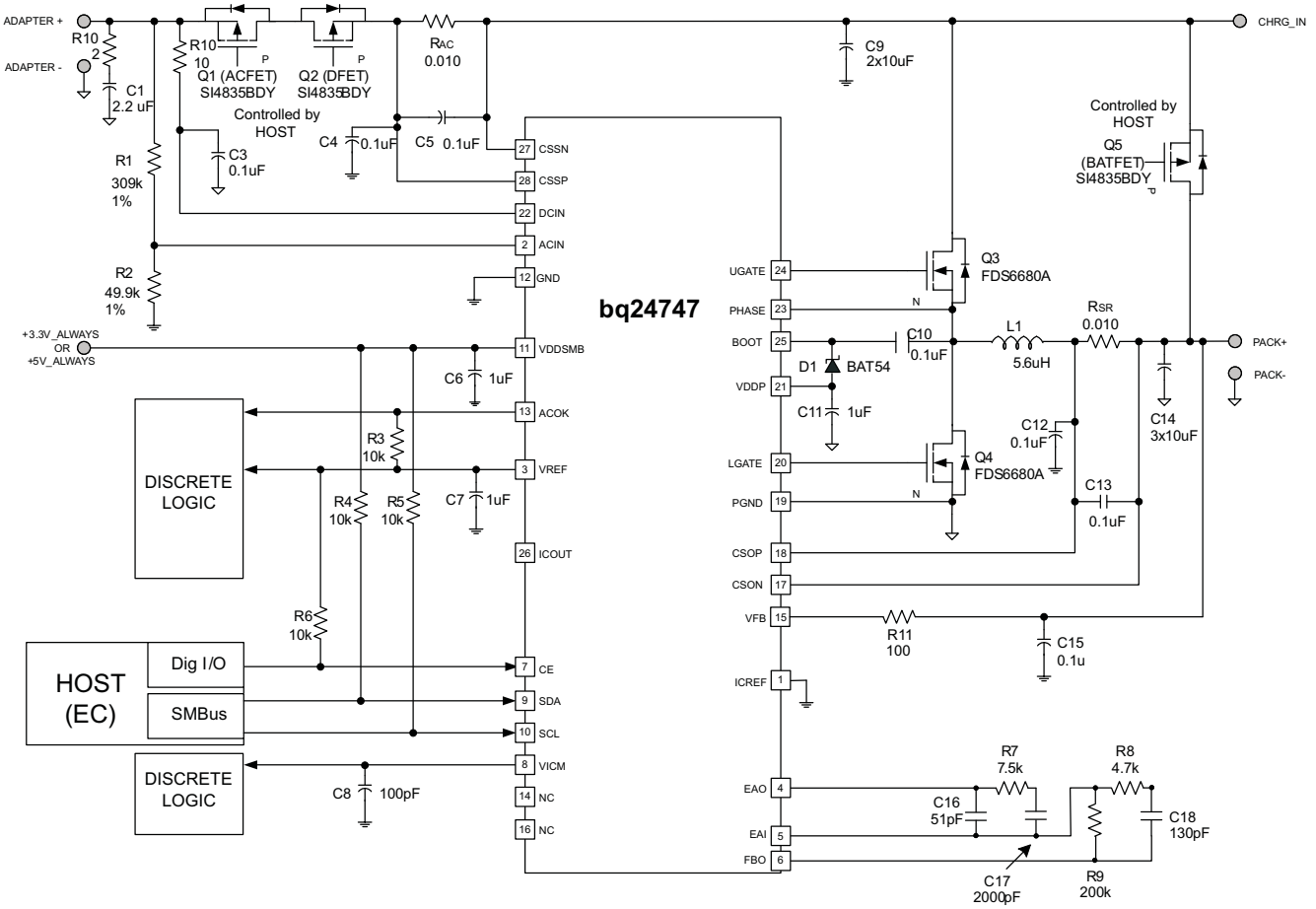
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

The bq24747 features Dynamic Power Management (DPM) and input power limiting. These features reduce battery-charge current when the input power limit is reached to avoid overloading the AC adaptor when supplying the load and the battery charger simultaneously. A highly accurate current-sense amplifier enables precise measurement of input current from the AC adapter, allowing monitoring the overall system power. If the adapter current is above the programmed low-power threshold, a signal is sent to host so that the system optimizes its performance to the power available from the adapter. An integrated comparator monitors the input current through the current-sense amplifier, and indicates when the input current exceeds a programmable threshold limit.

TYPICAL APPLICATIONS

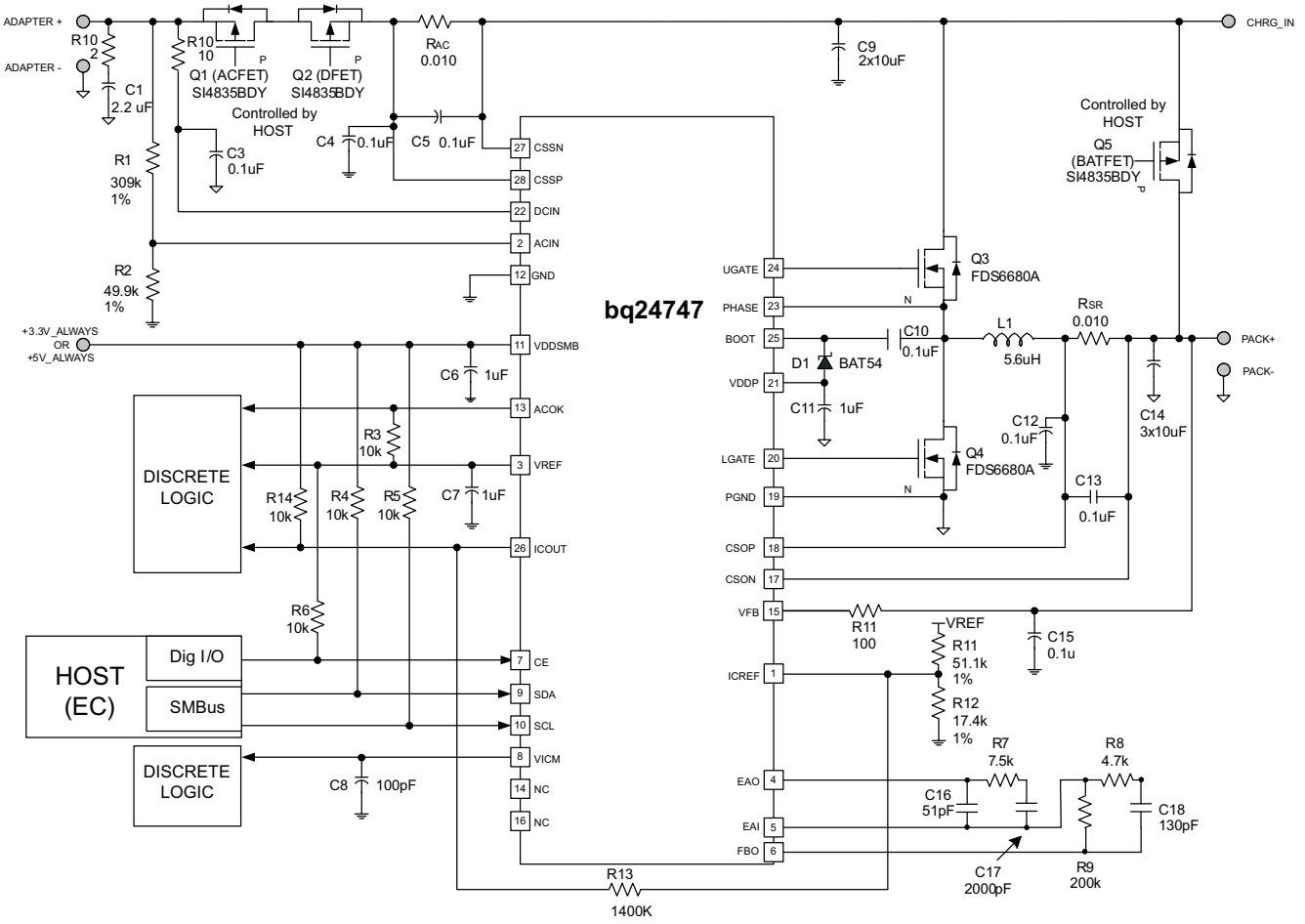
V_{IN} = 20 V, V_{BAT} = 4-cell Li-Ion, I_{CHARGE} = 4.5 A



Pull-up rail could be either VREF or other system rail.

Figure 1. Typical System Schematic: Using External Input Current Comparator (discrete logic) Instead of Internal Comparator

V_{IN} = 20 V, V_{BAT} = 4-cell Li-Ion, I_{CHARGE} = 4.5 A, $VICM_{er\_limit}$ = 6 A, for ICOUT Input Current comparator.



Pull-up rail could be either VREF or other system rail.

Figure 2. Typical System Schematic, Using Internal Input Current Comparator

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE	ORDERING NUMBER (Tape and Reel)	QUANTITY
bq24747	28-PIN 5 x 5 mm^2 QFN	bq24747RHDR	3000
		bq24747RHDT	250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A = 70°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
QFN – RHD(1)	39°C/W	2.36 W	0.028 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN

TERMINAL		FUNCTION
NO.		
1	ICREF	Input current comparator voltage reference input. Connect a resistor-divider from VREF to ICREF, and GND to program the reference for the ICOUT comparator. The ICREF pin voltage is compared to the VICM pin voltage and the logic output is given on the ICOUT open-drain pin. Connecting a positive feedback resistor from the ICREF pin to the ICOUT pin programs the hysteresis.
2	ACIN	Adapter detected voltage set input. Program the adapter detect threshold by connecting a resistor divider from adapter input to ACIN pin to GND pin. Adapter voltage is detected if ACIN pin voltage is greater than 2.4 V. VICM current sense amplifier, ICOUT comparator, ICREF input, and ACOK output are active when ACIN pin voltage is greater than 0.6 V.
3	VREF	3.3 V regulated voltage output. Place a 1 µF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for ratio metric programming of voltage and current regulation and for programming the ICREF threshold.
4	EAO	Error Amplifier Output for compensation. Connect the feedback-compensation components from EAO to EAI. Typically, a capacitor in parallel with a series resistor and capacitor. This node is internally compared to the PWM saw-tooth oscillator signal.
5	EAI	Error Amplifier Input for compensation. Connect the feedback compensation components from EAI to EAO. Connect the input compensation from FBO to EAI.
6	FBO	Feedback Output for compensation. Connect the input compensation from FBO to EAI. Typically, a resistor in parallel with a series resistor and capacitor.
7	CE	Charge enable active-high logic input. HI enables charge. LO disables charge.
8	VICM	Adapter current sense amplifier output. VICM voltage is 20 times the differential voltage across CSSP-CSSN. Place a 100pF (max) or less ceramic decoupling capacitor from VICM to GND.
9	SDA	SMBus Data input. Connect to SMBus data line from the host controller. A 10-kΩ pull-up resistor to the host controller power rail is needed.
10	SCL	SMBus Clock input. Connect to SMBus clock line from the host controller. A 10-kΩ pull-up resistor to the host controller power rail is needed.
11	VDDSMB	Input voltage for SMBus logic. Connect a 3.3 V always supply rail, or 5 V always rail to VDDSMB pin. Connect a 0.1µF ceramic capacitor from VDDSMB to GND for decoupling.
12	GND	Analog Ground. On PCB layout, connect to the analog ground plane, and only connect to PGND through the power-pad underneath the IC.
13	ACOK	Valid adapter active-high detect logic open-drain output. Pulled HI when Input voltage is above ACIN programmed threshold. Connect a 10-kΩ pull-up resistor from ACOK pin to pull-up supply rail.
14	NC	No Connect. Pin floating internally.
15	VFB	Battery-voltage remote sense. Directly connect a Kelvin sense trace from the battery-pack positive terminal to the VFB pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from VFB to GND close to the IC to filter high-frequency noise.
16	NC	No Connect. Pin floating internally.
17	CSON	Charge-current sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from CSON pin to GND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from CSON to CSOP to provide differential-mode filtering.
18	CSOP	Charge-current sense resistor, positive input. An optional 0.1-µF ceramic capacitor is placed from CSOP pin to GND for common mode filtering. An optional 0.1-µF ceramic capacitor is placed from CSON to CSOP to provide differential-mode filtering.
19	PGND	Power ground. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of input and output capacitors of the charger. Only connect to GND through the power-pad underneath the IC.
20	LGATE	PWM low-side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
21	VDDP	PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from VDDP to PGND pin, close to the IC. Use for high-side driver bootstrap voltage by connecting a small signal Schottky diode from VDDP to BOOT.
22	DCIN	IC-power positive supply. Connect to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse blocking power P-channel MOSFET. Place a 1µF ceramic capacitor from DCIN to PGND pin close to the IC.
23	PHASE	PWM high-side driver negative supply. Connect to the phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1µF bootstrap capacitor from PHASE to BOOT.
24	UGATE	PWM high-side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
25	BOOT	PWM high-side driver positive supply. Connect a 0.1µF bootstrap ceramic capacitor from BOOT to PHASE. Connect a small bootstrap Schottky diode from VDDP to BOOT.

Table 1. TERMINAL FUNCTIONS – 28-PIN QFN (continued)

TERMINAL		FUNCTION
NO.		
26	ICOUT	Input current comparator active-high open-drain logic output. Place a 10 kΩ pull-up resistor from ICOUT pin to the pull-up voltage rail. Place a positive feedback resistor from ICOUT pin to ICREF pin for programming hysteresis. The output is HI when VICM pin voltage is lower than ICREF pin voltage. The output is LO when VICM pin voltage is higher than ICREF pin voltage.
27	CSSN	Adapter current-sense resistor, negative input. An optional 0.1-µF ceramic capacitor is placed from CSSN pin to GND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from CSSN to CSSP to provide differential-mode filtering.
28	CSSP	Adapter current-sense resistor, positive input. An optional 0.1-µF ceramic capacitor is placed from CSSP pin to GND for common-mode filtering. An optional 0.1-µF ceramic capacitor is placed from CSSN to CSSP to provide differential-mode filtering.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	DCIN, CSOP, CSON, CSSP, CSSN, VFB, ACOK	–0.3 to 30	V
	PHASE	–1 to 30	
	EAI, EAO, FBO, VDDP, LGATE, ACIN, VICM, ICOUT, ICREF, CE, SDA, SCL	–0.3 to 7	
	VDDSMB	–0.3 to 5.5	
	VREF	–0.3 to 3.6	
	BOOT, UGATE with respect to GND and PGND	–0.3 to 36	
	GND, PGND	–1 to 1	
Maximum difference voltage: CSOP–CSON, CSSP–CSSN		–0.5 to 0.5	
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, and negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	PHASE	–0.7		24	V
	DCIN, CSOP, CSON, CSSP, CSSN, VFB, ACOK	0		24	
	VDDP, LGATE	0		6.5	
	VREF			3.3	
	EAI, EAO, FBO, ACIN, VICM, ICOUT, ICREF, CE, VDDSMB, SDA, SCL	0		5.5	
	BOOT, UGATE with respect to GND and PGND	0		30	
	GND, PGND	–0.3		0.3	
Maximum difference voltage: CSOP–CSON, CSSP–CSSN		–0.3		0.3	
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	

ELECTRICAL CHARACTERISTICS

7.0 V ≤ V(DCIN) ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{DCIN_OP}	DCIN input voltage operating range		7		24	V
CHARGE VOLTAGE REGULATION						
V_{VFB_OP}	VFB input voltage range		0		DCIN	V
$V_{VFB\_REG\_ACC}$	VFB charge voltage regulation accuracy	ChargeVoltage() = 0x41A0	16.716	16.8	16.884	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x3130	12.529	12.592	12.655	V
			–0.5%		0.5%	
		ChargeVoltage() = 0x20D0	8.350	8.4	8.450	V
			–0.6%		0.6%	
		ChargeVoltage() = 0x1060	4.154	4.192	4.230	V
			–0.9%		0.9%	
$V_{VFB\_REG\_RNG}$	Charge voltage regulation range	T_J = 0 to 125°C, 1.024 V–19.2 V, Max DAC value is 19.2 V	1.024		19.2	V
CHARGE CURRENT REGULATION						
$V_{IREG\_CHG\_RNG}$	Charge current regulation differential voltage range	$V_{IREG\_CHG} = V_{CSOP} – V_{CSON}$, Max DAC value is 80.64 mV	0		80.64	mV
$I_{CHRG\_REG\_ACC}$	Charge current regulation accuracy	ChargeCurrent() = 0x0F80		3968		mA
			–3%		3%	
		ChargeCurrent() = 0x0800		2048		mA
			–5%		5%	
		ChargeCurrent() = 0x0200		512		mA
			–25%		25%	
		ChargeCurrent() = 0x0080		128		mA
			–33%		33%	
INPUT CURRENT REGULATION						
$V_{IREG\_DPM\_RNG}$	Adapter current regulation differential voltage range	$V_{IREG\_DPM} = V_{CSSP} – V_{CSSN}$, Max DAC value is 110.084 mV	0		110.1	mV
$I_{INPUT\_REG\_ACC}$	Input current regulation accuracy	InputCurrent() ≥ 0x0800		4096		mA
			–3%		3%	
		InputCurrent() = 0x0400		2048		mA
			–5%		5%	
		InputCurrent() = 0x0100		512		mA
			–25%		25%	
		InputCurrent() = 0x0080		256		mA
			–33%		33%	
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACIN} > 0.6 V, 0 - 30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{ACIN} > 0.6 V	35		80	mA
VDDP REGULATOR						
V_{VDDP_REG}	VDDP regulator voltage	V_{ACIN} > 0.6 V, 0 - 50 mA	5.7	6.0	6.3	V
I_{VDDP_LIM}	VDDP current limit	V_{VDDP} = 0 V, V_{ACIN} > 0.6 V	90		135	mA
		V_{VDDP} = 5 V, V_{ACIN} > 0.6 V	80			

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V(DCIN) ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADAPTER CURRENT SENSE AMPLIFIER						
V_{CSSP/N_OP}	Input common mode range	Voltage on CSSP/CSSN	0		24	V
V_{VICM}	VICM output voltage range		0		2.25	V
A_{VICM}	Current sense amplifier voltage gain	$A_{VICM} = V_{VICM}/ V_{IREG\_DPM}$		20		V/V
	Adapter current sense accuracy	V_{IREG_DPM} = V(CSSP–CSSN) ≥ 40 mV	–2%		2%	
		V_{IREG_DPM} = V(CSSP–CSSN) =20 mV	–3%		3%	
		V_{IREG_DPM} = V(CSSP–CSSN) =5 mV	–25%		25%	
		V_{IREG_DPM} = V(CSSP–CSSN) =1.5 mV	–33%		33%	
I_{VICM_LIM}	Output current limit	V_{VICM} = 0 V	1			mA
C_{VICM_MAX}	Maximum output load capacitance	For stability with 0 mA to 1 mA load			100	pF
ACIN COMPARATOR INPUT UNDERVOLTAGE)						
$V_{DCIN\_VFB\_OP}$	Differential voltage from DCIN to VFB		–20		24	V
V_{ACIN_CHG}	ACIN rising threshold	Min voltage to enable charging, V_{ACIN} rising	2.376	2.40	2.424	V
$V_{ACIN\_CHG\_HYS}$	ACIN falling hysteresis	V_{ACIN} falling		40		mV
	ACIN rising deglitch(1)	V_{ACIN} rising	50	100	150	µs
	ACIN falling deglitch	V_{ACIN} falling		1		µs
V_{ACIN_BIAS}	Adapter present rising threshold	Min voltage to enable all bias, V_{ACIN} rising	0.56	0.62	0.68	V
$V_{ACIN\_BIAS\_HYS}$	Adapter present falling hysteresis	V_{ACIN} falling		20		mV
	ACIN rising deglitch (1)	V_{ACIN} rising		200		µs
	ACIN falling deglitch	V_{ACIN} falling		1		
DCIN / VFB COMPARATOR (REVERSE DISCHARGING PROTECTION)						
$V_{DCIN-VFB\_FALL}$	DCIN to VFB falling threshold	$V_{DCIN} – V_{VFB}$ to turn off ACFET	140	185	240	mV
$V_{DCIN-VFB\_\_HYS}$	DCIN to VFB hysteresis			50		mV
	DCIN to VFB rising deglitch	$V_{DCIN} – V_{VFB} > V_{DCIN-VFB\_RISE}$		1		ms
	DCIN to VFB falling deglitch	$V_{DCIN} – V_{VFB} < V_{DCIN-VFB\_FALL}$		3.3		µs
VFB OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Over-voltage rising threshold	As percentage of V_{VFB_REG}		104		%
V_{OV_FALL}	Over-voltage falling threshold	As percentage of V_{VFB_REG}		102		
VFB SHORT (UNDERVOLTAGE and TRICKLE CHARGE) COMPARATOR						
$V_{VFB\_SHORT\_RISE}$	VFB short rising threshold		2.4	2.7	2.9	V
$V_{VFB\_SHORT\_HYS}$	VFB short rising hysteresis			215		mV
	VFB short rising deglitch	$V_{VFB} > V_{VFB\_SHORT}+V_{VFB\_SHORT\_HYS}$ Detection delay		1.5		µs
	VFB short falling deglitch	$V_{VFB} < V_{VFB\_SHORT}$		3.3		µs
$I_{TRKL\_REG\_ACC}$	Trickle Charge current regulation accuracy in BATSHORT	$V_{VFB} < V_{VFB\_SHORT}$	60	220	300	mA
$I_{LOW\_MAX\_REG}$	Maximum Charge current regulation at Low Voltage (<4V)	$V_{VFB\_SHORT} < V_{VFB} < 4$		3		A
CHARGE OVERCURRENT COMPARATOR						
V_{OC}	Charge overcurrent falling threshold	As percentage of I_{REG_CHG}		145%		
	Minimum Current Limit (CSOP–CSON)			50		mV
	Internal Filter Pole Frequency			160		kHz
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
UVLO	AC undervoltage rising threshold	Measure on DCIN pin	3.5	4	4.5	V
V_{UVLO_HYS}	AC undervoltage hysteresis, falling			260		mV
INPUT CURRENT COMPARATOR						
V_{ICCOMP_OFFSET}	Input current comparator offset voltage		-6.8	0.12	6.8	mV

(1) Verified by design.

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V(DCIN) ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN COMPARATOR						
	VLOWV_VFB comparator			4		V
	Reset time CE after falling-edge on-shot			2		ms
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		
PWM HIGH SIDE DRIVER (UGATE)						
$R_{DS\_HI\_ON}$	High side driver (HSD) turn-on resistance	V_{BOOT} – V_{PHASE} = 5.5 V			6	Ω
$R_{DS\_HI\_OFF}$	High side driver turn-off resistance	V_{BOOT} – V_{PHASE} = 5.5 V			1	Ω
$V_{BOOT\_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BOOT} – V_{PHASE} when low side refresh pulse is requested	4			V
I_{BOOT_LEAK}	BOOT leakage current when charge enabled	High Side is on; Charge enabled			200	µA
PWM LOW SIDE DRIVER (LGATE)						
$R_{DS\_LO\_ON}$	Low side driver (LSD) turn-on resistance				6	Ω
$R_{DS\_LO\_OFF}$	Low side driver turn-off resistance				1	Ω
PWM DRIVERS TIMING						
	Driver Dead Time	Dead time when switching between LGATE and UGATE , no load at LGATE and UGATE	30			ns
PWM OSCILLATOR						
F_{SW}	PWM switching frequency		240		360	kHz
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of DCIN		6.67		%DCIN
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state battery current from CSOP, CSON, VFB, DCIN, BOOT, PHASE, etc	V_{VFB} = 16.8 V, V_{ACIN} < 0.6 V, V_{DCIN} > 5 V, 0°C ≤ T_J ≤ 85°C		7	10	µA
I_{BAT_ON}	Battery on-state quiescent current	V_{VFB} = 16.8 V, 0.6V < V_{ACIN} < 2.4 V, V_{DCIN} > 5 V		0.7	1	mA
$I_{BAT\_LOAD\_CD}$	Internal battery load current, charge disabled	Charge is disabled: V_{VFB} = 16.8 V, V_{ACIN} > 2.4 V, V_{DCIN} > 5 V		0.7	1	mA
$I_{BAT\_LOAD\_CE}$	Internal battery load current, charge enabled	Charge is enabled: V_{VFB} = 16.8 V, V_{ACIN} > 2.4 V, V_{DCIN} > 5 V	6	10	12	mA
I_{AC}	Adapter quiescent current	Charge disabled, V_{DCIN} = 20 V		0.7	1	mA
I_{AC_SWITCH}	Adapter switching quiescent current	Charge enabled, V_{DCIN} = 20 V, converter running		25		mA
INTERNAL SOFT START (8 steps to regulation current ICHG)						
	Soft start steps			8		step
	Soft start step time			1.5		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-Enable Delay after Power-up	Delay from when adapter is detected to when the charger is allowed to turn on		1.5		ms
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE SYNCHRONOUS TO NON-SYNCHRONOUS)						
V_{UCP}	Cycle-by-cycle Synchronous to Non-Synchronous Transition Threshold	Cycle-by-cycle, (CSOP-CSON) voltage, falling, LGATE turns-off and latches off until next cycle	5	10	15	mV
	Blankout Time after LGATE turns-on	Blankout comparator after LGATE turns-on		100		ns
LOGIC INPUT PIN CHARACTERISTICS (CE)(2) Pull-up CE with ≥2.2 kΩ resistor or directly to VREF.						
V_{IN_LO}	Input low threshold voltage				0.8	V
V_{IN_HI}	Input high threshold voltage		2.1			
V_{BIAS}	Input bias current	V = 0 TO V_{VDDP}			1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS (ACOK, ICOUT)						
V_{OUT_LO}	Output low saturation voltage	Sink Current = 5 mA			0.5	V

(2) Pull up CE with ≥ 2 kΩ resistor, or connect directly to VREF.

ELECTRICAL CHARACTERISTICS (continued)

7.0 V ≤ V(DCIN) ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDSMB INPUT SUPPLY FOR SMBus						
V_{VDDSMB_RANGE}	VDDSMB input voltage range		2.7		5.5	V
$V_{VDDSMB\_UVLO\_Threshold\_Rising}$	VDDSMB undervoltage lockout threshold voltage, rising	V_{VDDSMB} Rising	2.4	2.5	2.65	V
$V_{VDDSMB\_UVLO\_Hyst\_Rising}$	VDDSMB undervoltage lockout hysteresis voltage, falling	V_{VDDSMB} Falling	100	150	200	mV
IVDDSMB_Iq	VDDSMB quiescent current	V_{VDDSMB} = SCL = SDA = 5.5 V, 0°C ≤ T_J ≤ 85°C		20	27	µA

ELECTRICAL CHARACTERISTICS

7 Vdc ≤ $V_{(VCC)}$ ≤ 24 Vdc, –20°C<T_J <125°C, ref = AGND (unless otherwise noted)(1)

PARAMETER [SMB TIMING SPECIFICATION (VDD = 2.7 V to 5.5 V) (see Figures 4 and 5)]		MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS					
t_R	SCLK/SDATA rise time			1	µs
t_F	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	4		50	µs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			µs
$t_{SU(STA)}$	Setup time for START condition	4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			µs
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DAT)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			µs
$F_{S(CL)}$	Clock Frequency	10		100	kHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout	22	25	35	ms
t_{WDI}	Watchdog timeout period	140	170	210	s
OUTPUT BUFFER CHARACTERISTICS					
$V_{(SDAL)}$	Output LO voltage at SDA, $I_{(SDA)}$ = 3 mA			0.4	V

(1) Devices participating in a transfer will timeout when any clock low exceeds the 25 ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35 ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).

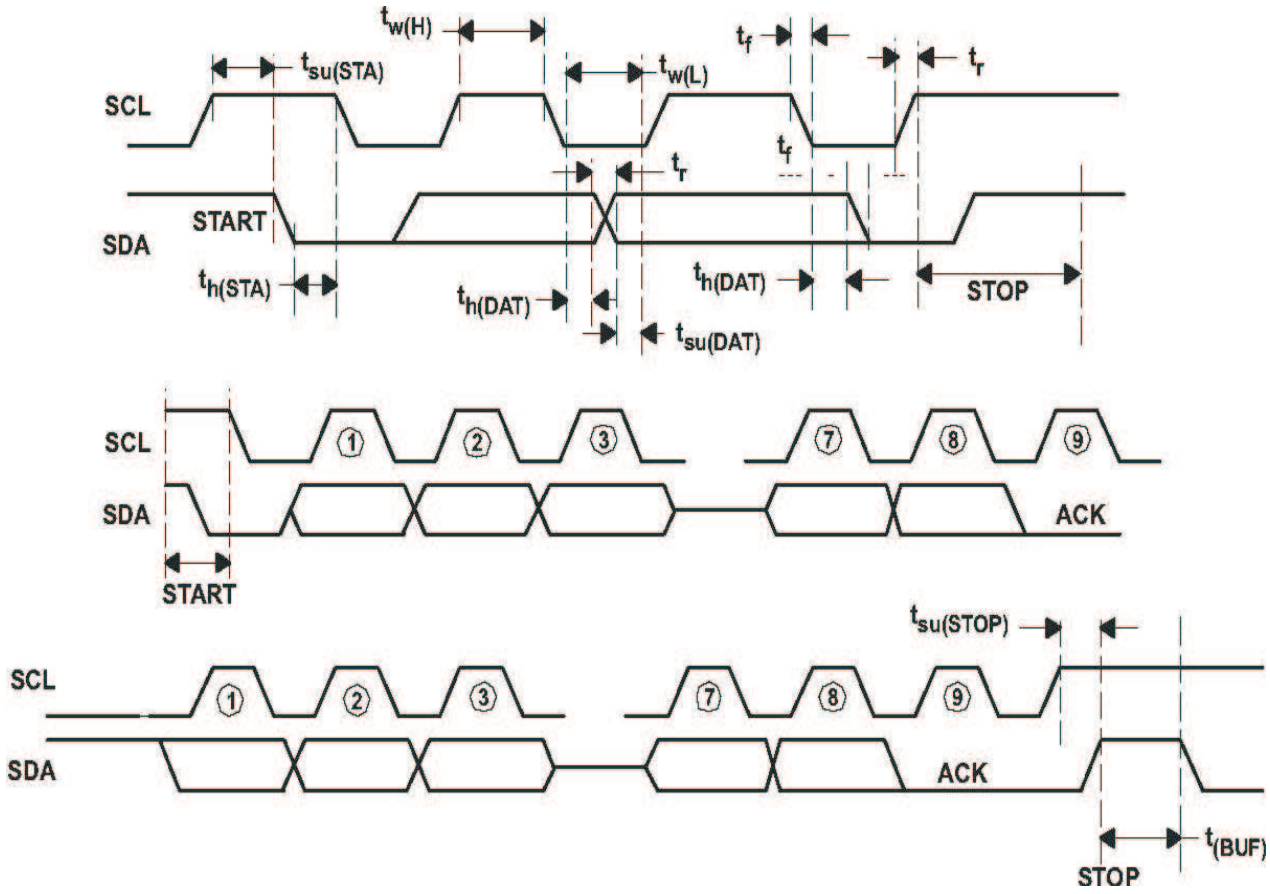


Figure 3. SMBus Communication Timing Waveforms

TYPICAL CHARACTERISTICS

VREF LOAD AND LINE REGULATION vs LOAD CURRENT

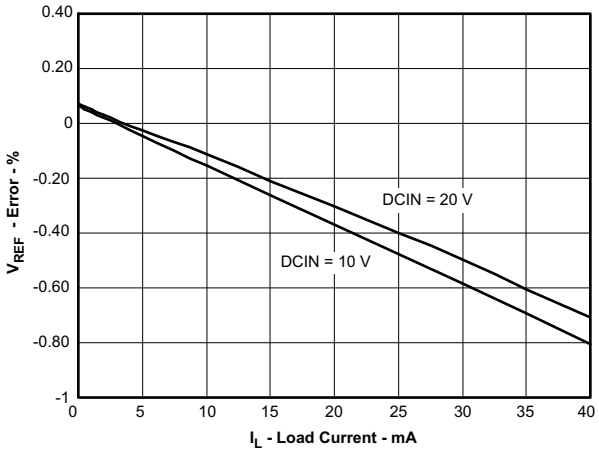


Figure 4.

VDDP LOAD AND LINE REGULATION vs LOAD CURRENT

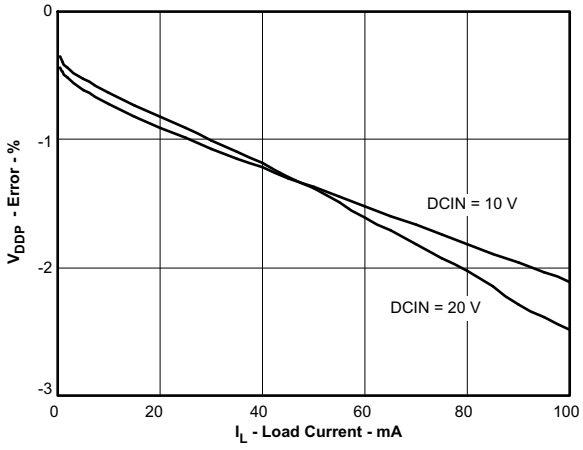


Figure 5.

TYPICAL CHARACTERISTICS (continued)

VFB (BATTERY) VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

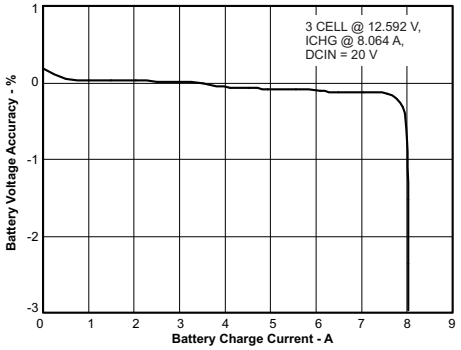


Figure 6.

VFB (BATTERY) VOLTAGE REGULATION ACCURACY vs DAC VBAT SETPOINT

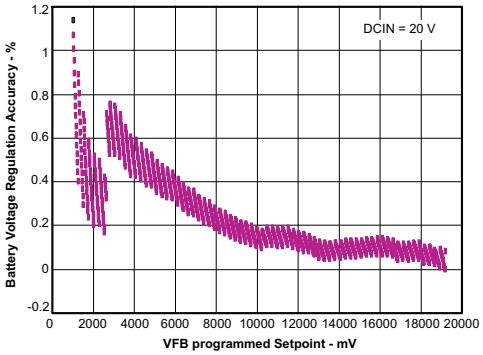


Figure 7.

CHARGE CURRENT REGULATION ACCURACY vs DAC ICHRG SETPOINT

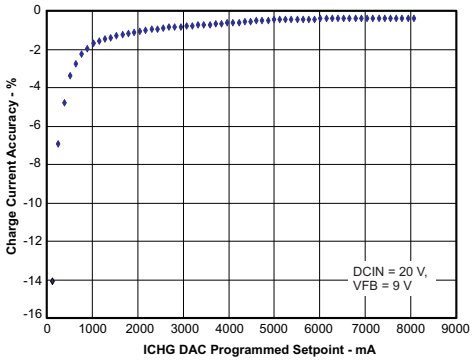


Figure 8.

CHARGE CURRENT REGULATION ACCURACY vs VFB (BATTERY) VOLTAGE

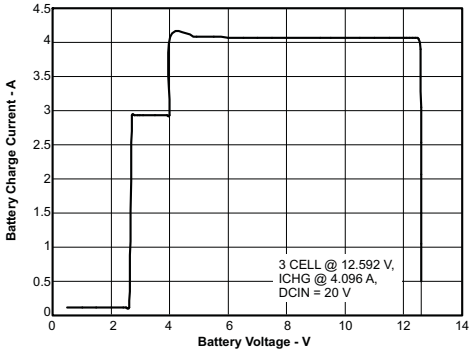


Figure 9.

INPUT CURRENT REGULATION (DPM) ACCURACY vs DAC IDPM SETPOINT

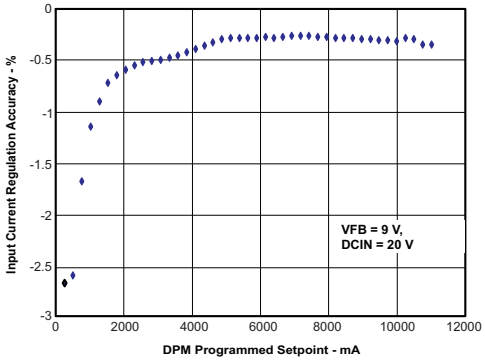


Figure 10.

VICM INPUT CURRENT SENSE AMPLIFIER ACCURACY INPUT CHARGE CURRENT

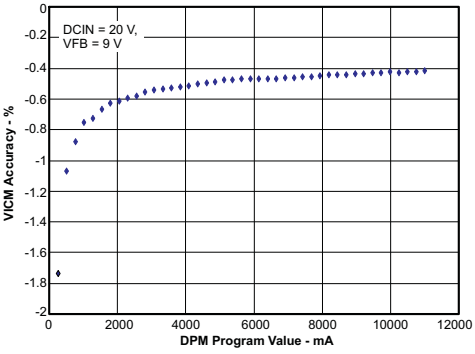


Figure 11.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT REGULATION (DPM) & CHARGE CURRENT vs SYSTEM CURRENT

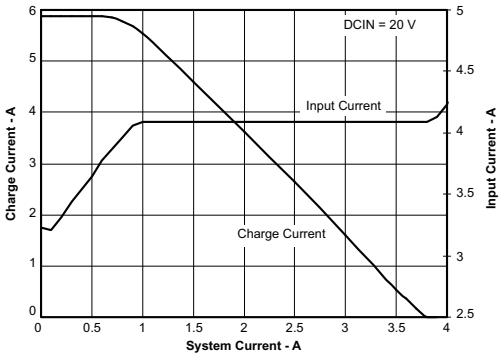


Figure 12.

INPUT CURRENT REGULATION (DPM) TRANSIENT SYSTEM LOAD RESPONSE CCM TO CCM

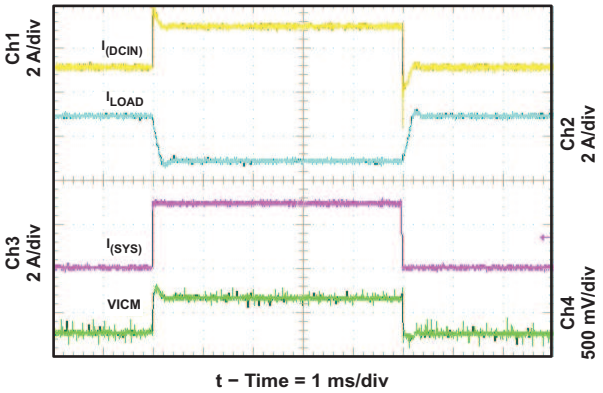


Figure 13.

INPUT CURRENT REGULATION (DPM) TRANSIENT SYSTEM LOAD RESPONSE CCM TO DCM

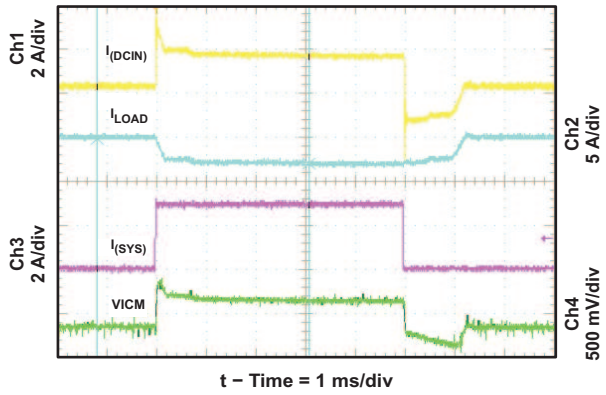


Figure 14.

CHARGE CURRENT REGULATION ACCURACY VFB (BATTERY) VOLTAGE

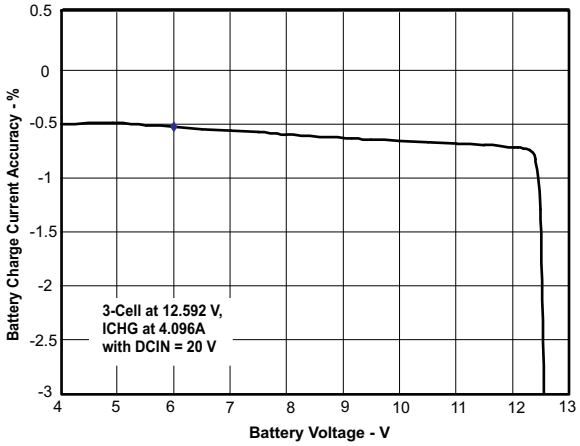


Figure 15.

EFFICIENCY BATTERY CHARGE CURRENT

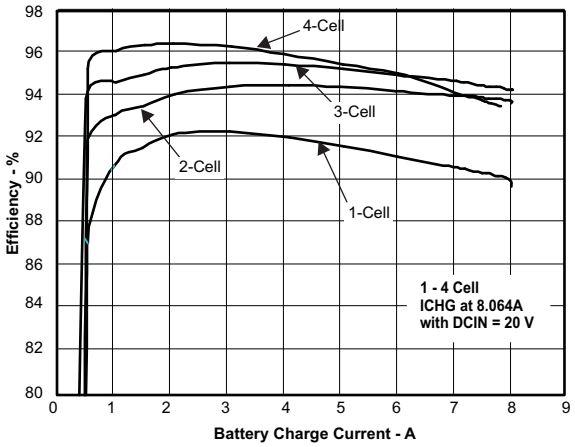


Figure 16.

BATTERY REMOVAL (From Constant Current Mode)

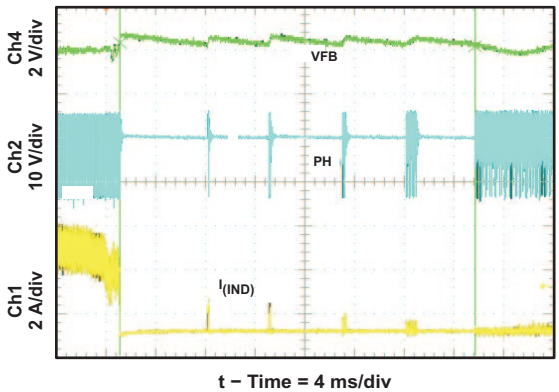


Figure 17.

TYPICAL CHARACTERISTICS (continued)

CHARGER WHEN ADAPTER INSERTED

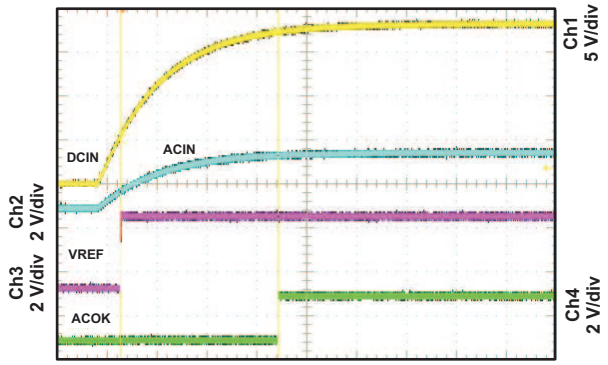


Figure 18.

ADAPTER REMOVED WHILE CHARGING

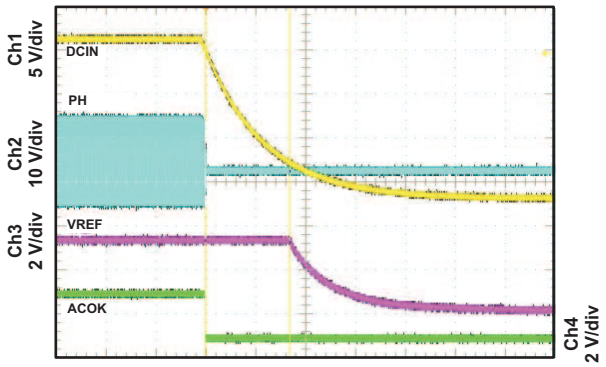


Figure 19.

CHARGE ENABLE/DISABLE

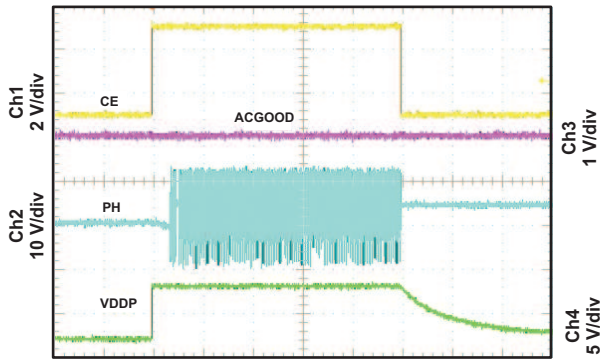


Figure 20.

SOFT-START, INDUCTOR CURRENT AND CHARGE CURRENT

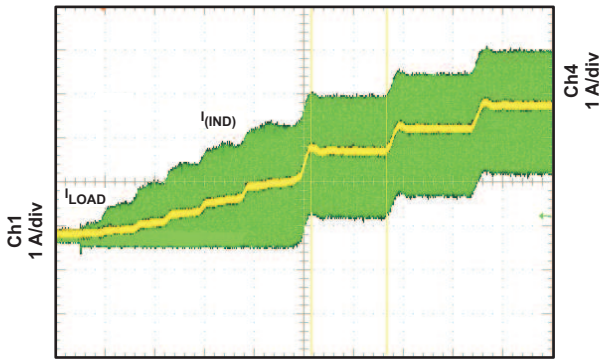


Figure 21.

CHARGE ENABLED by SMBus

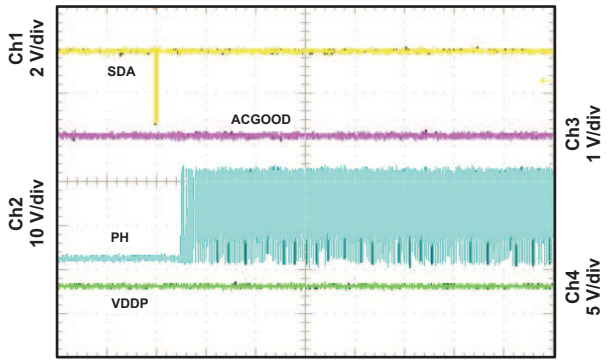


Figure 22.

CHARGE DISABLED by SMBus

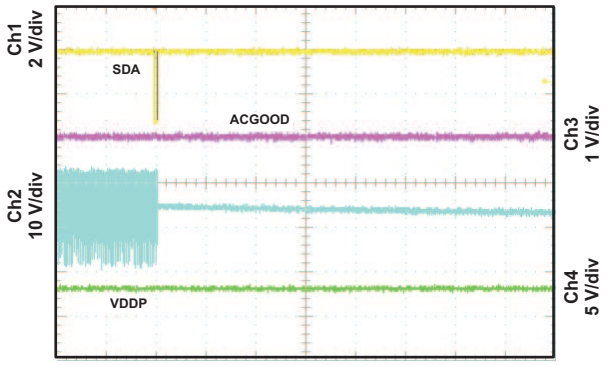


Figure 23.

TYPICAL CHARACTERISTICS (continued)

DEAD-TIME BETWEEN UGATE OFF AND LGATE ON

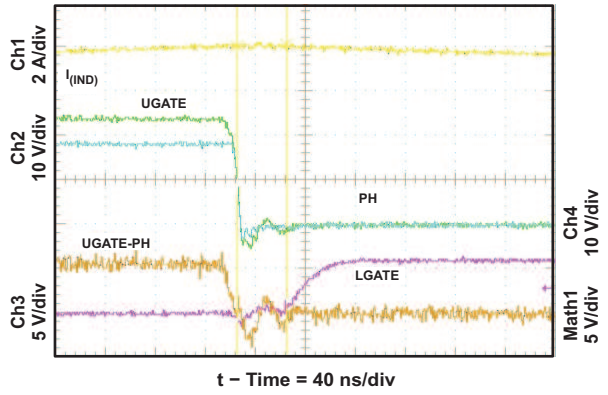


Figure 24.

DEAD-TIME BETWEEN LGATE OFF AND UGATE ON

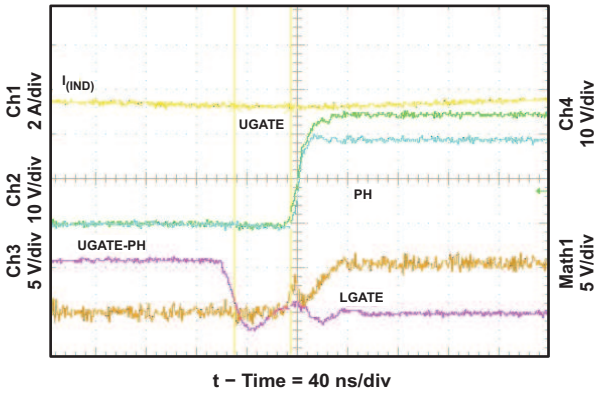


Figure 25.

NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

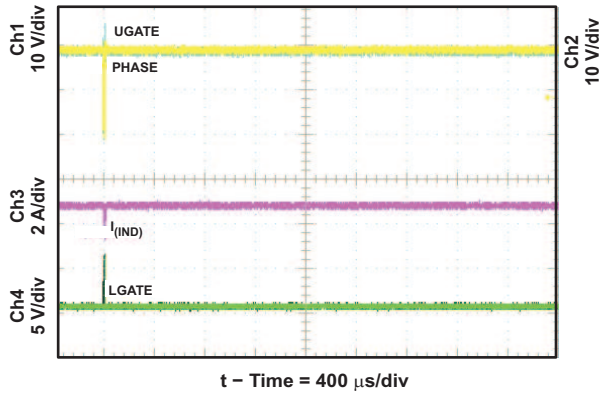


Figure 26.

BATTERY SHORTED CHARGER RESPONSE, OVERCURRENT PROTECTION (OCP) AND CHARGE CURRENT REGULATION

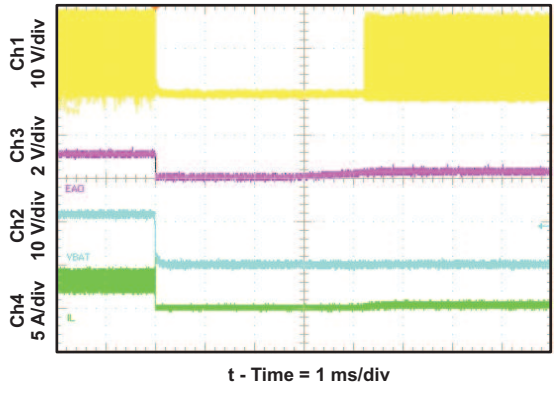


Figure 27.

CONTINUOUS CONDUCTION MODE (CCM) SWITCHING WAVEFORMS, ICHARGE = 3986 mA

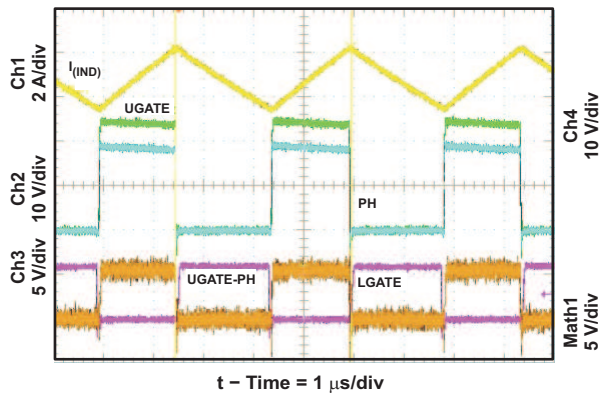


Figure 28.

DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING WAVEFORMS, ICHARGE = 256 mA

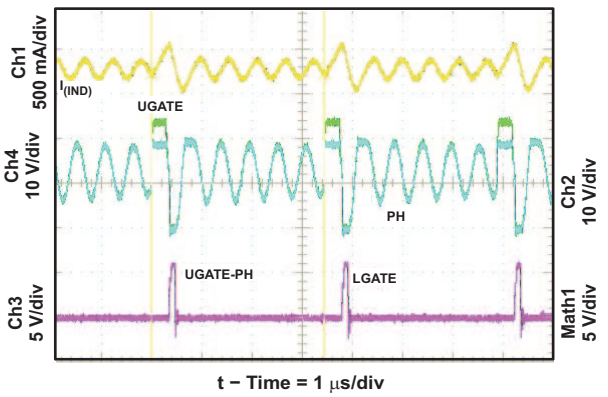


Figure 29.

TYPICAL CHARACTERISTICS (continued)

OFF-STATE BATTERY CURRENT (LOW Iq) vs VFB (BATTERY) VOLTAGE

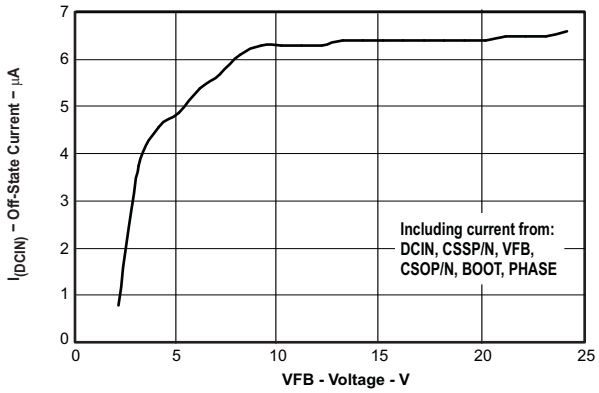


Figure 30.

OFF-STATE DCIN CURRENT (LOW Iq) vs DCIN INPUT VOLTAGE (With Adapter Connected)

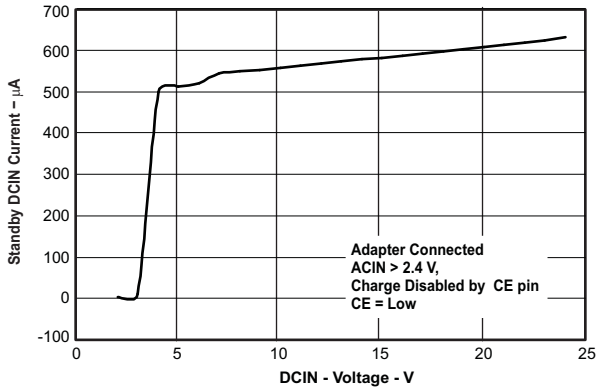
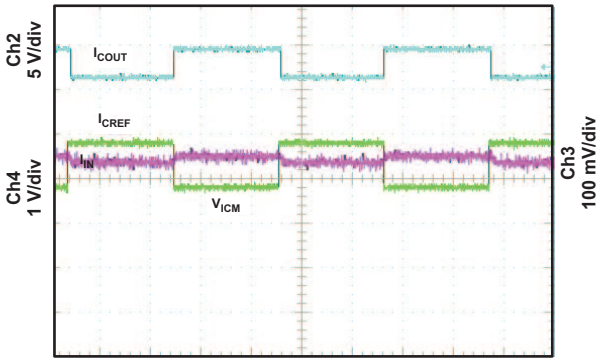


Figure 31.

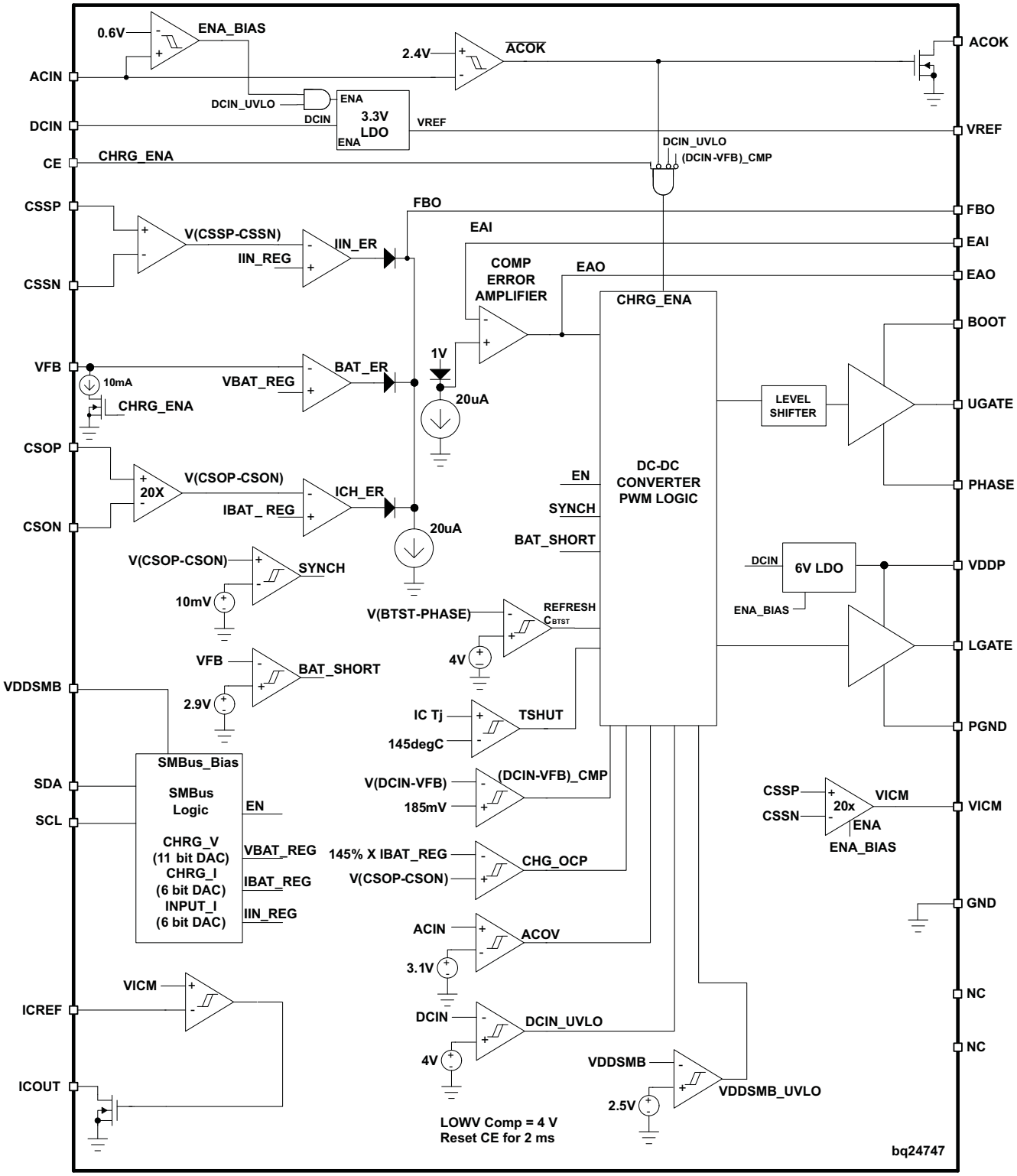
PROGRAMMABLE REFERENCE AND HYSTERESIS INPUT CURRENT COMPARATOR (With Pulsed Current)



t – Time = 4 µs/div

Figure 32.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

BATTERY VOLTAGE REGULATION

The bq24747 uses a high-accuracy voltage regulator to supply charging voltage. The battery voltage regulation setting is programmed by the host microcontroller (µC), through the SMBus interface that sets an 11-bit DAC. The input voltage range of VFB is between 1.024 V and 19.2 V. The per-cell battery termination voltage is a function of the battery chemistry. (Consult the battery manufacturer to determine this voltage.) The programmed value should be the per-cell voltage times the number of series cells.

The VFB pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1-µF ceramic capacitor from VFB to GND is recommended to be as close to the VFB pin as possible to decouple high frequency noise.

BATTERY CURRENT REGULATION

The *ChargeCurrent()* SMBus 6-bit DAC register sets the maximum charging current. Battery current is sensed by resistor R_{SR} connected between the CSOP and CSON pins. The maximum full-scale differential voltage between CSOP and CSON is 80.64 mV. Thus, for a 0.010-Ω sense resistor, the maximum charging current is 8.064 A.

The CSOP and CSON pins are used to measure the voltage across R_{SR}, which has a default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor gives a larger sense voltage and higher regulation accuracy, but at the expense of higher conduction loss.

INPUT ADAPTER CURRENT REGULATION

The total input current from an AC adapter or other DC source is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the input current exceeds the limit set by the *InputCurrent()* SMBus 6 bit DAC register. With the high-accuracy limiting, the current capability of the AC adaptor can be lowered, reducing system cost.

In a manner similar to battery-current regulation, adaptor current is sensed by resistor R_{AC} connected between the CSSP and CSSN pins. The maximum full-scale differential voltage between CSSP and CSSN is 110.08 mV. Thus, for a 0.010Ω sense resistor, the maximum input current is 11.008 A.

The CSSP and CSSN pins are used to sense R_{AC} with default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor gives a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

ADAPTER DETECT AND POWER UP

An external resistor voltage divider attenuates the adapter voltage before it goes to ACIN. The adapter-detect threshold should typically be programmed to a value greater than the maximum battery voltage and lower than the minimum allowed adapter voltage.

If DCIN is below 4 V, the charger is disabled and ACOK goes low.

If ACIN is below 0.6 V but DCIN is above 4 V, part of the bias is enabled, including a crude bandgap reference, ACFET drive and BATFET drive. VICM is disabled and pulled down to GND. The total quiescent current is less than 10µA.

When ACIN rises above 0.6 V and DCIN is above 4 V, all the bias circuits are enabled, the VDDP output goes to 6 V, and VREF goes to 3.3 V. VICM becomes valid to proportionally reflect the adapter current.

When ACIN keeps rising and passes 2.4 V, it indicates that a valid AC adapter is present. 200µs later, and the following occurs:

- ACOK is pulled high through an external pull-up resistor to the host digital voltage rail;
- The charger turns on if all the conditions are satisfied after an additional 2-ms deglitch time. (refer to *Enable and Disable Charging*)

ENABLE AND DISABLE CHARGING

The following conditions must be valid before charging is enabled:

- CE is HIGH;
- Adapter is detected (ACIN > 2.4 V);
- Adapter is higher than the DCIN-VFB threshold;
- 200µs delay is complete after adapter detected;
- VDDP and VREF are valid;
- Thermal Shutdown (TSHUT) is not active;

Any of the following conditions stop the charge cycle:

- CE is LOW;
- Adapter is removed;
- Adapter voltage is less than 250 mV above the battery;
- Adapter is over voltage;
- Charge output current is over programmed current;
- TSHUT IC temperature threshold is reached (145°C on rising-edge with 15°C hysteresis).

AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the charger regulation current every time the charger is enabled to ensure that there is no overshoot or stress on the output capacitors or the power converter. The soft-start function steps up the charge current into 8 evenly-divided steps, gradually building up to the full programmed charge current. Each step lasts approximately 1 ms, for a typical rise time of 8 ms. No external components are needed for this function.

CONVERTER OPERATION

The synchronous-buck PWM converter operates at a fixed frequency (300 kHz) in voltage mode with a feed-forward control scheme. A type-III compensation network allows the use of ceramic capacitors at the output of the converter. The input compensation stage is connected between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter has a characteristic resonant frequency that ensures sufficient phase margin for the target bandwidth.

The resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}}$$

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the converter duty cycle. The ramp height is 1/15 of the input adapter voltage, always keeping it directly proportional to the input adapter voltage. This cancels out any loop-gain variation due to an input voltage change, simplifying loop-compensation design. The ramp is offset by 250 mV in order to allow a 0% duty cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to respond to a 100% duty-cycle PWM request. The internal gate-drive logic allows a 99.98% duty cycle while ensuring that the N-channel upper device always has enough voltage to stay fully on. If the BOOT-pin-to-PHASE-pin voltage falls below 4.5 V for more than 3 cycles, the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PHASE node down and recharge the BOOT capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BOOT-PHASE) voltage is again detected falling low due to leakage current discharging the BOOT capacitor below 4 V, and the reset pulse is reissued.

The 300-kHz fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output-filter design and keeping it out of the audible-noise region. The charge-current sense resistor R_{SR}) should be positioned with half or more of the total output capacitance placed before R_{SR}, contacting both R_{SR} and the output inductor; and the remaining capacitance placed after R_{SR}. The output capacitance should be divided and placed on either side of R_{SR}. A ratio of 50:50% gives the best performance, but the node in which the output inductor and R_{SR} connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better accuracy. The type-III compensation provides phase boost near the crossover frequency to provide sufficient phase margin.

SYNCHRONOUS AND NON-SYNCHRONOUS OPERATION

The charger operates in non-synchronous mode when the sensed charge current is below the internal ISYNSET value of 13 mV (1.3 A) falling, and 0.8 mV (800 mA) rising (with built-in hysteresis). Otherwise, the charger operates in synchronous mode.

In synchronous mode, the low-side n-channel power MOSFET is on, and the high-side n-channel power MOSFET is off. The internal gate-drive logic enforces break-before-make switching to prevent shoot-through currents. During the 30-ns dead time when both FETs are off, the back diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turned on keeps the power dissipation low, and safely allows high-current charging. In synchronous mode, the inductor current is always flowing and operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

In non-synchronous operation, after the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET turns on for approximately 80 ns, then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, when the high-side power MOSFET is turned on again. The 80-ns low-side MOSFET on-time is required to ensure that the bootstrap capacitor is always charged and able to keep the high-side power MOSFET turned on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage, and can both source and sink current. The 80-ns low-side pulse pulls the PHASE node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the VDDP LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from flowing. The inductor current is blocked by the off-state low-side MOSFET, and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

In DCM operation, the loop response automatically changes, and acts as a single-pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. At very low currents, the loop response is slower, because there is less sinking current available to discharge the output voltage. At very low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80-ns recharge pulse. This should be low enough to be absorbed by the input capacitance.

When the converter goes into 0% duty cycle, neither MOSFET turns on (no 80-ns recharge pulse), and there is no discharge from the battery.

ISYNSET CONTROL (CHARGE UNDERCURRENT)

In bq24747, ISYN is the internally-set ISYNSET value as the charge-current threshold at which the charger switches from non-synchronous operation to synchronous operation. The low-side driver turns on for only 80 ns to charge the boost capacitor. This is important to prevent negative inductor current, which may cause a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This can lead to an overvoltage condition on the DCIN node, and potentially can damage the system. This programmable value allows setting the current threshold for any inductor ripple current to avoid negative inductor current. The minimum synchronous threshold should be set from 50%–100% of the inductor ripple current, where the inductor ripple current is calculated using Equation 1.

$$\frac{I_{ripple\_\max}}{2} \le I_{SYN} \le I_{ripple\_\max}$$

and

$$I_{ripple} = \frac{(V_{in} - V_{bat}) \times \frac{V_{bat}}{V_{in}} \times \frac{1}{f_s}}{L} = \frac{V_{in} \times (1-D) \times D \times \frac{1}{f_s}}{L} \quad (1)$$

Where: V_{IN_MAX}: maximum adapter voltage
V_{BAT_MIN}: minimum BAT voltage
f_S: switching frequency
L_{MIN}: minimum output inductor

The ISYNSET comparator, or charge undercurrent comparator, compares the voltage between CSOP-CSON and the 13-mV internal threshold. The threshold is set internally to 13 mV on the falling edge and 8 mV on the rising edge (with built-in hysteresis) with 10% variation.

HIGH ACCURACY VICM USING CURRENT SENSE AMPLIFIER (CSA)

An industry-standard, high-accuracy current-sense amplifier (CSA) provides an analog output voltage at the VICM pin that can be used by a host system to monitor the input current. The CSA amplifies the input sensed voltage of CSSP-CSSN by 20× through the VICM pin. The VICM output is a voltage source 20× the input differential voltage. When DCIN is above 4 V and ACIN is above 0.6 V, VICM no longer stays at ground, but becomes active. A lower voltage can be used by connecting a resistor divider from VICM to GND, while still achieving good accuracy over temperature if the resistors are matched by their thermal coefficients.

A 0.1µF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, after the 0.1µF capacitor, if additional filtering is desired. Note that adding filtering also adds additional response delay.

VDDSMB INPUT SUPPLY

The VDDSMB input provides bias power to the SMBus interface which is active when: 1) DCIN > DCIN_UVLO, 2) ACIN > 0.6 V, and 3) VDDSBM > VDDSBM_UVLO. Connect VDDSMB to an external 3.3 V or 5 V supply rail to keep the SMBus interface active while the supply to DCIN is connected. Under this condition, the internal registers are maintained, and SMBus communication can occur between the host and the charger. Bypass VDDSMB to GND with a 0.1-µF or greater ceramic capacitor. The VDDSMB UVLO threshold is 2.7 V rising and 250 mV falling (with hysteresis). The SMBus is always active and can be written to or read from whenever VDDSMB is above the VDDSMB UVLO threshold.

INPUT UNDER VOLTAGE LOCK OUT (UVLO)

The system must have a minimum 4 V DCIN voltage from the input adapter to allow proper charger operation. When the DCIN voltage is below 4 V, the bias circuits VDDP and VREF stay inactive, even with ACIN above 0.6 V.

BATTERY OVERVOLTAGE PROTECTION

The converter will not allow the high-side FET to turn-on when the battery voltage at VFB exceeds 104% of the regulation voltage set-point, until the VFB voltage returns below 101% of the regulation voltage. This allows quick response to an overvoltage condition – such as occurs when the load is removed or the battery is disconnected. A 10-mA current sink from VFB to PGND is on only during charge and allows discharging the stored output inductor energy that is transferred to the output capacitors.

BATTERY SHORTED (Battery Undervoltage) PROTECTION AND BATTERY TRICKLE CHARGING

The bq24747 has a VFB SHORT comparator monitoring the output battery VFB voltage. If the voltage falls below 2.5 V (absolute, fixed), a battery-short status is detected. The charger continues charging at the value programmed on the ChargeCurrent(0x14) register down to 2.5 V falling, and 2.7 V rising on the VFB pin.

The bq24747 automatically reduces the charge current limit to a fixed 128 mA to trickle charge the battery, when the voltage on the VFB pin falls below 2.5 V. The charge current returns to the value programmed on the ChargeCurrent(0x14) register, when the VFB pin voltage rises above 2.7 V.

This function provides short circuit protection from the battery node, and it also provides a safe trickle charge to close deeply discharged open packs.

INPUT CURRENT COMPARATOR TRIP DETECTION

To optimize system performance, the host monitors the adapter current. When the adapter current is above a threshold set via ICREF, the ICOUT pin asserts low to act as an alarm signal to the host, indicating that input power has exceeded the programmed limit, allowing the host to throttle back system power by reducing clock frequency, lowering rail voltages, or disabling parts of the system. The ICOUT pin is an open-drain output, and must have a pull-up resistor connected. The output is logic HI when the VICM output voltage [VICM = 20 × V(CSSP-CSSN)] is lower than the ICREF input voltage. The ICREF threshold is set by an external resistor divider using VREF. A hysteresis can be programmed by connecting a positive feedback resistor from the ICOUT pin to the ICREF pin.

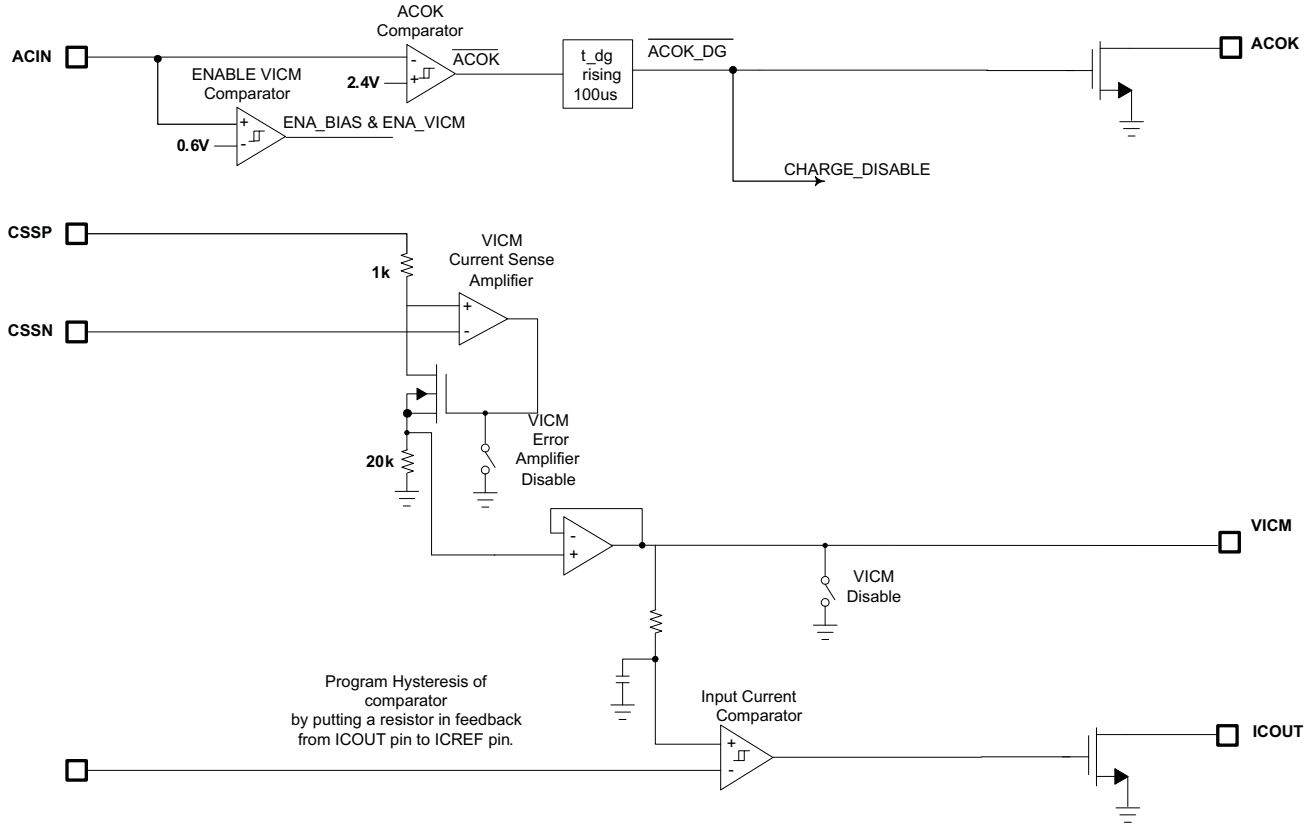


Figure 33. ACOK, ICREF, and ICOUT Logic

CHARGE OVERCURRENT PROTECTION

The charger has a secondary overcurrent monitor that prevents the charge current from exceeding 145% of the programmed charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

THERMAL SHUTDOWN PROTECTION

The QFN package has low thermal impedance, providing good thermal conduction from the silicon to the ambient air, to keep junction temperatures low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 155°C. The charger stays off until the junction temperature falls below 135°C.

OPEN-DRAIN STATUS OUTPUTS (ACOK, ICOUT)

Two status outputs are available; both require external pull up resistors to pull the pins to the system digital rail for a high level.

The ACOK open-drain output goes high when ACIN is above 2.4 V. It indicates that a functional adapter is providing a valid input voltage.

The ICOUT open-drain output goes low when the input current is higher than the threshold programmed via the ICREF pin. Hysteresis can be programmed by adding a resistor from the ICREF pin to the ICOUT pin.

SMBus INTERFACE

The bq24747 operates as a slave, receiving control inputs from the host through the SMBus interface.

BATTERY-CHARGER COMMANDS

The bq24747 supports four battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in Table 2. ManufacturerID() and DeviceID() can be used to identify the bq24747. On the bq24747, the ManufacturerID() command always returns 0x0040 and the DeviceID() command always returns 0x0006.

Table 2. Battery Charger SMBus Registers

REGISTER ADDRESS	REGISTER NAME	READ/WRITE	DESCRIPTION	POR STATE
0x14	ChargeCurrent()	Read or Write	6-Bit Charge Current Setting	0x0000
0x15	ChargeVoltage()	Read or Write	11-Bit Charge Voltage Setting	0x0000
0x3F	InputCurrent()	Read or Write	6-Bit Input Current Setting	0x0080
0xFE	ManufacturerID()	Read Only	Manufacturer ID	0x0040
0xFF	DeviceID()	Read Only	Device ID	0x0006

SMBus Interface

The bq24747 receives commands from the SMBus interface. The bq24747 uses a simplified subset of the commands documented in the *System Management Bus Specification V1.1*, which can be downloaded from www.smbus.org. The bq24747 uses the SMBus Read-Word and Write-Word protocols (see Figure 34) to communicate with the smart battery. The bq24747 performs only as an SMBus slave device with address 0b0001001_ (0x12), and does not initiate communication on the bus. In addition, the bq24747 has two identification (ID) registers (0xFE): a 16-bit device ID register and a 16-bit manufacturer ID register (0xFF).

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors (10 kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications.

Communication starts when the master signals a START condition; a high-to-low transition on SDA while SCL is high. When the master has finished communicating, the master issues a STOP condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. Figure 35 and Figure 36 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the START and STOP conditions. The SDA state changes only while SCL is low, except for the START and STOP conditions. Data is transmitted in 8-bit bytes, sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte to or from the bq24747 because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The bq24747 supports the charger commands as described in Table 5.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB L SB	0	

Preset to 0b0001001 **ChargeCurrent() = 0x14** D7 D0 D15 D8
ChargeVoltage() = 0x15
InputCurrent() = 0x3F

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 BITS	1b	1b	8 BITS	1b		7 BITS	1b	1b	8 BITS	1b	8 BITS	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

Preset to 0b0001001 ChargeSpecInfo() = 0x11 Preset to 0b0001001 D7 D0 D15 D8
ChargerStatus() = 0x13
ChargeMode() = 0x14
ChargeMode() = 0x15
ChargeMode() = 0x3F

LEGEND:
S = START CONDITION OR REPEATED START CONDITION
ACK = ACKNOWLEDGE (LOGIC-LOW)
W = WRITE BIT (LOGIC-LOW)
P = STOP CONDITION
NACK = NOT ACKNOWLEDGE (LOGIC-HIGH)
R = READ BIT (LOGIC-HIGH)

MASTER TO SLAVE
SLAVE TO MASTER

Figure 34. SMBus Write-Word and Read-Word Protocols

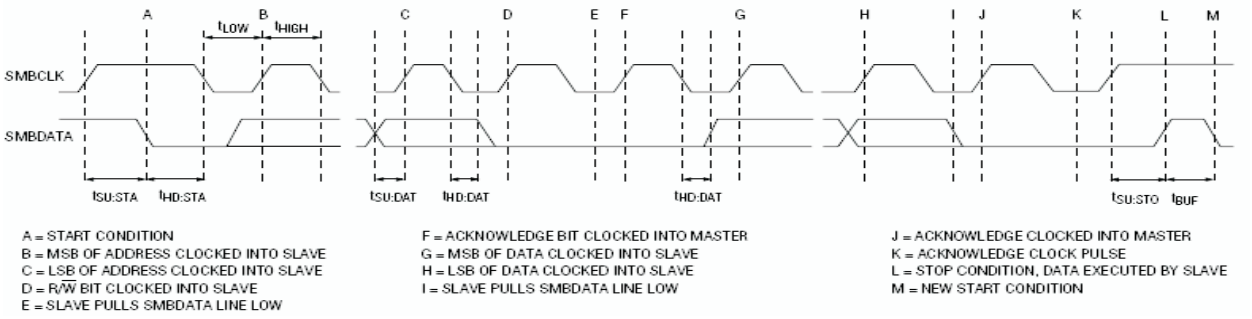
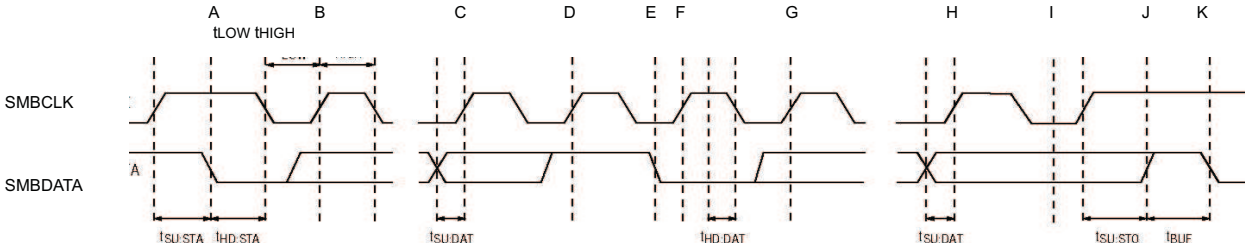


Figure 35. SMBus Write Timing



A = START CONDITION
B = MSB OF ADDRESS CLOCKED INTO SLAVE
C = LSB OF ADDRESS CLOCKED INTO SLAVE
D = R/W BIT CLOCKED INTO SLAVE
E = SLAVE PULLS SMBDATA LINE LOW
F = ACKNOWLEDGE BIT CLOCKED INTO MASTER
G = MSB OF DATA CLOCKED INTO MASTER
H = LSB OF DATA CLOCKED INTO MASTER
I = ACKNOWLEDGE CLOCK PULSE
J = STOP CONDITION
K = NEW START CONDITION

Figure 36. SMBus Read Timing

SETTING THE CHARGE VOLTAGE

To program the output charge voltage regulation setpoint, use the SMBus to write a 16-bit ChargeVoltage() command using the data format listed in Table 3. The ChargeVoltage() command uses the Write-Word protocol (see Figure 34). The command code for ChargeVoltage() is 0x15 (0b00010101). The bq24747 provides a charge-voltage range of 1.024 V to 19.200 V, with 16 mV resolution. Set ChargeVoltage() below 1.024 V to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() command are sent. Both UGATE and LGATE pins remain low until the charger is restarted.

Table 3. Charge Voltage Register (0x15)

BIT	BIT NAME	DESCRIPTION
0	–	Not used.
1	–	Not used.
2	–	Not used.
3	–	Not used.
4	Charge Voltage, DACV 0	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 16 mV of charger voltage
5	Charge Voltage, DACV 1	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 32 mV of charger voltage
6	Charge Voltage, DACV 2	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 64 mV of charger voltage.
7	Charge Voltage, DACV 3	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 128 mV of charger voltage.
8	Charge Voltage, DACV 4	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 256 mV of charger voltage.
9	Charge Voltage, DACV 5	0 = Adds 0 mV of charger voltage, 1024 mV min. 1 = Adds 512 mV of charger voltage
10	Charge Voltage, DACV 6	0 = Adds 0 mV of charger voltage. 1 = Adds 1024 mV of charger voltage.
11	Charge Voltage, DACV 7	0 = Adds 0 mV of charger voltage. 1 = Adds 2048 mV of charger voltage.
12	Charge Voltage, DACV 8	0 = Adds 0 mV of charger voltage. 1 = Adds 4096 mV of charger voltage.
13	Charge Voltage, DACV 9	0 = Adds 0 mV of charger voltage. 1 = Adds 8192 mV of charger voltage.
14	Charge Voltage, DACV 10	0 = Adds 0 mV of charger voltage. 1 = Adds 16384 mV of charger voltage.
15	–	Not used.

SETTING THE CHARGE CURRENT

To set the charge current, use the SMBus to write a 16bit ChargeCurrent() command using the data format listed in Table 4. The ChargeCurrent() command uses the Write-Word protocol (see Figure 34). The command code for ChargeCurrent() is 0x14 (0b00010100). When using a 10-mΩ sense resistor, the bq24747 provides a charge-current range of 128 mA to 8.064 A, with 128 mA resolution. Set ChargeCurrent() to 0 to terminate charging. Upon reset, the ChargeVoltage() and ChargeCurrent() values are cleared and the charger remains off until both the ChargeVoltage() and the ChargeCurrent() commands are received. Both UGATE and LGATE pins remain low until the charger is restarted.

The bq24747 includes a foldback current limit when the battery voltage is low. If the battery voltage is less than 2.5 V, the charge current is temporarily set to 128 mA. The ChargeCurrent() register value is preserved, and becomes active again when the battery voltage is higher than 2.7 V. This function effectively provides a fold-back current limit, protecting the charger during short circuit and overload.

Table 4. Charge Current Register (0x14), Using 10mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	–	Not used.
1	–	Not used.
2	–	Not used.
3	–	Not used.
4	–	Not used.
5	–	Not used.
6	–	Not used.
7	Charge Current, DACI 0	0 = Adds 0 mA of charger current 1 = Adds 128 mA of charger current.
8	Charge Current, DACI 1	0 = Adds 0 mA of charger current 1 = Adds 256 mA of charger current.
9	Charge Current, DACI 2	0 = Adds 0 mA of charger current 1 = Adds 512 mA of charger current
10	Charge Current, DACI 3	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
11	Charge Current, DACI 4	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
12	Charge Current, DACI 5	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current, 8064 mA.
13	–	Not used.
14	–	Not used.
15	–	Not used.

SETTING THE INPUT CURRENT

System current normally fluctuates as portions of the system are powered up or down, or enter low-power mode. By using the input-current limit circuit, the output-current requirement of the AC wall adapter can be lowered, reducing system cost.

The total input current, from a power-line wall adapter or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the programmed input current limit, the bq24747 decreases the charge current to provide priority to the system load current. As the system supply current rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit.

The internal amplifier compares the differential voltage between CSSP and CSSN to a scaled voltage set by the InputCurrent() command (see Table 5). The total input current is the sum of the device supply current, the charger input current, and the system load current. The total input current can be estimated as follows:

Table 5. Input Current Register (0x3F), Using 10mΩ Sense Resistor

BIT	BIT NAME	DESCRIPTION
0	–	Not used.
1	–	Not used.
2	–	Not used.
3	–	Not used.
4	–	Not used.
5	–	Not used.
6	–	Not used.
7	Input Current, DACS 0	0 = Adds 0 mA of charger current 1 = Adds 256 mA of charger current.
8	Input Current, DACS 1	0 = Adds 0 mA of charger current 1 = Adds 512 mA of charger current
9	Input Current, DACS 2	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
10	Input Current, DACS 3	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
11	Input Current, DACS 4	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current
12	Input Current, DACS 5	0 = Adds 0 mA of charger current. 1 = Adds 8192 mA of charger current, 11008 mA max.
13	–	Not used.
14	–	Not used.
15	–	Not used.

$$I_{INPUT} = I_{LOAD} + \left[\frac{I_{LOAD} \times V_{BATTERY}}{V_{IN} \times \eta} \right] + I_{BIAS} \quad (2)$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

To set the input current limit, write a 16-bit InputCurrent() command using the data format listed in Table 5. The InputCurrent() command uses the Write-Word protocol (see Figure 34). The command code for InputCurrent() is 0x3F (0b00111111). When using a 10-mΩ sense resistor, the bq24747 provides an input-current limit range of 256 mA to 11.008 A, with 256 mA resolution. InputCurrent() settings from 1 mA to 256 mA result in a current limit of 256 mA. Upon reset the input current limit is 256 mA.

CHARGER TIMEOUT

The bq24747 includes a timer to terminate charging if the charger does not receive a ChargeVoltage() or ChargeCurrent() command within 175 s. If a timeout occurs, both ChargeVoltage() and ChargeCurrent() commands must be resent to re-enable charging.

REMOTE SENSE

The bq24747 has a dedicated remote sense pin, VFB, which allows the rejection of board resistance and selector resistance. To fully utilize remote sensing, connect VFB directly to the battery interface through an unshared battery-sense Kelvin trace, and place a 0.1-µF ceramic capacitor near the VFB pin to GND (see Figure 1).

Remote Kelvin Sensing provides higher regulation accuracy, by eliminating parasitic voltage drops. Remote sensing cancels the effect of impedance in series with the battery. This impedance normally causes the battery charger to prematurely enter constant-voltage mode with reducing charge current.

INPUT CURRENT MEASUREMENT

Use VICM to monitor the system-input current sensed across CSSP and CSSN. The voltage at VICM is proportional to the input current by the equation:

$$VICM = 20 \times V_{(CSSP-CSSN)} = 20 \times (I_{in} \times R_{sense})$$

where I_{in} is the input DC current supplied by the AC adapter, 20 is the gain, and R_{sense} is the input sense resistor. VICM has a 0 to (VREF–100 mV) output voltage range. Leave VICM open if not used. Use a 100 pF (maximum) ceramic capacitor.

VDDP GATE DRIVE REGULATOR

An integrated low-dropout (LDO) linear regulator provides a 6-V supply derived from DCIN, for high efficiency, and delivers over 75 mA of load current. The LDO powers the gate drivers of the n-channel MOSFETs. VDDP has a minimum current limit of 90 mA. This allows the bq24747 to work with high gate charge (both high-side and low-side) MOSFETs. Bypass VDDP to PGND with a 1-µF or greater ceramic capacitor.

AC ADAPTER DETECTION

The bq24747 includes a hysteretic comparator that detects the presence of an AC power adapter. When ACIN is greater than 2.4 V, the open-drain ACOK output becomes high impedance. Connect a 10-kΩ pullup resistor between the pull-up rail and ACOK. Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Select the resistive voltage-divider not to exceed the 7 V absolute maximum rating of ACIN.

OPERATING CONDITIONS

The bq24747 has the following operating states:

- **Adapter Present:** When DCIN is greater than 4 V and ACIN is greater than 2.4 V, the adapter is considered to be present. In this condition, both the VDDP and VREF function properly and battery charging is allowed:
  - **Charging:** The total bq24747 quiescent current when charging is 1 mA (max) plus the current required to drive the MOSFETs.
  - **Not Charging:** To disable charging, set either ChargeCurrent() or ChargeVoltage() to zero. When the adapter is present and charging is disabled, the total adapter quiescent current is less than 1.5 mA and the total battery quiescent current is less than 200 µA.
- **Adapter Absent (Power Fail):** When VCSSP is less than VCSON + 150 mV, the bq24747 is in the power-fail state, since the DC-DC converter is in dropout. The charger does not attempt to charge in the power-fail state. Typically, this occurs when the adapter is absent. When the adapter is absent, the total bq24747 quiescent battery current is less than 1µA (max).
- **VDDSMBus Undervoltage (POR):** When VDD is less than 2.5 V, the VDD supply is in an undervoltage state and the internal registers are in their power-on-reset (POR) state. The SMBus interface does not respond to commands. When VDD rises above 2.7 V, the bq24747 is in a power-on-reset state. Charging does not occur until the ChargeVoltage() and ChargeCurrent() commands are sent. When VDD is greater than 2.5 V, SMBus register contents are preserved.

The bq24747 allows charging under the following conditions:

1. DCIN > 4 V, VDDP > 4 V, VREF > 3.1 V
2. VCSSP > VCSON + 250 mV (15 mV falling threshold)
3. VDDSMBus > 2.5 V

Charge Termination for Li-Ion or Li-Polymer

The primary termination method for Li-Ion and Li-Polymer is minimum current. Secondary temperature termination also provides additional safety. The host controls the charge initiation and the termination. A battery pack gas gauge assists the hosts on setting the voltages and determining when to terminate based on the battery pack state of charge.

Component List for Typical System Circuit of Figure 2

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30V, –6A, SO-8, Vishay-Siliconix, Si4435
Q4, Q2	2	N-channel MOSFET, 30V, 12.5A, SO-8, Fairchild, FDS6680A
D1	1	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
RAC, RSR	2	Sense Resistor, 10 m W, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 10µH, 7A, 31m Vishay-Dale, IHLP5050FD-01
C1, C6, C7, C11, C12	5	Capacitor, Ceramic, 10µF, 35V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C4, C8, C10	3	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C2, C3, C9, C13–C15	6	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C5	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0805, Kemet
R3, R4, R5	3	Resistor, Chip, 10kΩ, 1/16W, 5%, 0402
R1	1	Resistor, Chip, 432kΩ, 1/16W, 1%, 0402
R2	1	Resistor, Chip, 66.5kΩ, 1/16W, 1%, 0402
R6	1	Resistor, Chip, 33kΩ, 1/16W, 5%, 0402
R7	1	Resistor, Chip, 200kΩ, 1/16W, 1%, 0402
R8	1	Resistor, Chip, 24.9kΩ, 1/16W, 1%, 0402
R9	1	Resistor, Chip, 1.8MΩ, 1/16W, 1%, 0402
R10	1	Resistor, 10Ω
R11	1	Resistor, 100Ω, 1/16W, 5%, 0402

GLOSSARY

VICM Output Voltage of Input Current Monitor

ICREF Input Current Reference - sets the threshold for the input current limit

DPM Dynamic Power Management

CSOP, CSON Current Sense Output of battery positive and negative

These pins are used with an external low-value series resistor to monitor the current to and from the battery pack.

CSSP, CSSN Current Sense Supply positive and negative

These pins are used with an external low-value series resistor to monitor the current from the adapter supply.

POR Power on reset

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24747RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24747RHDT	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

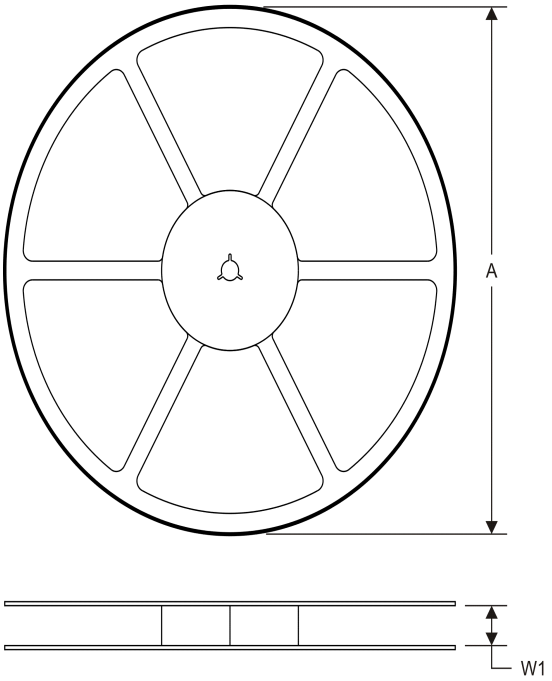
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

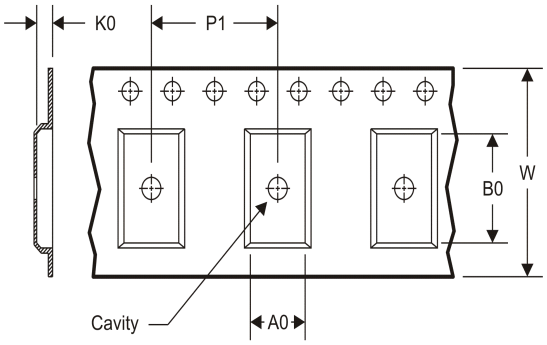
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



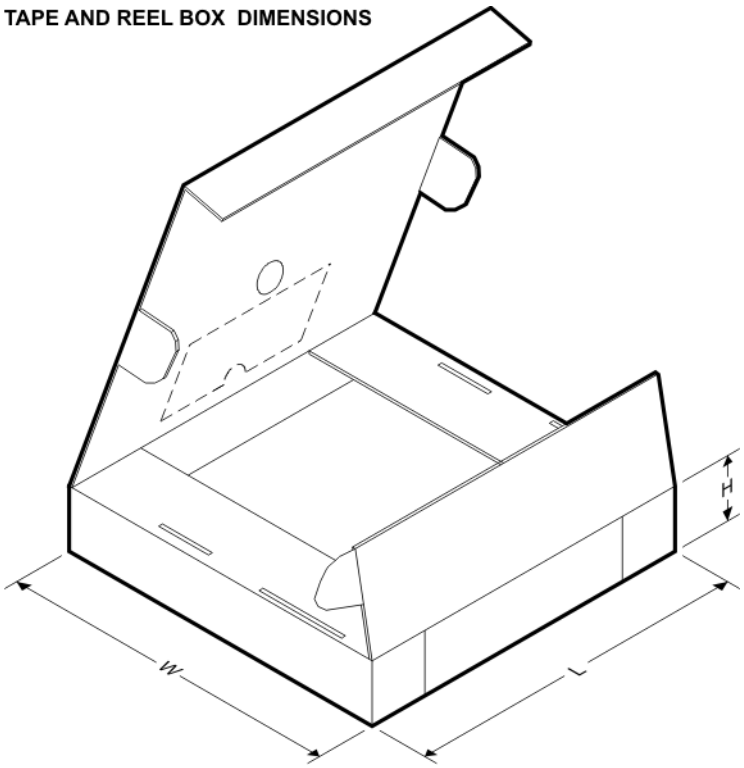
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24747RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24747RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24747RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
BQ24747RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

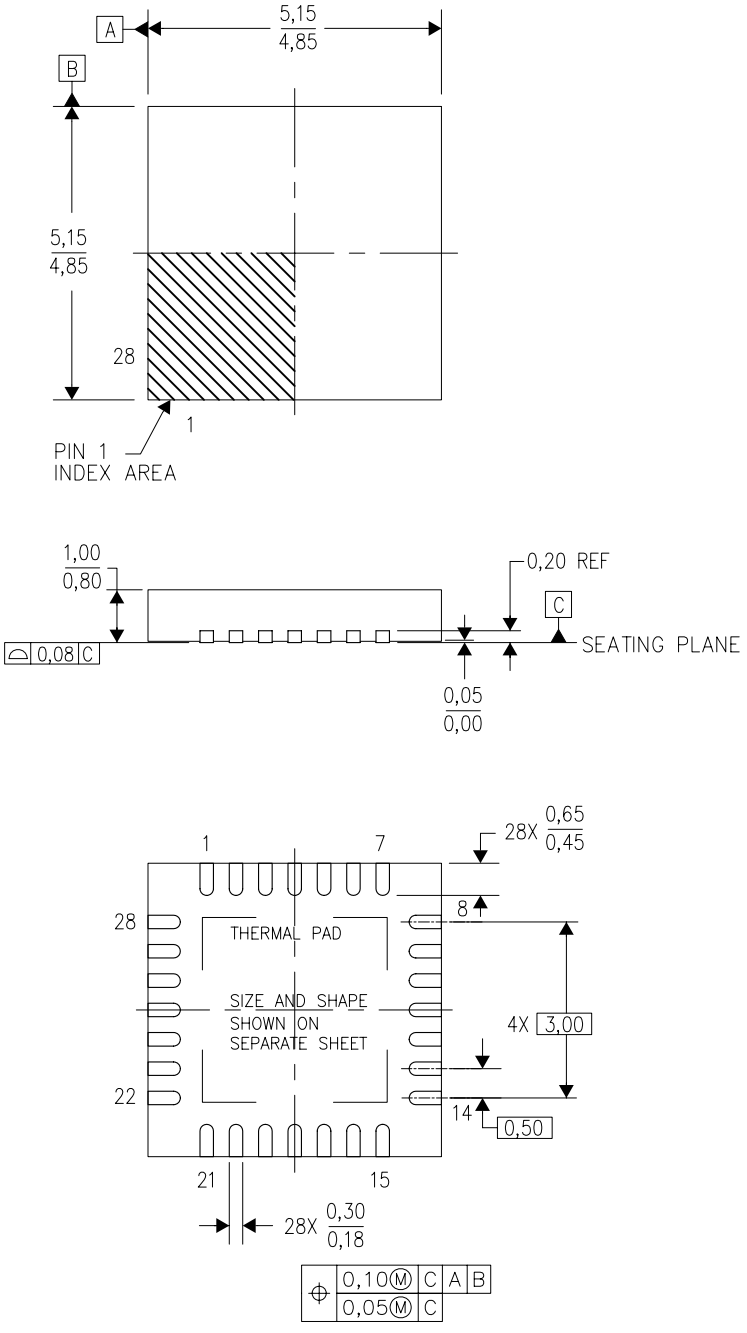
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24747RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24747RHDR	VQFN	RHD	28	3000	346.0	346.0	29.0
BQ24747RHDT	VQFN	RHD	28	250	210.0	185.0	35.0
BQ24747RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

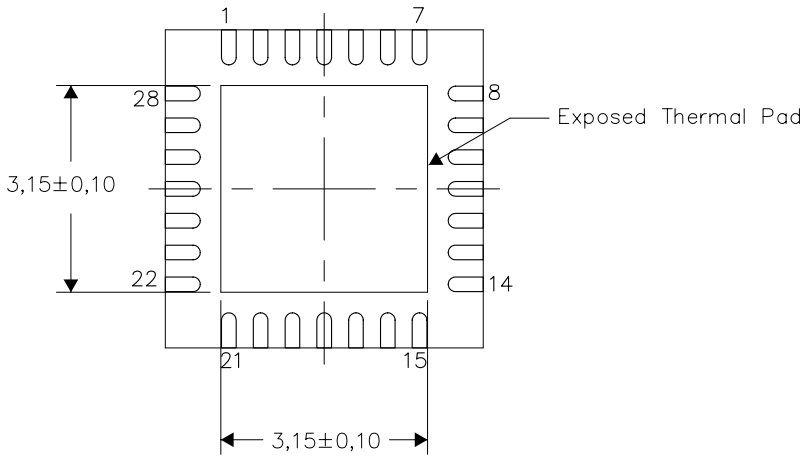
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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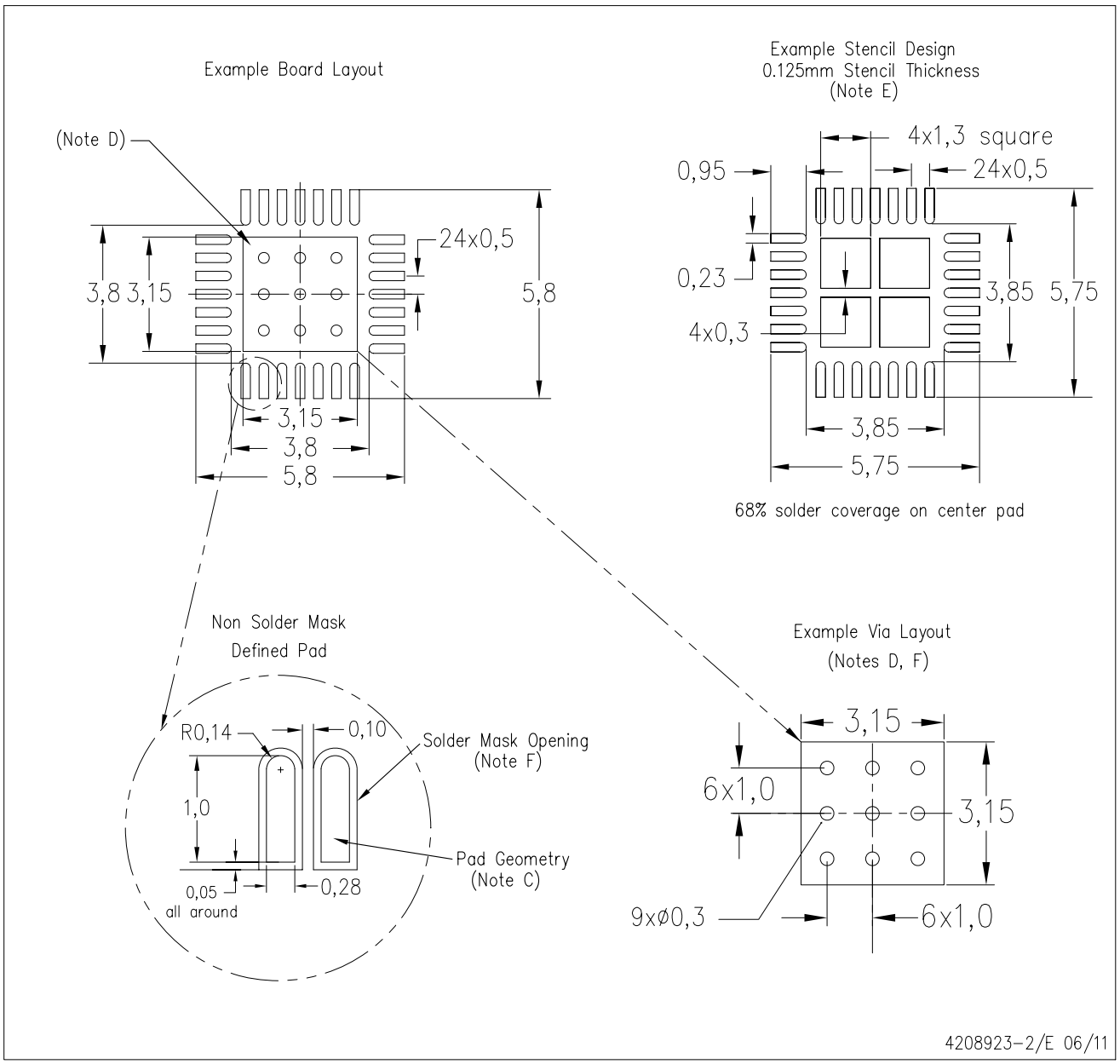
NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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