BLM7G1822S-20PB; BLM7G1822S-20PBG

LDMOS 2-stage power MMIC

Rev. 5 — 27 February 2018

AMPLEON

Product data sheet

1. Product profile

1.1 General description

The BLM7G1822S-20PB(G) is a dual section, 2-stage power MMIC using Ampleon's state of the art GEN7 LDMOS technology. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 1805 MHz to 2170 MHz. Available in gull wing or straight lead outline.

Table 1. Performance

Typical RF performance at T_{case} = 25 °C; I_{Dq1} = 27 mA; I_{Dq2} = 76 mA.
Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF; per section unless otherwise specified in a class-AB production circuit.

Test signal	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
single carrier W-CDMA	2167.5	28	2	32.3	23	–41

1.2 Features and benefits

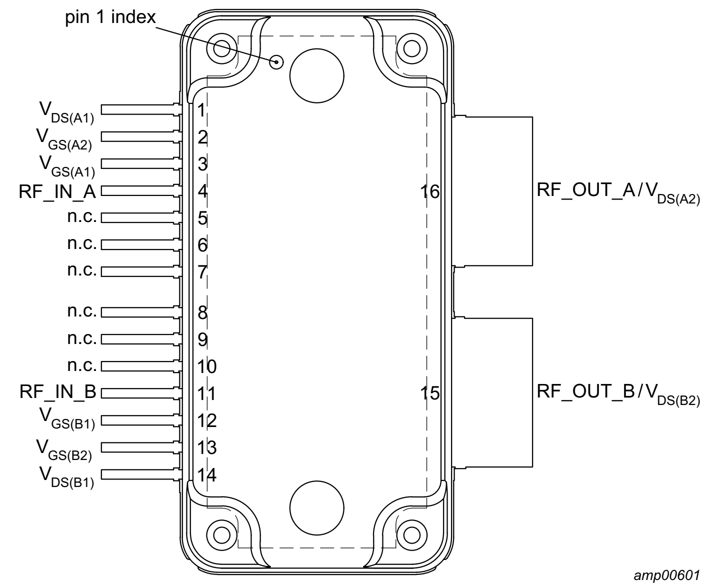
- Designed for broadband operation (frequency 1805 MHz to 2170 MHz)
- High section-to-section isolation enabling multiple combinations
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power MMIC for multi-carrier and multi-standard GSM, W-CDMA and LTE base stations in the 1805 MHz to 2170 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
  - Dual section or single ended
  - Doherty
  - Quadrature combined
  - Push-pull

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of driver stage A1
$V_{GS(A2)}$	2	gate-source voltage of final stage A2
$V_{GS(A1)}$	3	gate-source voltage of driver stage A1
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
$V_{GS(B1)}$	12	gate-source voltage of driver stage B1
$V_{GS(B2)}$	13	gate-source voltage of final stage B2
$V_{DS(B1)}$	14	drain-source voltage of driver stage B1

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_B/$V_{DS(B2)}$	15	RF output section B / drain-source voltage of final stage B2
RF_OUT_A/$V_{DS(A2)}$	16	RF output section A / drain-source voltage of final stage A2
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G1822S-20PB	-	plastic, heatsink small outline package; 16 leads (flat)	SOT1211-3
BLM7G1822S-20PBG	-	plastic, heatsink small outline package; 16 leads	SOT1212-3

4. Block diagram

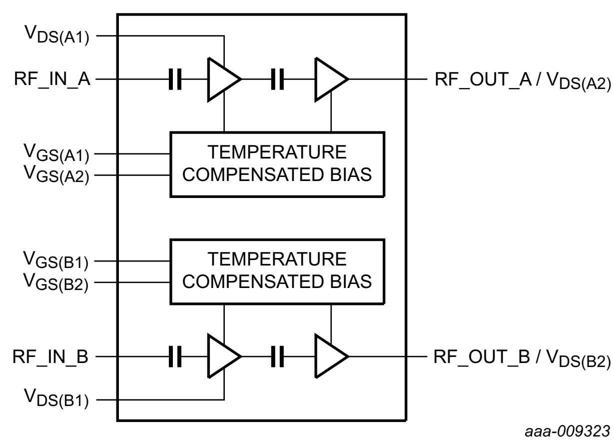


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; T_{case} = 90 °C; P_L = 3.56 W	[1]	1.9	K/W
		driver stage; T_{case} = 90 °C; P_L = 3.56 W	[1]	6.2	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Final stage							
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 150.8 μA		65	-	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 76 mA		1.5	2	2.5	V
		V_{DS} = 28 V; I_D = 76 mA	[1]	1.7	2.65	3.6	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	−40 °C ≤ T_{case} ≤ +85 °C	[1]	-	±1	-	%
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = 5.55 V; V_{DS} = 10 V		-	2.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V		-	-	140	nA
Driver stage							
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 30.16 μA		65	-	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 27 mA		1.6	2.1	2.6	V
		V_{DS} = 28 V; I_D = 27 mA	[2]	1.9	2.85	3.8	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	−40 °C ≤ T_{case} ≤ +85 °C	[2]	-	±1	-	%
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = 5.55 V; V_{DS} = 10 V		-	0.55	-	A
I_{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V		-	-	140	nA

[1] In production circuit with 1105 Ω gate feed resistor.

[2] In production circuit with 765 Ω gate feed resistor.

Table 7. RF Characteristics

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 27 mA; I_{Dq2} = 76 mA; $P_{L(AV)}$ = 2 W. Per section unless otherwise specified, measured in an Ampleon wideband f = 1807.5 MHz to 2167.5 MHz straight lead production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: single carrier W-CDMA [1]						
G_p	power gain	f = 1807.5 MHz	-	34	-	dB
		f = 2167.5 MHz	30.8	32.3	33.8	dB
η_D	drain efficiency	f = 1807.5 MHz	-	22	-	%
		f = 2167.5 MHz	20	23	-	%
RL_{in}	input return loss	f = 2167.5 MHz	-	–19	–10	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	f = 1807.5 MHz	-	–41	-	dBc
		f = 2167.5 MHz	-	–41	–37	dBc
PAR_O	output peak-to-average ratio	f = 1807.5 MHz	-	8.4	-	dB
		f = 2167.5 MHz	7.2	8.4	-	dB
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	T = –40 °C to +85 °C				
		final stage I_{Dq}; gate feed resistor = 1105 Ω	-	±1	-	%
		driver stage I_{Dq}; gate feed resistor = 765 Ω	-	±1	-	%
Test signal: CW [2]						
$\Delta\varphi_{s21}$	phase response difference	between sections	–10	-	+10	deg
$\Delta\|s_{21}\|^2$	insertion power gain difference	between sections	–0.5	-	+0.5	dB

[1] 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01% probability on CCDF.

[2] f = 2170 MHz.

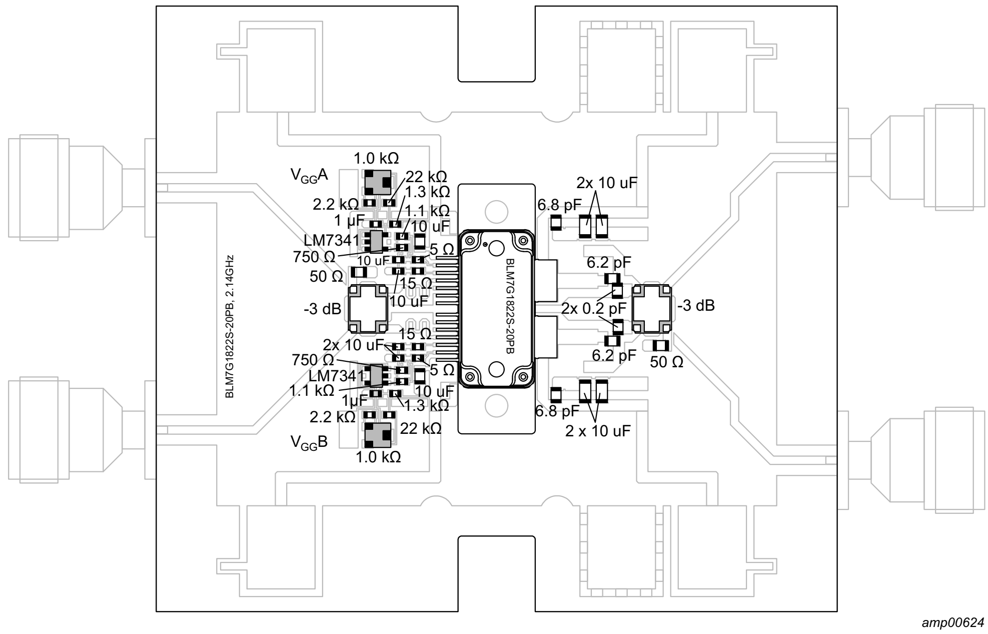
8. Application information

Table 8. Typical performance

Test signal: 1-tone CW; RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 45 mA (both sections); I_{Dq2} = 140 mA (both sections) unless otherwise specified, measured in an Ampleon f = 2110 MHz to 2170 MHz straight lead class AB application circuit (see Figure 3 for the component layout and Figure 4 for the electrical schematic).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	f = 2140 MHz	-	43.5	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 2140 MHz	-	44.1	-	dBm
η_D	drain efficiency	at $P_{L(1dB)}$; f = 2140 MHz	-	47.6	-	%
G_p	power gain	$P_{L(AV)}$ = 1.585 W; f = 2140 MHz	-	31.5	-	dB
B_{video}	video bandwidth	2-tone CW; $P_{L(AV)}$ = 1.585 W; f = 2140 MHz	-	170	-	MHz
G_{flat}	gain flatness	over a frequency range of 60 MHz; $P_{L(AV)}$ = 1.585 W	-	0.4	-	dB
$\Delta G/\Delta T$	gain variation with temperature	f = 2140 MHz	-	0.03	-	dB/°C
$\|s_{12}\|^2$	isolation	between sections A and B; $P_{L(AV)}$ = 1.585 W; f = 2140 MHz [1]	-	28.5	-	dB
K	Rollett stability factor	T = –40 °C; f = 0.1 GHz to 3 GHz	-	>1	-	

[1] Measured on dual section evaluation board I_{Dq1} = 40 mA (both sections); I_{Dq2} = 150 mA (both sections).



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

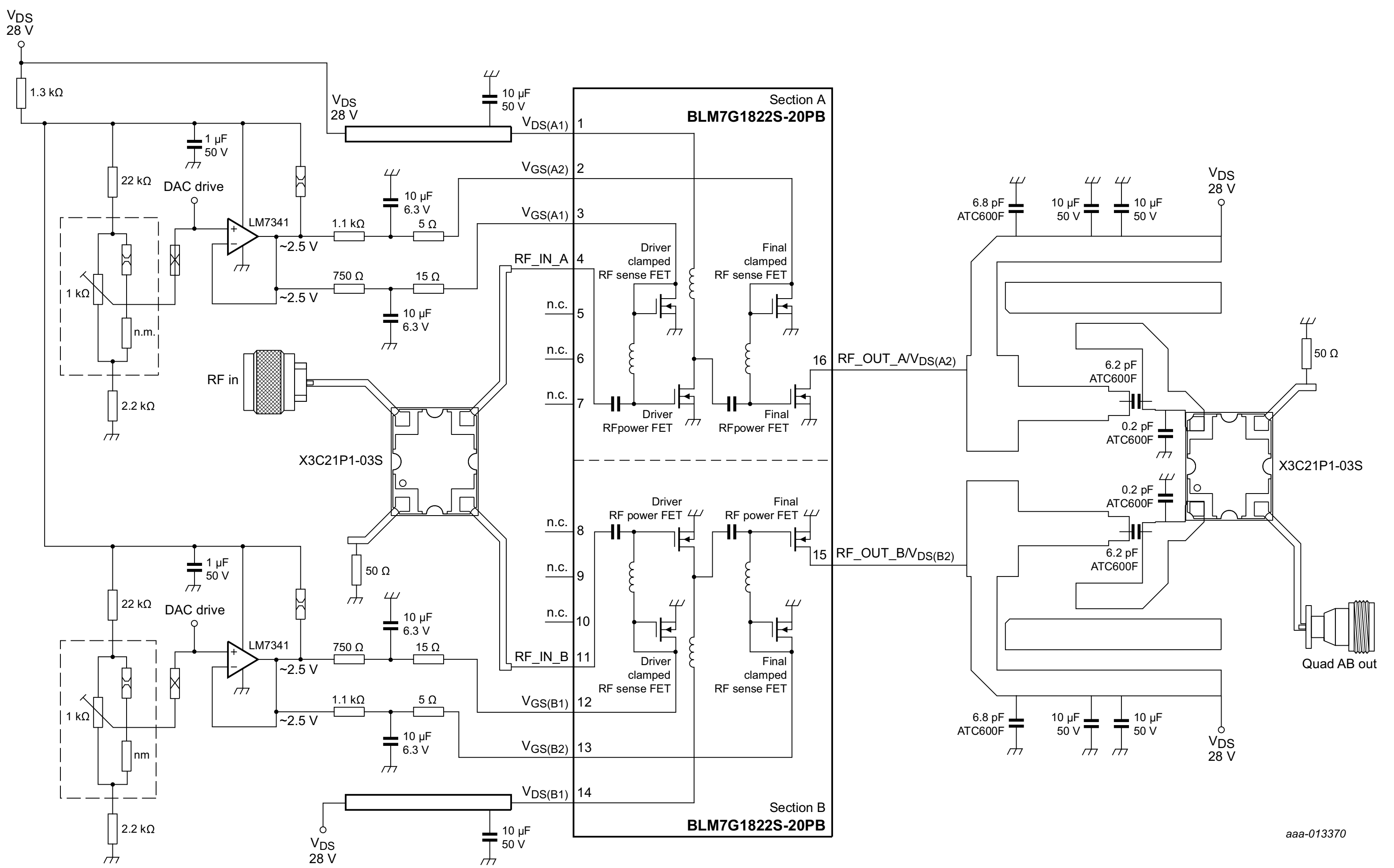


Fig 4. Electrical schematic

8.1 Possible circuit topologies

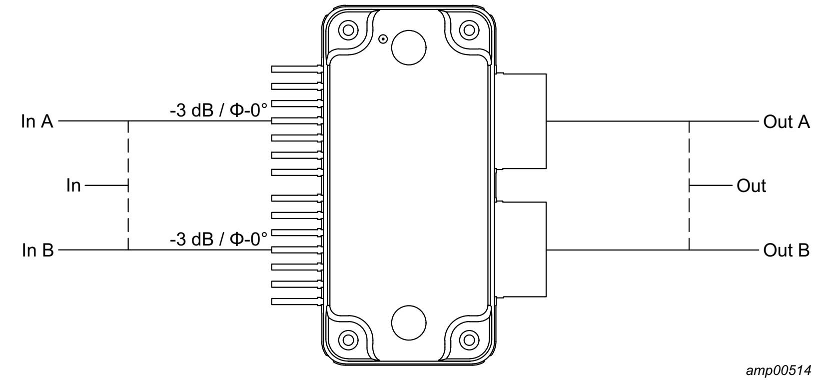


Fig 5. Dual section or single ended

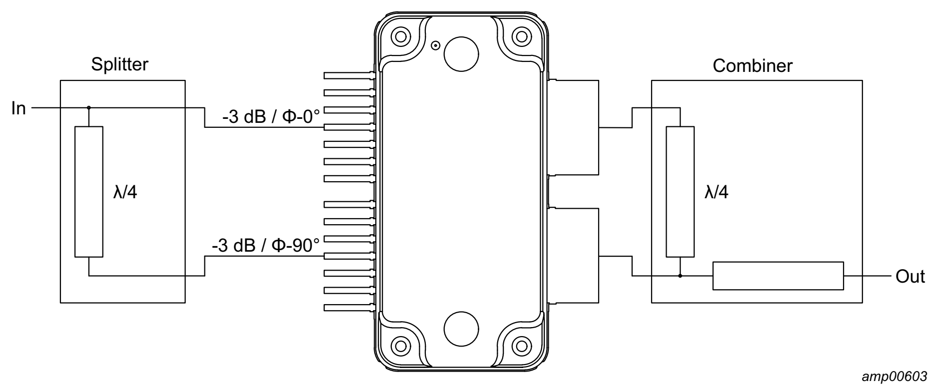


Fig 6. Doherty

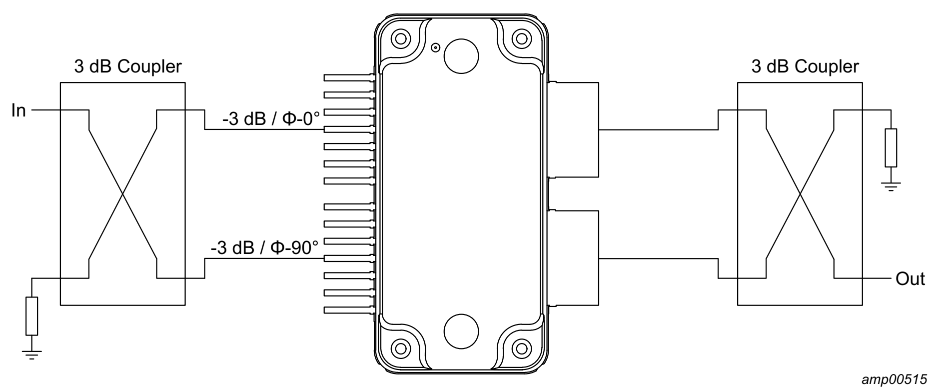


Fig 7. Quadrature combined

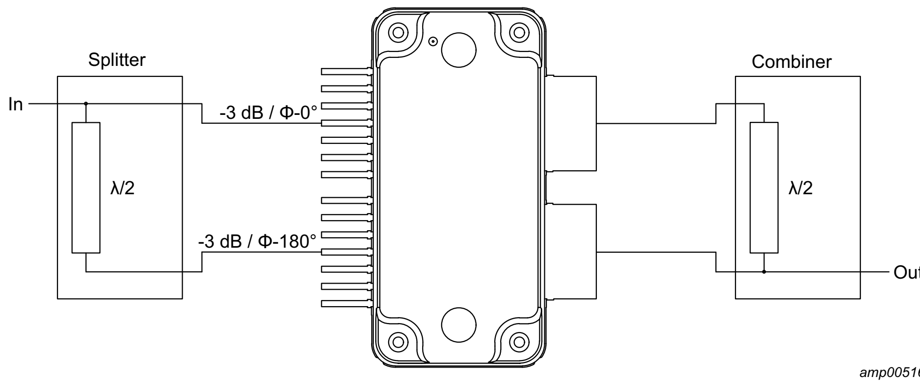


Fig 8. Push-pull

8.2 Ruggedness in class-AB operation

The BLM7G1822S-20PB and BLM7G1822S-20PBG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq1} = 20 mA (per section); I_{Dq2} = 75 mA (per section); P_i = 16 dBm (CW and corresponding to $P_{L(3dB)}$ under Z_S = 50 Ω load); f = 2140 MHz.

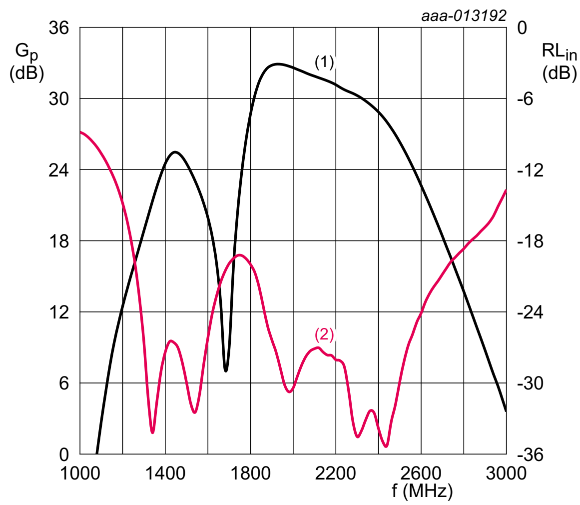
8.3 Impedance information

Table 9. Typical impedance at 3 dB compression point

Measured load-pull data per section; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 20 mA; I_{Dq2} = 65 mA; t_p = 100 μs; δ = 10 %; Z_S = 50 Ω. Typical values unless otherwise specified.

f	tuned for maximum output power					tuned for maximum efficiency				
	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(dBm)	(%)	(deg)	(Ω)	(dB)	(dBm)	(%)	(deg)
BLM7G1822S-20PB										
1700	15.3 – j14.5	33.2	42.7	50.6	8.3	28.5 – j20.2	34.6	41.6	56.5	9.2
1800	16.3 – j11.7	32.9	42.7	50.8	6.3	31.3 – j8.60	34.1	41.6	57.1	7.0
1900	16.1 – j9.70	32.1	42.8	50.8	6.1	26.5 – j0.01	33.3	41.7	57.3	6.9
2000	15.5 – j8.10	31.5	42.8	50.1	6.1	21.0 + j2.20	32.6	42.0	56.4	7.3
2100	14.4 – j6.90	31.5	42.9	50.0	6.9	15.6 + j2.00	32.9	42.1	55.8	8.6
2200	13.7 – j6.60	31.7	42.7	49.8	8.5	12.3 + j1.20	33.0	41.6	54.3	9.6
2300	12.8 – j6.80	31.4	42.5	49.1	10.6	10.0 + j0.10	32.5	41.3	53.6	10.3
BLM7G1822S-20PBG										
1700	15.8 – j16.1	33.5	42.5	52.9	9.2	28.9 – j21.8	35.1	41.6	57.9	11.1
1800	16.5 – j13.8	32.9	42.5	51.2	7.7	30.6 – j11.6	34.2	41.6	56.8	8.4
1900	16.7 – j12.4	32.2	42.5	50.2	7.2	27.9 – j4.64	33.5	41.7	55.9	7.8
2000	16.3 – j9.74	31.7	42.5	51.2	7.3	20.4 + j0.45	32.7	41.7	55.6	9.0
2100	15.6 – j8.61	31.5	42.6	52.0	9.5	15.9 + j0.68	32.6	41.7	56.5	11.8
2200	14.6 – j8.87	31.3	42.5	49.7	10.3	12.7 – j0.44	32.4	41.6	53.8	12.1
2300	13.4 – j9.32	30.5	42.4	48.2	12.8	10.7 – j1.98	31.7	41.6	53.7	13.2

8.4 Graphs

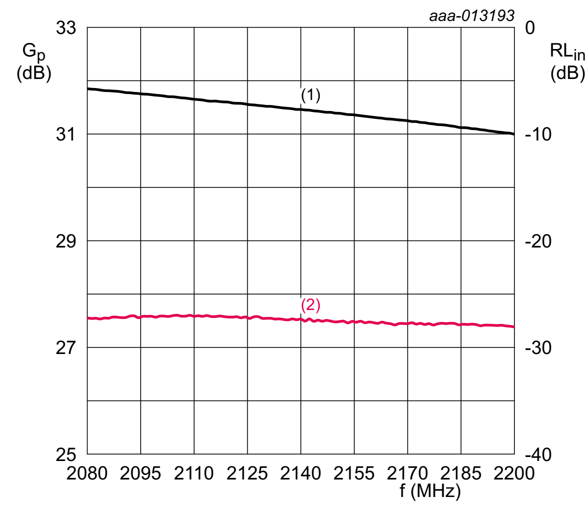


T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA; P_L = 1.585 W. Per section.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 9. Wideband power gain and input return loss as function of frequency; typical values

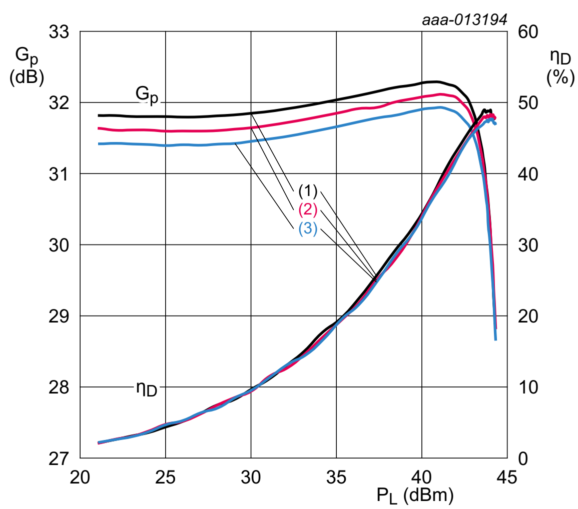


T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA; P_L = 1.585 W. Per section.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 10. In-band power gain and input return loss as function of frequency; typical values



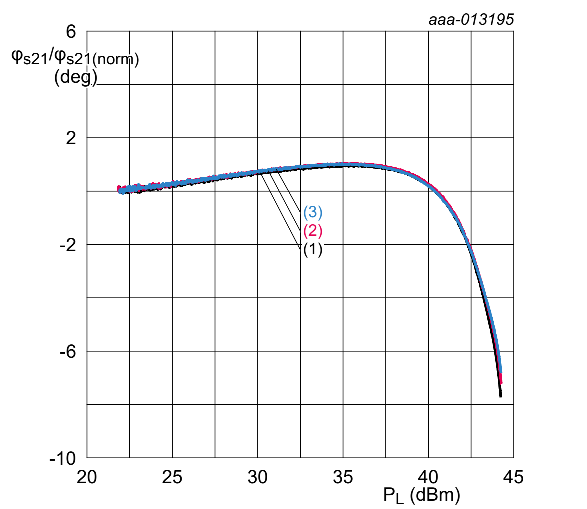
T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA. Per section.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 11. Power gain and drain efficiency as function of output power; typical values



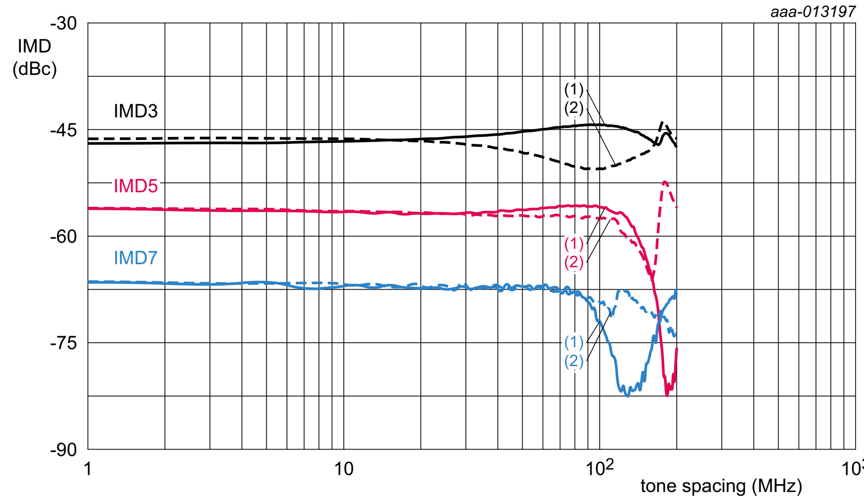
Normalized at P_L = 22 dBm; T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA. Per section.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 12. Normalized phase response as a function of output power; typical values

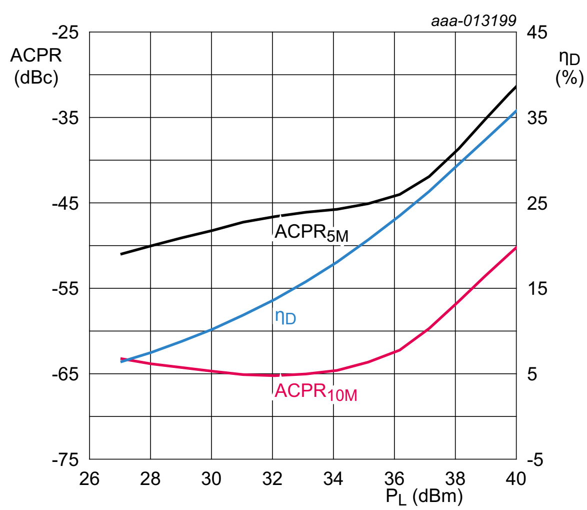


T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA; f = 2140 MHz; 2-tone CW; $P_{L(AV)}$ = 0.25 W. Per section.

(1) IMD low

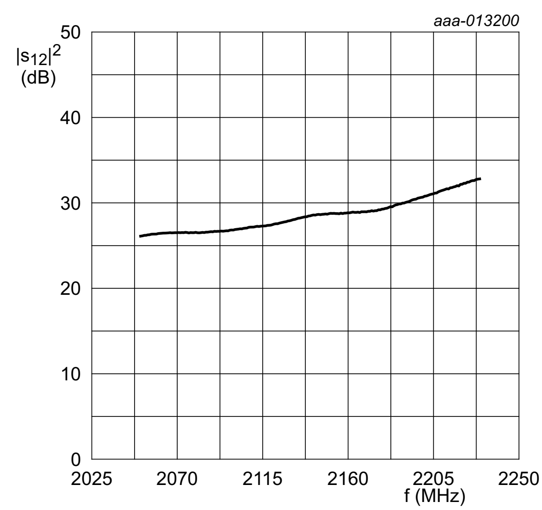
(2) IMD high

Fig 13. Intermodulation distortion as a function of tone spacing; typical values



T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 22 mA; I_{Dq2} = 70 mA; f = 2140 MHz; 1-carrier W-CDMA; test model 1; PAR = 7.2 dB at 0.01 % probability on CCDF. Per section.

Fig 14. Adjacent channel power ratio and drain efficiency as function of output power; typical values

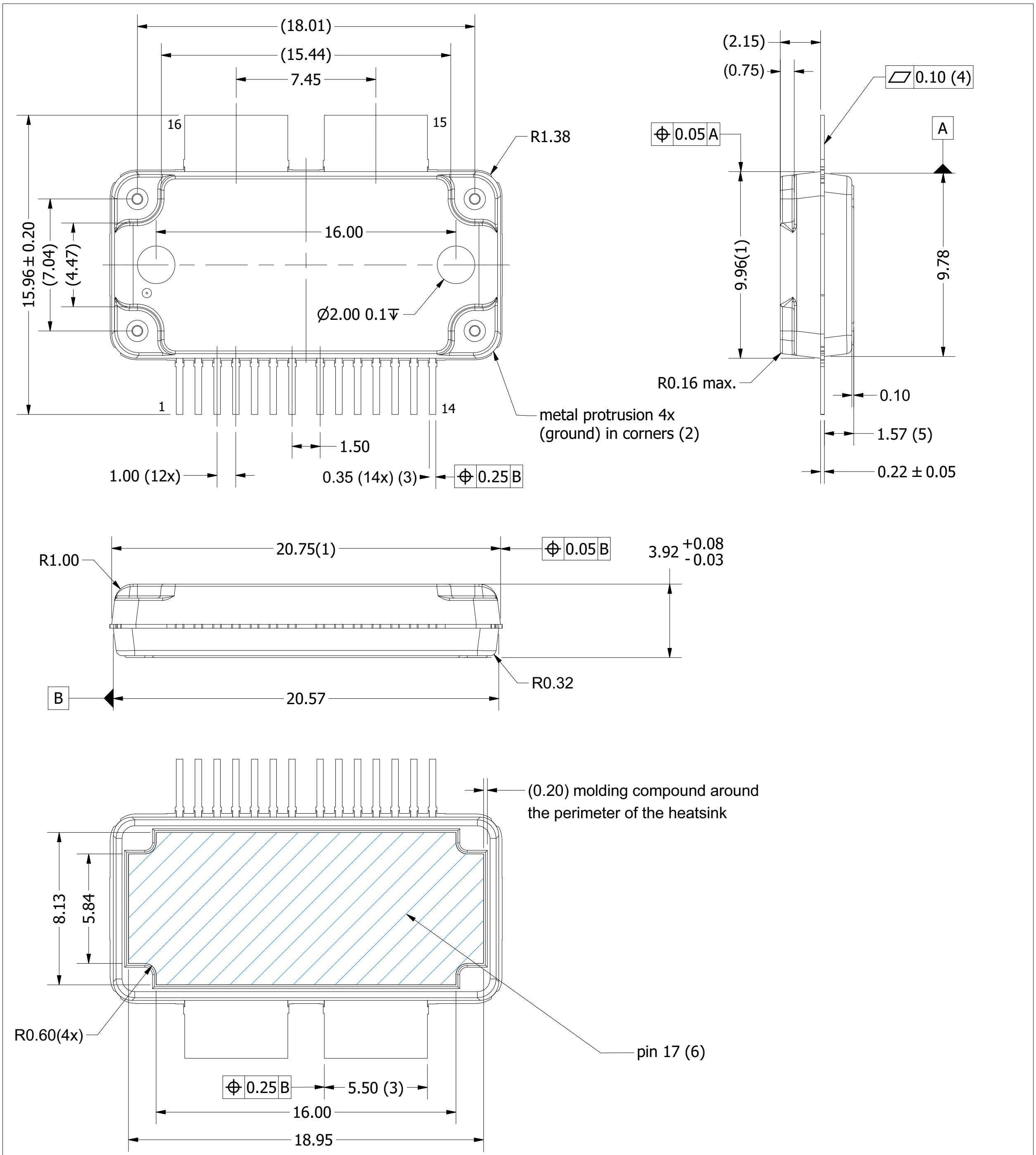


T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 20 mA; I_{Dq2} = 75 mA. Per section. Measured on evaluation board.

Fig 15. Isolation as a function of frequency; typical values

9. Package outline

SOT1211-3

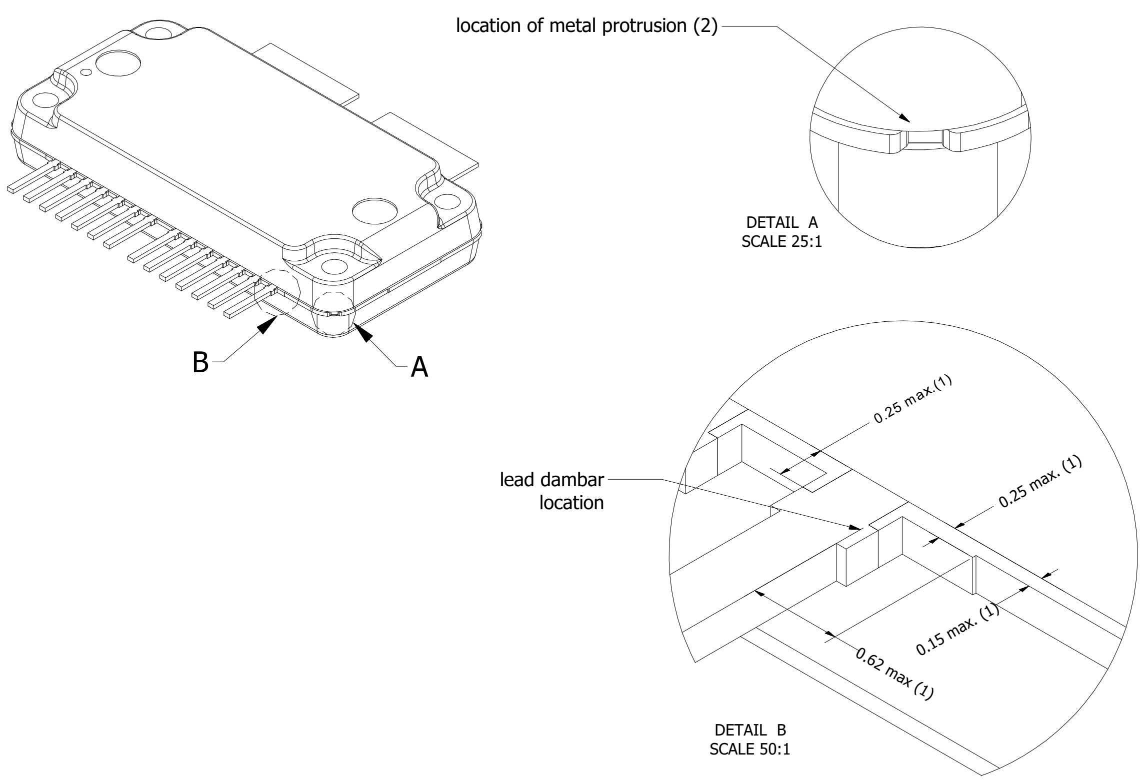


Package outline drawing:	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 9/4/2017
SOT1211-3		Third angle projection	Sheet 1 of 2

Fig 16. Package outline SOT1211-3 (sheet 1 of 2)

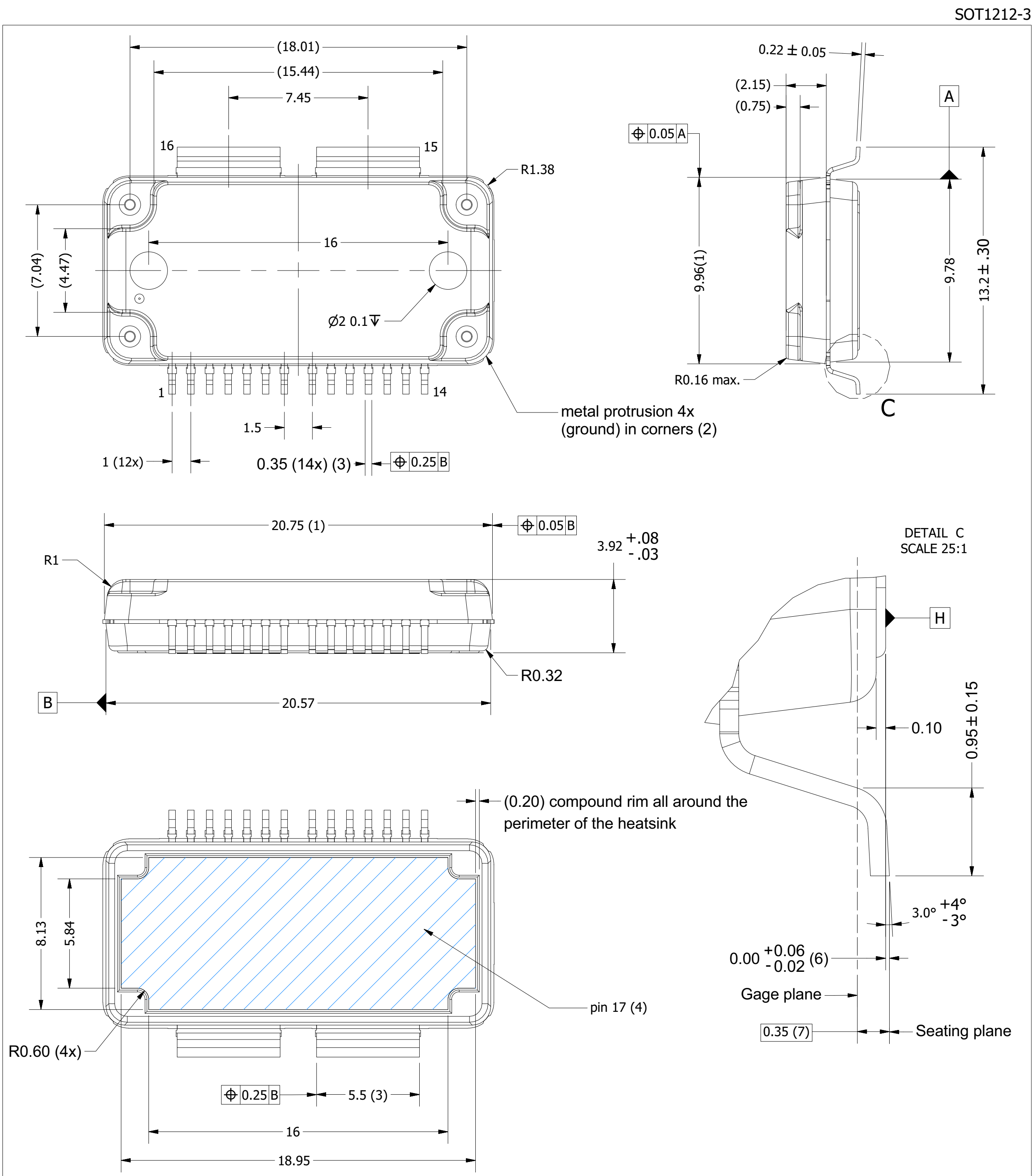
SOT1211-3

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm. max. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The lead coplanarity over all leads is 0.1 mm maximum.
(5)	Dimension is measured 0.5 mm from the edge of the top package body.
(6)	The hatched area indicates the exposed metal heatsink.
(7)	The leads and exposed heatsink are plated with matte Tin (Sn).



Package outline drawing: SOT1211-3	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 9/4/2017
		Third angle projection	Sheet 2 of 2

Fig 17. Package outline SOT1211-3 (sheet 2 of 2)

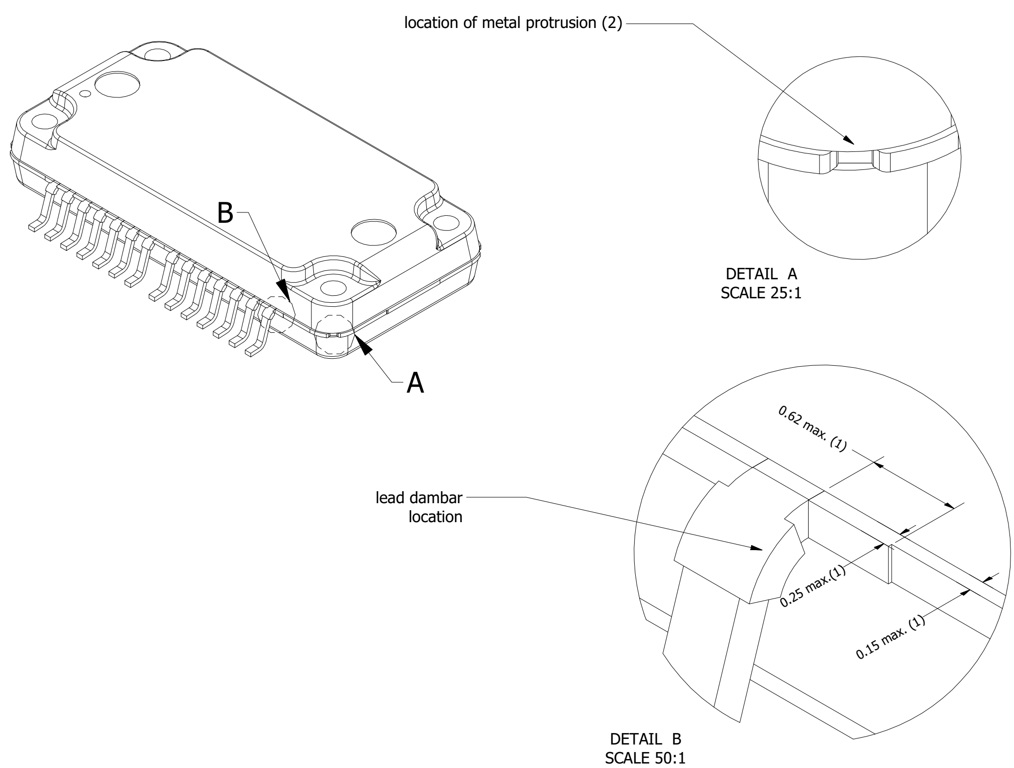


Package outline drawing: SOT1212-3	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 9/4/2017
		Third angle projection	Sheet 1 of 2

Fig 18. Package outline SOT1212-3 (sheet 1 of 2)

SOT1212-3

Drawing Notes	
Items	Description
(1)	Dimensions are excluding mold protrusion. Areas located adjacent to the leads have a maximum mold protrusion of 0.25 mm (per side) and 0.62 mm max. in length. In between the 14 leads the protrusion is 0.25 mm max. At all other areas the mold protrusion is maximum 0.15 mm per side. See also detail B.
(2)	The metal protrusion (tie bars) in the corner will not stick out of the molding compound protrusions (detail A).
(3)	The lead dambar (metal) protrusions are not included. Add 0.14 mm max to the total lead dimension at the dambar location.
(4)	The hatched area indicated the exposed heatsink.
(5)	The leads and exposed heatsink are plated with matte Tin (Sn).
(6)	Dimension is measured with respect to the bottom of the heatsink Datum H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.
(7)	Gage plane (foot length) to be measured from the seating plane.



Package outline drawing: SOT1212-3	units in mm.	Tolerances unless otherwise stated: Dimension: ± 0.05 Angle: ± 1°	Revision: 0 Revision date: 9/4/2017
		Third angle projection	Sheet 2 of 2

Fig 19. Package outline SOT1212-3 (sheet 2 of 2)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1A [2]

[1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.

[2] HBM classification 1A is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
AM	Amplitude Modulation
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN7	Seventh Generation
GSM	Global System for Mobile Communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LTE	Long Term Evolution
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
PM	Phase Modulation
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G1822S-20PB_S-20PBG v.5	20180227	Product data sheet		BLM7G1822S-20PB_S-20PBG v.4
Modifications:	• Figure 1 on page 2: figure updated • Table 3 on page 3: package outline versions changed to SOT1211-3 and SOT1212-3 • Table 8 on page 5: typo corrected • Figure 3 on page 6: figure updated • Figure 5 on page 8: figure updated • Figure 6 on page 8: figure updated • Figure 7 on page 8: figure updated • Figure 8 on page 9: figure updated • Table 9 on page 9: typo corrected • Section 9 on page 12: package outline versions changed from SOT1211-2 and SOT1212-2 to SOT1211-3 and SOT1212-3 • Table 10 on page 16: added table			
BLM7G1822S-20PB_S-20PBG v.4	20150901	Product data sheet		BLM7G1822S-20PB_S-20PBG v.3
BLM7G1822S-20PB_S-20PBG v.3	20150701	Product data sheet	-	BLM7G1822S-20PB_S-20PBG v.2
BLM7G1822S-20PB_S-20PBG v.2	20140626	Objective data sheet	-	BLM7G1822S-20PB_S-20PBG v.1
BLM7G1822S-20PB_S-20PBG v.1	20131219	Objective data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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15. Contents

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