30 MHz to 4.5 GHz, 45 dB RF Detector

Data Sheet

ADL5506

FEATURES

- Complete RF detector function
- Typical dynamic range: 45 dB
- Frequency range from 30 MHz to 4.5 GHz
- Excellent temperature stability
- Stable linear in decibel response
- Power on/off response time: 65 ns/145 ns (rise/fall)
  - −5 dBm input power applied
- Operates from −40°C to +85°C
- Low power: 3.8 mA at 3.0 V
  - Power supply voltage range from 2.5 V to 5.5 V
- Disable current <1 µA

APPLICATIONS

- RSSI and TSSI for wireless terminal devices
- RF transmitter or receiver power measurement

GENERAL DESCRIPTION

The ADL5506 is a complete, low cost subsystem for the measurement of RF signals in the 30 MHz to 4.5 GHz frequency range, with a typical dynamic range of 45 dB, intended for use in a wide variety of wireless terminal devices. It provides a wider dynamic range and better accuracy than is possible using discrete diode detectors. In particular, its temperature stability is excellent over −40°C to +85°C.

Its high sensitivity allows measurement of low power levels, thus reducing the amount of power that needs to be coupled to the detector. It is essentially a voltage responding device, with a typical dynamic range of 45 dB.

For convenience, the signal is internally ac-coupled, using a 5 pF capacitor and a broadband 50 Ω match, with an external shunt resistor of 52 Ω. This high-pass coupling, with a corner at approximately 19 MHz, determines the lowest operating frequency. Therefore, the source can be dc grounded.

The ADL5506 output increases from approximately 0.14 V to a little over 1 V as the input signal level increases from 1.25 mV rms (−45 dBm) to 224 mV rms (0 dBm). The output is proportional to the logarithm of the input power level; that is, the reading is presented directly in decibels and is scaled about 18 mV/dB at 900 MHz. A capacitor can be connected between the VLOG pin and the CFLT pin when it is desirable to increase the time interval over which averaging of the input waveform occurs.

The ADL5506 is available in a 6-ball WLCSP and consumes 3.8 mA from a 3.0 V supply. When powered down, the typical disable supply current is <1 µA.

FUNCTIONAL BLOCK DIAGRAM

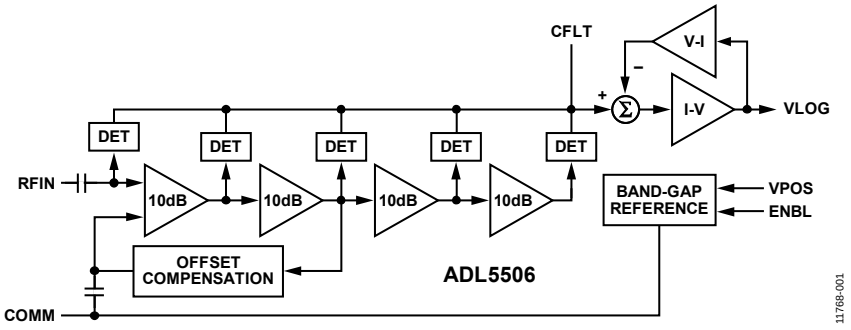

Figure 1.

Rev. A

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/2017—Rev. 0 to Rev. A

Changes to Land Pattern and Soldering Information Section ... 22

11/2013—Revision 0: Initial Version

SPECIFICATIONS

VPOS = 3.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	Pin RFIN				
Frequency Range			30 to 4500		MHz
Input Voltage Range	Internally ac-coupled		1.25 to 400		mV rms
Equivalent Power Range	52.3 Ω external termination		−45 to +5		dBm
Input Resistance[1]	f = 0.1 GHz, 52.3 Ω shunt resistor at RFIN		50		Ω
OUTPUT INTERFACE	Pin VLOG				
Output Offset Voltage	No signal at RFIN, $R_L \geq 10$ kΩ		0.14		V
Maximum Output Voltage	Transient during enable sequencing		2.25		V
Available Output Current	Sourcing/sinking		4/1		mA
Rise Time	P_{IN} = off to −5 dBm, 10% to 90%		65		ns
Fall Time	P_{IN} = −5 dBm to off, 90% to 10%		145		ns
Residual RF (at Twice the Input Frequency)	f = 0.1 GHz		50		µV
Output Noise	RF input = 1900 MHz, −10 dBm, f_{NOISE} = 100 kHz, C_{FLT} = open		175		nV/√Hz
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power	High condition, −40°C ≤ T_A ≤ +85°C	1.2		V_{POS}	V
Input Current When High	2.7 V at ENBL, −40°C ≤ T_A ≤ +85°C		<1		µA
Logic Level to Disable Power	Low condition, −40°C ≤ T_A ≤ +85°C	0		0.5	V
POWER INTERFACE	Pin VPOS				
Supply Voltage		2.5	3.0	5.5	V
Quiescent Current			3.8		mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		4.6		mA
vs. Supply	2.5 V ≤ V_{POS} ≤ 5.5 V		3.9		mA
Disable Current	−40°C ≤ T_A ≤ +85°C, enable voltage = 0 V		<1		µA
30 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		42		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −25 dBm, and −5 dBm		5		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −25 dBm, and −5 dBm		−37		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.9/−0.6[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −5 dBm		+0.8/−0.9[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −5 dBm		18.8		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −5 dBm		−45.5		dBm
Output Voltage—High Power Input	P_{IN} = −5 dBm		762		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		293		mV
50 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		45		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −25 dBm, and −5 dBm		4		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −25 dBm, and −5 dBm		−41		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.5/−0.7[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −5 dBm		+0.9/−0.95[2]		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Logarithmic Slope	Calibration at −30 dBm and −5 dBm		17.8		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −5 dBm		−51.5		dBm
Output Voltage—High Power Input	P_{IN} = −5 dBm		821		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		380		mV
100 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		46		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		2		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.15/−0.5[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.7/−0.9[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		17.7		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−53.7		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		774		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		420		mV
450 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		45		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −8 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −8 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.3/−0.5[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.6/−0.9[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		18.4		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−53.2		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		797		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		428		mV
900 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		45		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.3/−0.5[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.6/−0.8[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		18.2		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−54		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		798		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		435		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
1900 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		46		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		2		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.1/−0.4[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.2/−0.7[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		17.5		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−55.5		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		797		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		446		mV
2140 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		45		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.1/−0.5[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.2/−0.7[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		17.5		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−56		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		800		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		450		mV
2700 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		46		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −40 dBm, −30 dBm, and −10 dBm		−45		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.2/−0.7[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.3/−0.9[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		17.5		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−57		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		808		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		461		mV
3500 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		45		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −42 dBm, −30 dBm, and −10 dBm		1		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −42 dBm, −30 dBm, and −10 dBm		−44		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	−40°C < T_A < +85°C; P_{IN} = −30 dBm		+0.1/−1.1[2]		dB
	−40°C < T_A < +85°C; P_{IN} = −10 dBm		+0.2/−1[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		17.2		mV/dB
Logarithmic Intercept	Calibration at−30 dBm and −10 dBm		−55		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		773		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		430		mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
4500 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		42		dB
Maximum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −30 dBm, and −10 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Three-point calibration at −35 dBm, −30 dBm, and −10 dBm		−39		dBm
Deviation vs. Temperature	Deviation from output at 25°C, 3 V				
	T_A = −40°C; P_{IN} = −30 dBm		−3.2		dB
	0°C < T_A < 85°C; P_{IN} = −30 dBm		+0.5/−0.8[2]		dB
	T_A = −40°C; P_{IN} = −10 dBm		−3.1		dB
	0°C < T_A < 85°C; P_{IN} = −10 dBm		+0.1/−0.7[2]		dB
Logarithmic Slope	Calibration at −30 dBm and −10 dBm		16.7		mV/dB
Logarithmic Intercept	Calibration at −30 dBm and −10 dBm		−50		dBm
Output Voltage—High Power Input	P_{IN} = −10 dBm		684		mV
Output Voltage—Low Power Input	P_{IN} = −30 dBm		350		mV

[1] See Figure 32.
[2] The slash indicates a range. For example, +0.9/−0.6 means +0.9 to −0.6.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
RF Input Power, RFIN[1, 2]	15 dBm
Equivalent Voltage, Sine Wave Input	1.25 V rms
Internal Power Dissipation	75 mW
θ_{JA} (WLCSP)	260°C/W
Maximum Junction Temperature	145°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

[1] Driven from a 50 Ω source.
[2] Under 50 Ω input matched condition.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

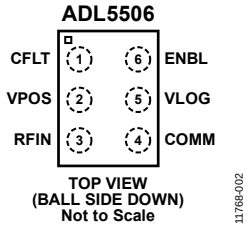

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CFLT	Connection for an External Capacitor, CFLT, to Reduce the Modulation Content from the Output Voltage. It also slows the response of the output and reduces the noise seen on the output. The capacitor is connected between CFLT and VLOG. See the Filter Capacitor section for choosing the correct CFLT value.
2	VPOS	Positive Supply. The positive supply voltage (V_{POS}) range is from 2.5 V to 5.5 V. Use decoupling capacitors near this pin on the printed circuit board.
3	RFIN	RF Input. 5 pF ac coupling capacitor on chip. Connect a 52.3 Ω shunt resistor near this pin for broadband 50 Ω match. See the Input Coupling Options section for more matching options.
4	COMM	Device Common (Ground). Connect this pin to system ground using a low impedance path.
5	VLOG	Logarithmic Output. The output voltage (V_{Log}) increases with increasing input amplitude. The output is proportional to the logarithm of the input signal level.
6	ENBL	Device Enable. Connect the ENBL pin to a logic high (1.2 V to V_{POS}) to enable the device. Connect the ENBL pin to a logic low (0 V to 0.5 V) to disable the device.

TYPICAL PERFORMANCE CHARACTERISTICS

VPOS = 3 V, T_A = +25°C (black), +85°C (red), 0°C (green), and −40°C (dark blue) where appropriate. C_{FLT} = open, unless otherwise noted. Input RF signal is a sine wave (CW), unless otherwise indicated. Error referred to slope and intercept at indicated calibration points at 25°C. Power referenced to 50 Ω source and with a 52.3 Ω shunt matching resistor on the board. Distribution plots based upon more than 50 devices.

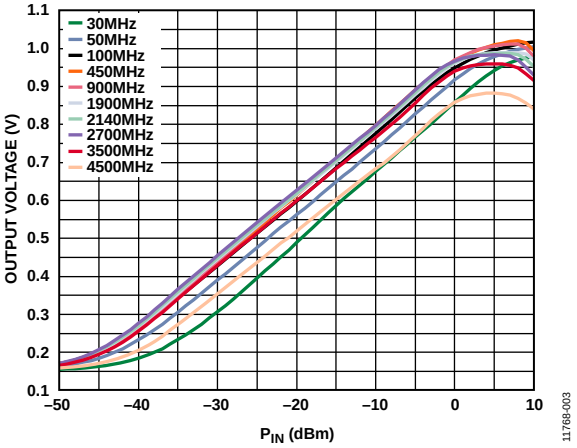

Figure 3. Typical V_{LOG} vs. P_{IN} over Frequency at 25°C

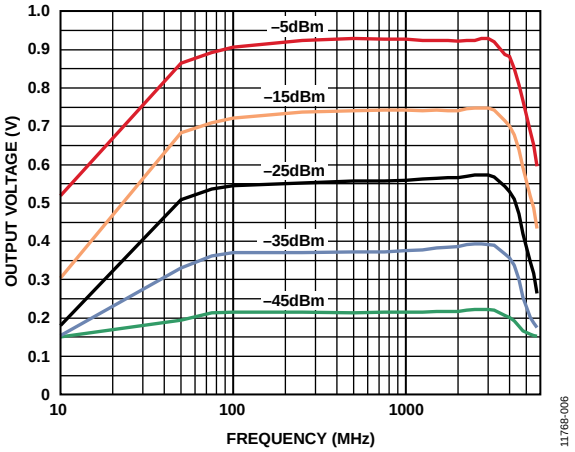

Figure 6. Typical V_{LOG} vs. Frequency for Five RF Input Levels at 25°C

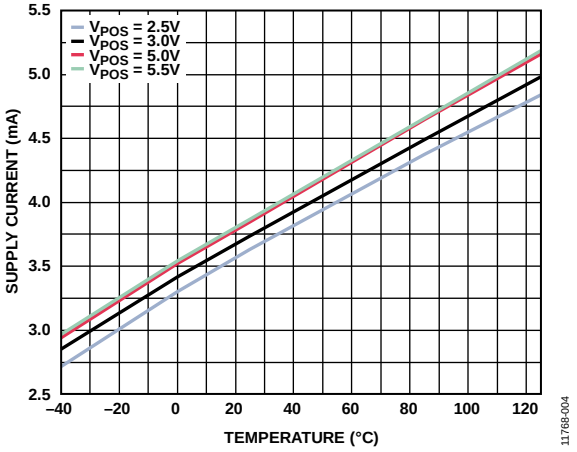

Figure 4. Quiescent Supply Current vs. Temperature, 2.5 V to 5.5 V Supply Voltage

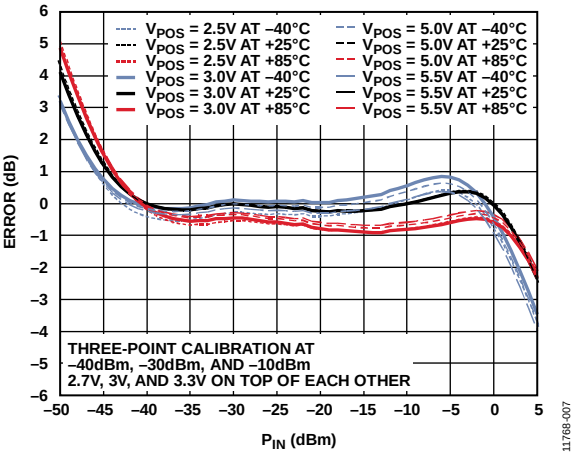

Figure 7. Log Conformance Error vs. P_{IN} over Supply Voltage and Temperature at 100 MHz

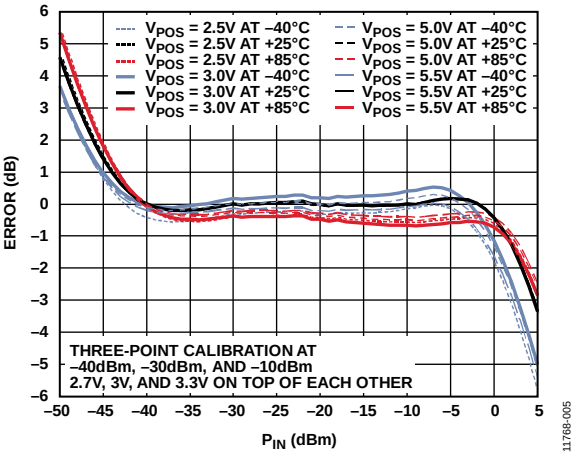

Figure 5. Log Conformance Error vs. P_{IN} over Supply Voltage and Temperature at 900 MHz

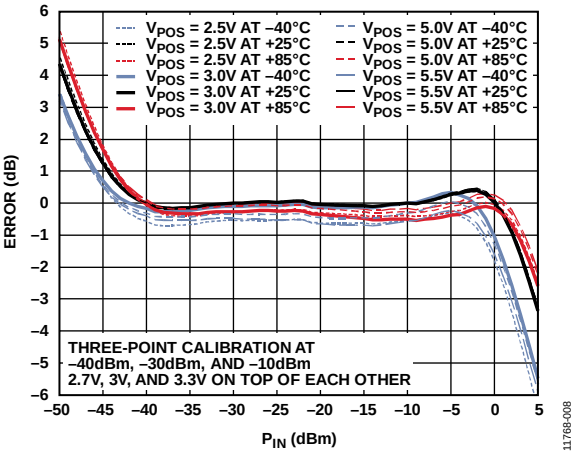

Figure 8. Log Conformance Error vs. P_{IN} over Supply Voltage and Temperature at 1900 MHz

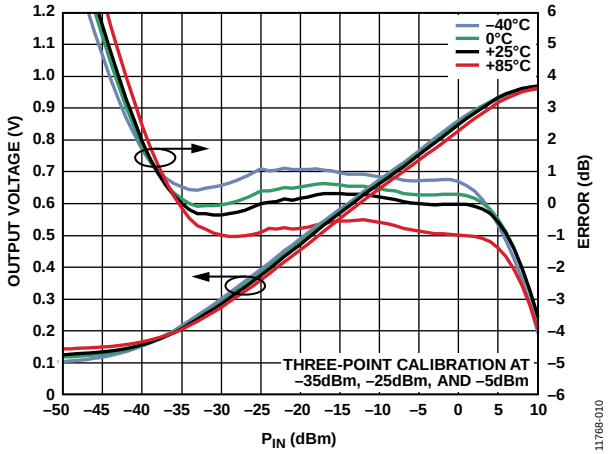

Figure 9. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 30 MHz

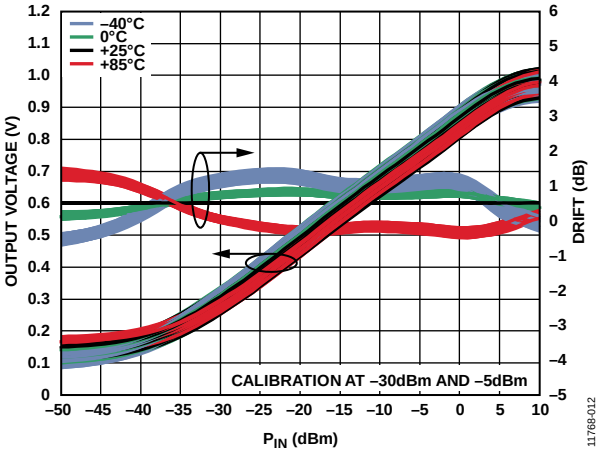

Figure 12. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 30 MHz

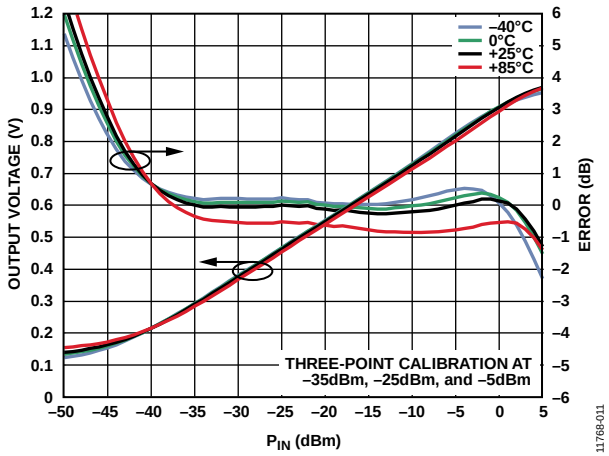

Figure 10. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 50 MHz

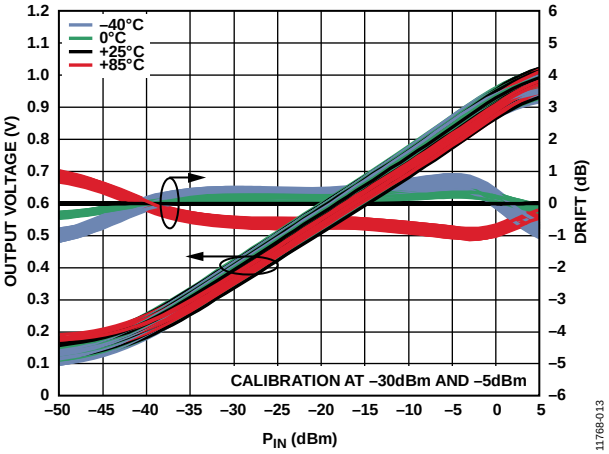

Figure 13. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 50 MHz

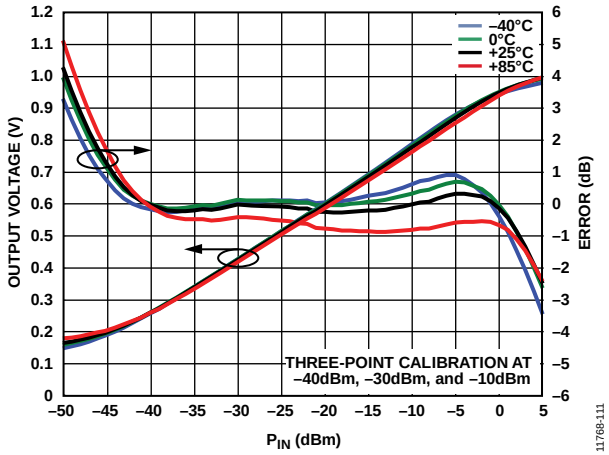

Figure 11. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 100 MHz

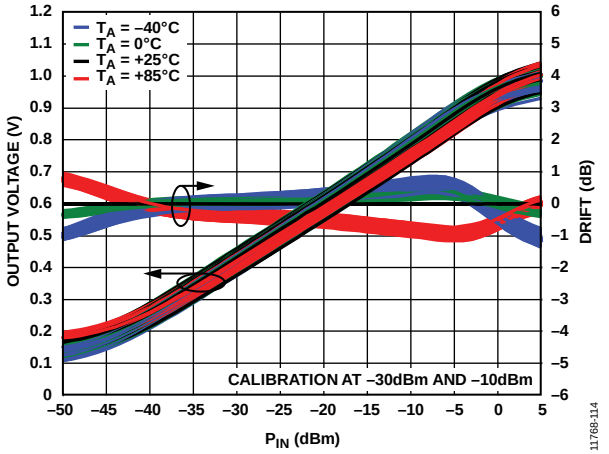

Figure 14. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 100 MHz

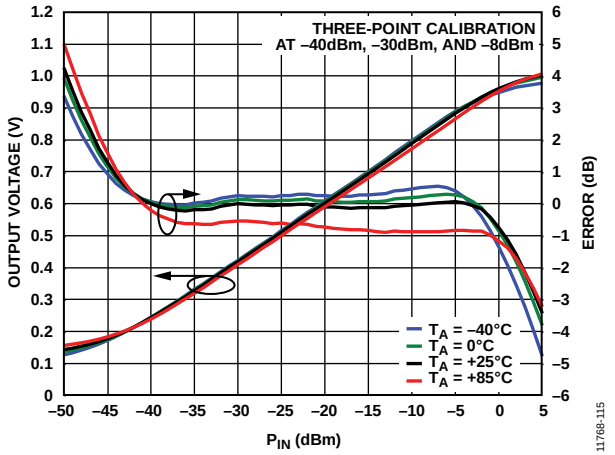

Figure 15. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 450 MHz

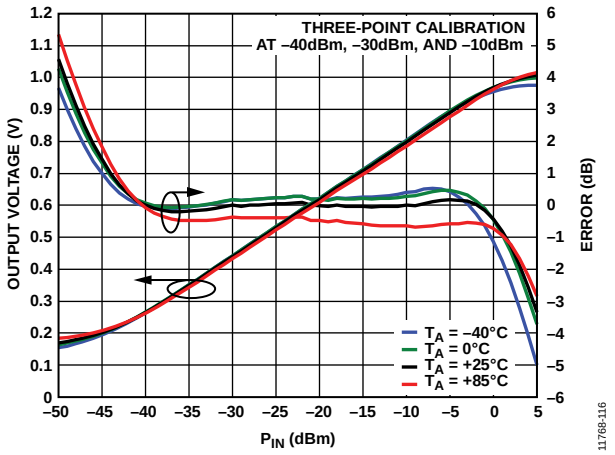

Figure 16. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 900 MHz

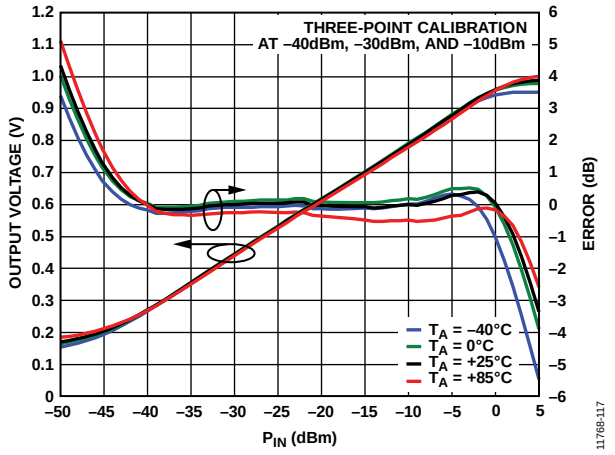

Figure 17. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 1900 MHz

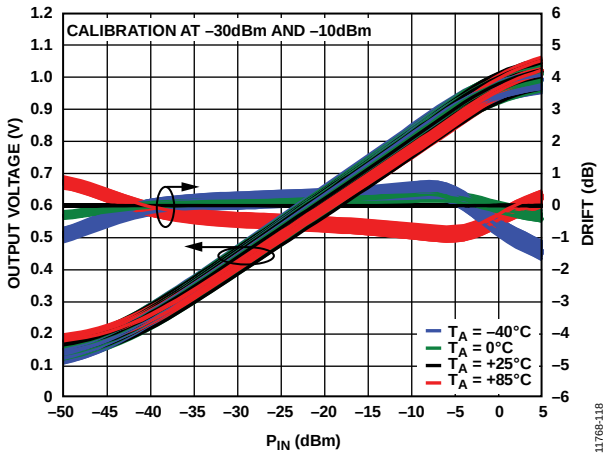

Figure 18. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 450 MHz

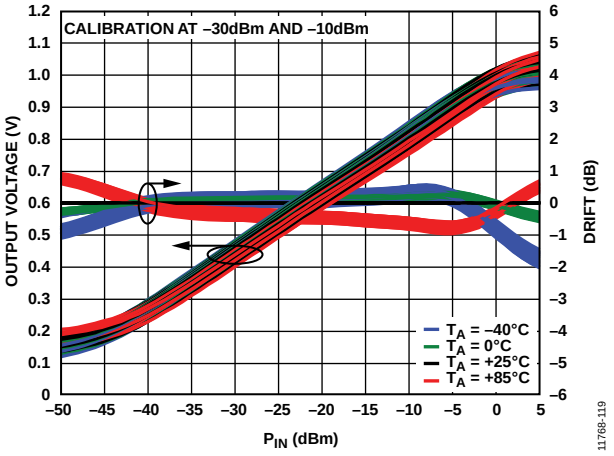

Figure 19. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 900 MHz

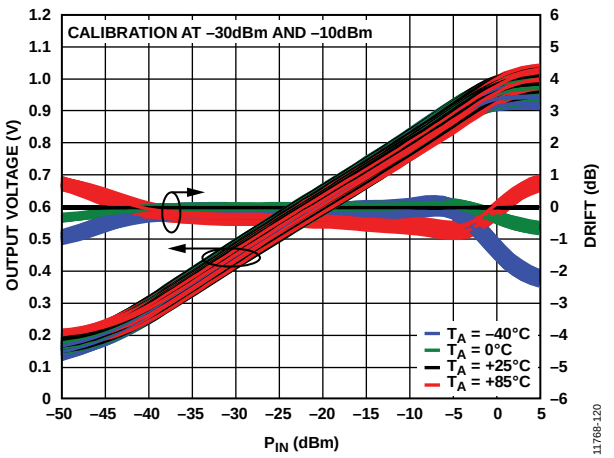

Figure 20. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 1900 MHz

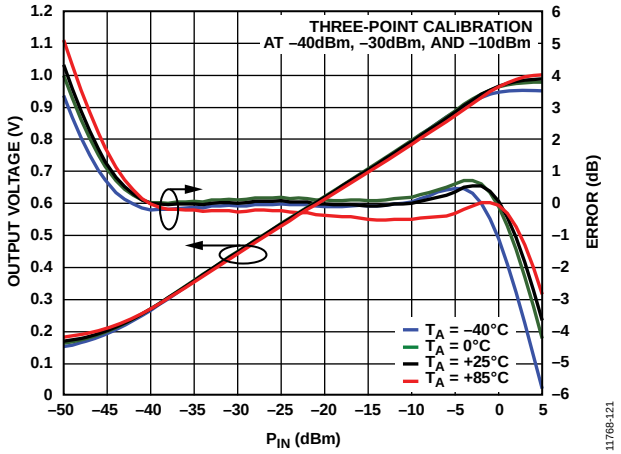

Figure 21. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 2140 MHz

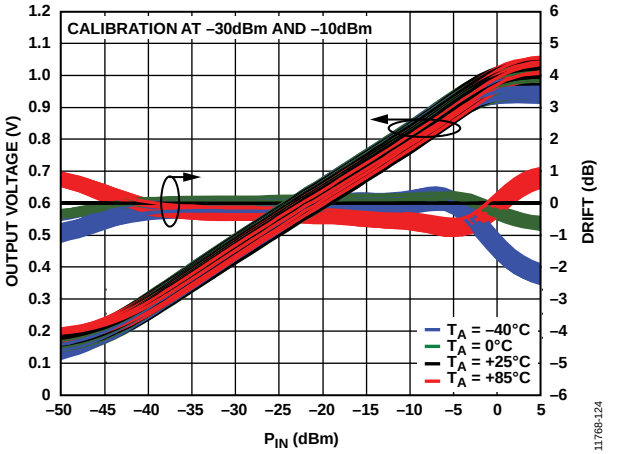

Figure 24. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 2140 MHz

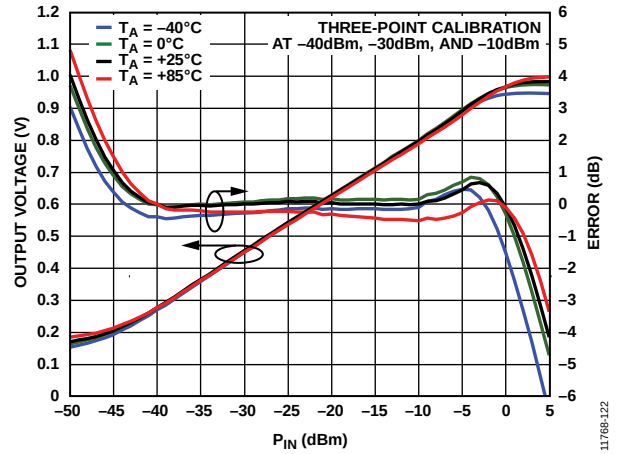

Figure 22. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 2700 MHz

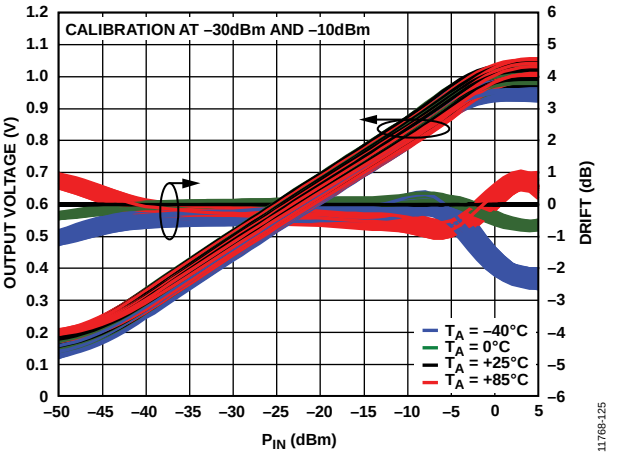

Figure 25. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 2700 MHz

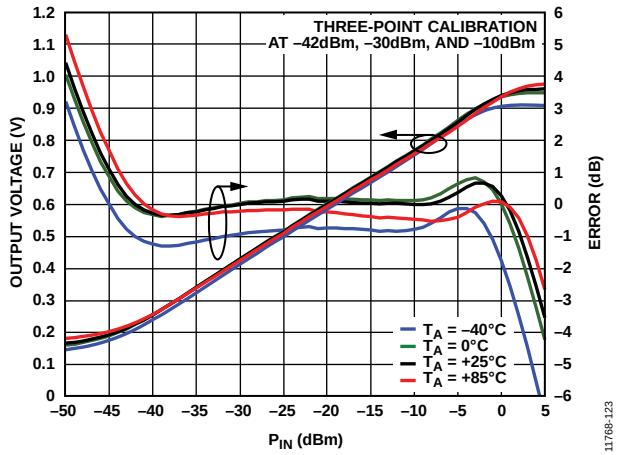

Figure 23. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 3500 MHz

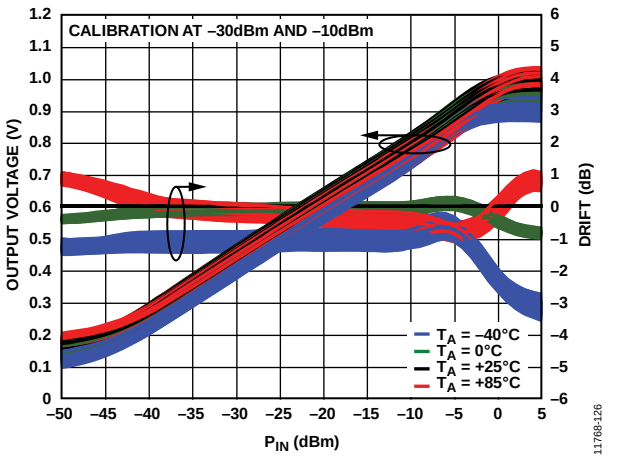

Figure 26. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 3500 MHz

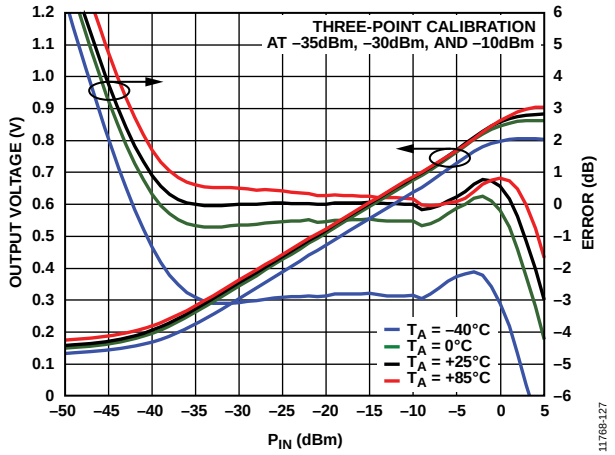

Figure 27. V_{LOG} and Log Conformance Error vs. P_{IN} over Temperature at 4500 MHz

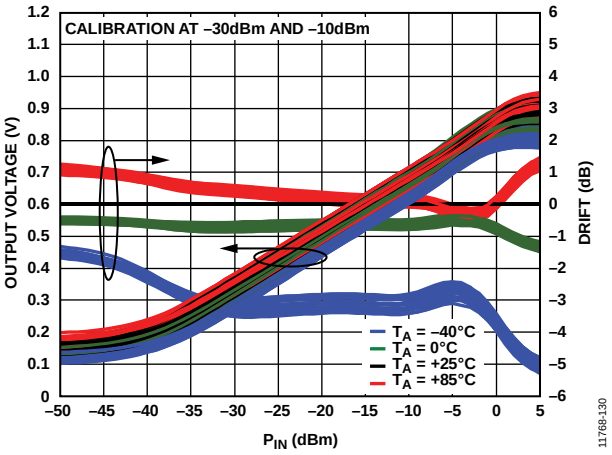

Figure 30. Distribution of Log Conformance Error with Respect to V_{LOG} at 25°C vs. P_{IN} and Temperature at 4500 MHz

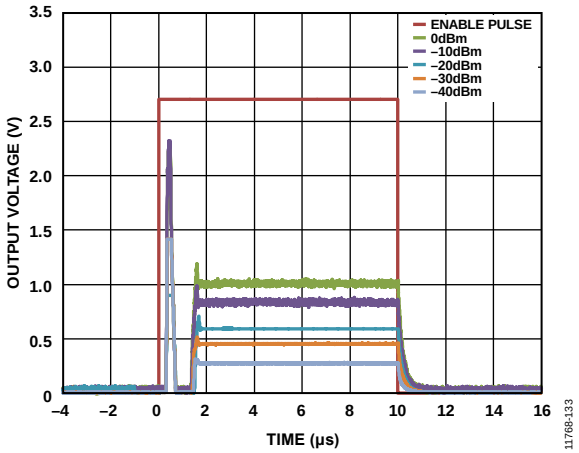

Figure 28. Output Response to Gating on ENBL Pin for Various RF Input Levels, Carrier Frequency = 900 MHz, C_{FLT} = Open (see Figure 39 in the Measurement Setups Section)

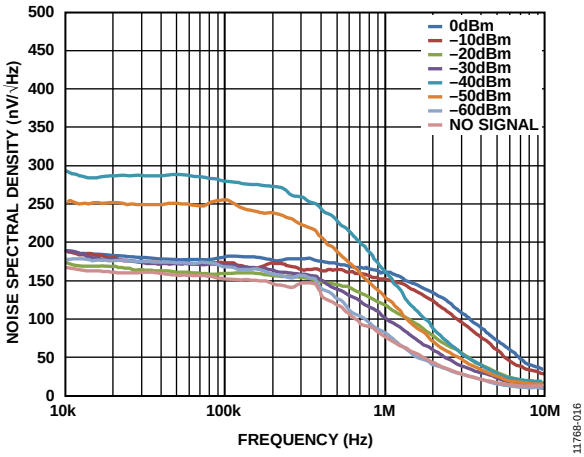

Figure 31. Noise Spectral Density, C_{FLT} = Open, 25°C

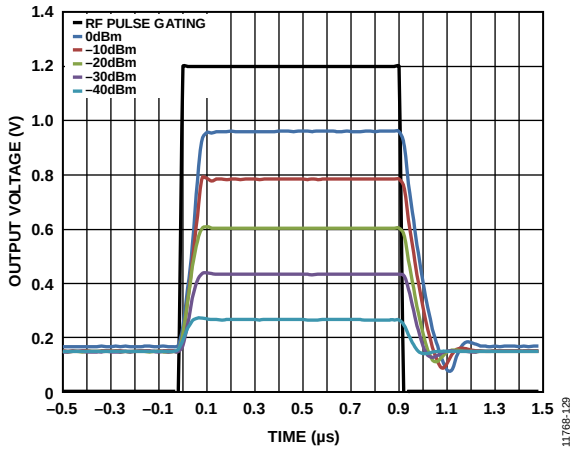

Figure 29. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency = 100 MHz, C_{FLT} = Open (See Figure 40 in the Measurement Setups Section)

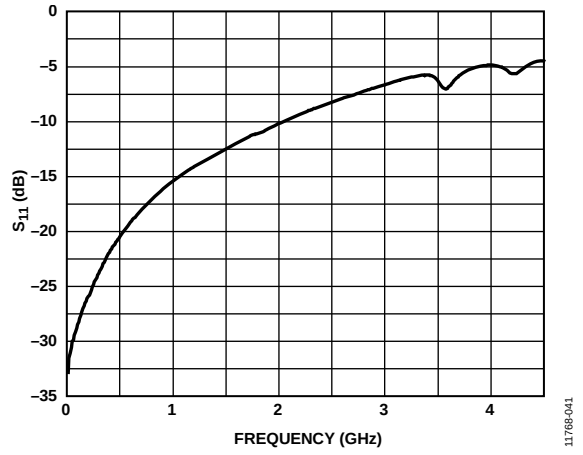

Figure 32. S_{11} at RF Input Port, 10 MHz to 4.5 GHz with 52.3 Ω Shunt Resistor at RF Input Port

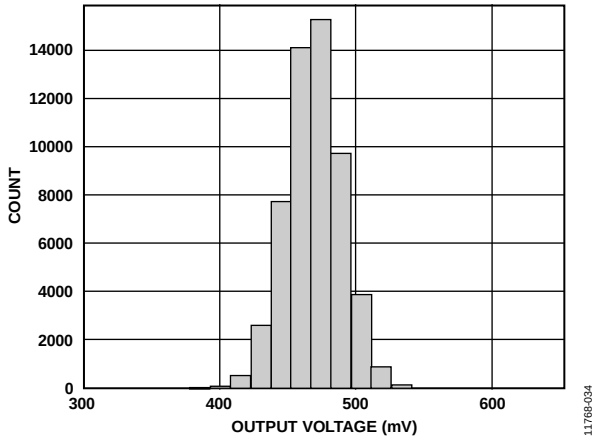

Figure 33. Distribution of V_{LOG} at 900 MHz, 25°C, P_{IN} = −30 dBm

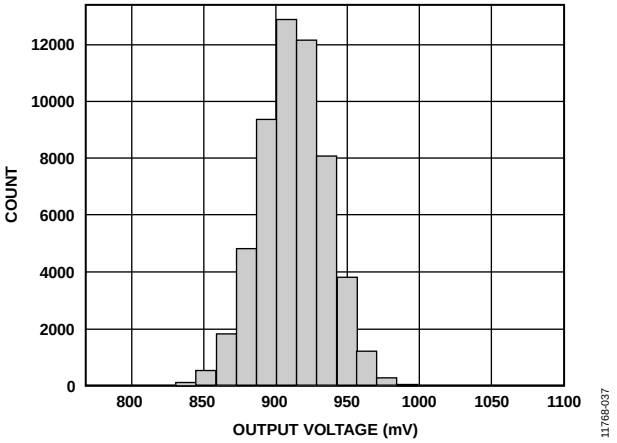

Figure 36. Distribution of V_{LOG} at 900 MHz, 25°C, P_{IN} = −6 dBm

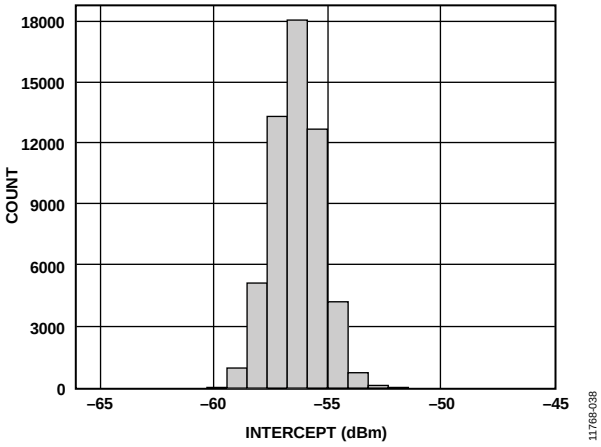

Figure 34. Distribution of Intercept at 900 MHz, 25°C

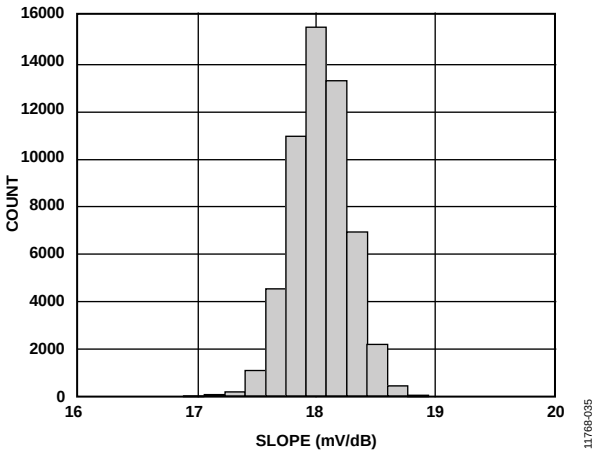

Figure 37. Distribution of Slope at 900 MHz, 25°C

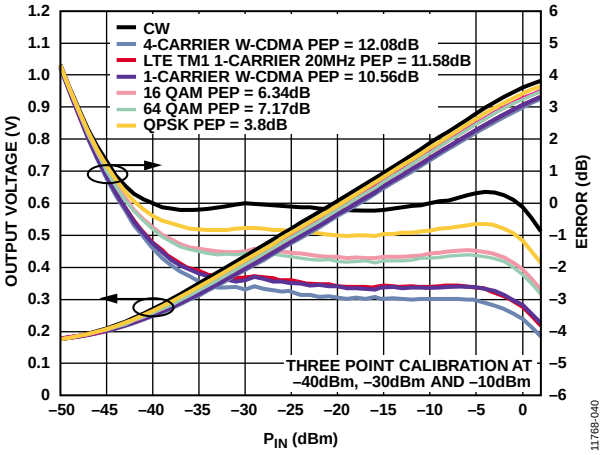

Figure 35. Error from CW Linear Reference vs. Signal Modulation (Four-Carrier W-CDMA, LTE TM1 One-Carrier 20 MHz, One-Carrier W-CDMA, 16 QAM, 64 QAM, QPSK), Frequency = 100 MHz

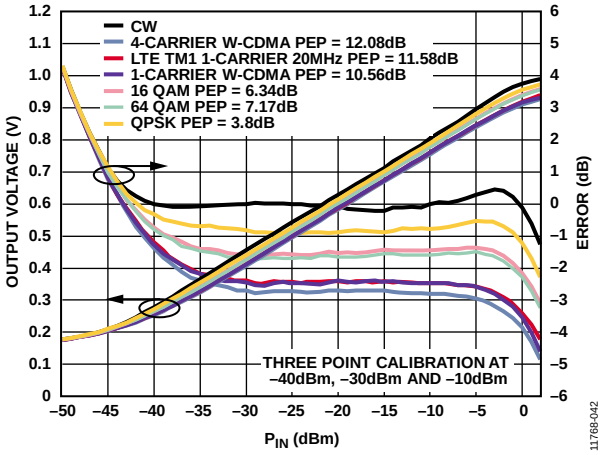

Figure 38. Error from CW Linear Reference vs. Signal Modulation (Four-Carrier W-CDMA, LTE TM1 One-Carrier 20 MHz, One-Carrier W-CDMA, 16 QAM, 64 QAM, QPSK), Frequency = 2.14 GHz

MEASUREMENT SETUPS

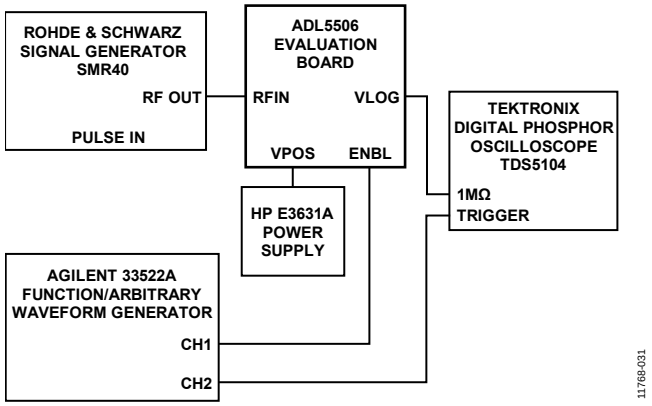

Figure 39. Hardware Configuration for Output Response to ENBL Pin Gating Measurements

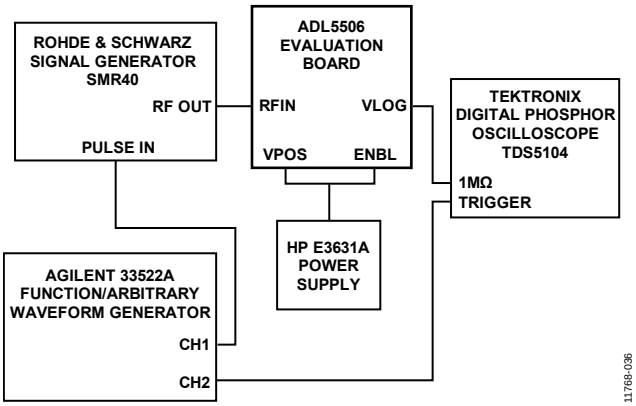

Figure 40. Hardware Configuration for Output Response to RF Pulse Input Measurements

THEORY OF OPERATION

The ADL5506 is a logarithmic detector (log amp), based on the principle of successive compression. It is similar in design to the AD8312 and is fabricated on an advanced BiCMOS process. It comes in a smaller 0.8 mm × 1.2 mm WLCSP package and offers 4.5 GHz RF bandwidth. Figure 41 shows the main features of the ADL5506 in block schematic form.

The ADL5506 combines two key functions needed for the measurement of signal level over a moderately wide dynamic range. First, it provides the amplification needed to respond to small signals in a chain of four amplifier/limiter cells, each having a small signal gain of 10 dB and a bandwidth of approximately 4.5 GHz. At the output of each amplifier stage is a full wave rectifier, essentially a square law detector cell that converts the RF signal voltages to a fluctuating current with an average value that increases with signal level. A further passive detector stage is added preceding the first stage. Therefore, there are five detectors, each separated by 10 dB, spanning about 50 dB of dynamic range. The overall accuracy at the extremes of this total range, viewed as the deviation from an ideal logarithmic response, that is, the log conformance error, can be judged by referencing Figure 5, Figure 7, and Figure 8, which show that errors across the central 40 dB are moderate. These figures show how the conformance to an ideal logarithmic function varies with temperature, frequency, and supply voltage.

The output of these detector cells is in the form of a differential current, making their summation a simple matter. It can easily be shown that such summation closely approximates a logarithmic function. This result is then converted to a voltage at the VLOG pin through a high gain stage. This output is connected back to a voltage-to-current (V-to-I) stage, in such a manner that V_{LOG} is a logarithmic measure of the RF input voltage with a slope and intercept controlled by the design. For a fixed termination resistance at the input of the ADL5506, a given voltage corresponds to a certain power level.

The external termination added before the ADL5506 determines the effective power scaling. This often takes the form of a simple resistor (52.3 Ω provides a net 50 Ω input), but more elaborate matching networks can be used. This impedance determines the logarithmic intercept, the input power for which the output crosses the baseline (V_{LOG} = 0 V) if the function were continuous for all values of input. Because this is never the case for a practical log amp, the intercept refers to the value obtained by the minimum error, straight line fit to the actual graph of V_{LOG} vs. input power. The quoted values in Table 1 assume a sinusoidal (CW) signal. Where there is complex modulation, as in CDMA, the calibration of the power response needs to be adjusted accordingly. Where a true power (waveform independent) response is needed, consider the use of an rms responding detector, such as the ADL5504.

However, in terms of the logarithmic slope, the amount by which the output V_{LOG} changes for each decibel of input change (voltage or power), is, in principle, independent of waveform or termination impedance. In practice, it usually falls off at higher frequencies because of the declining gain of the amplifier stages and other effects in the detector cells. For the ADL5506, the slope at 30 MHz is 18.8 mV/dB and falls slightly as frequency increases to about 16.7 mV/dB at 4.5 GHz. These values are sensibly independent of temperature and almost completely unaffected by supply voltages of 2.7 V to 5.5 V.

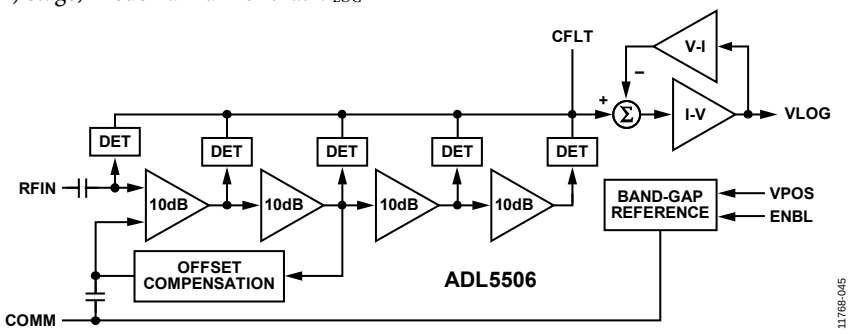

Figure 41. Block Schematic

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 42 shows the basic connections for measurement mode. A supply voltage of 2.5 V to 5.5 V is required. Decouple the supply to the VPOS pin with a low inductance 0.1 µF surface-mount ceramic capacitor. A series resistor of about 10 Ω can be added; this resistor slightly reduces the supply voltage to the ADL5506 and depends on the load resistance at the output to ground. Avoid its use in applications where the power supply voltage is very low. A series inductor provides similar power supply filtering with minimal drop in supply voltage.

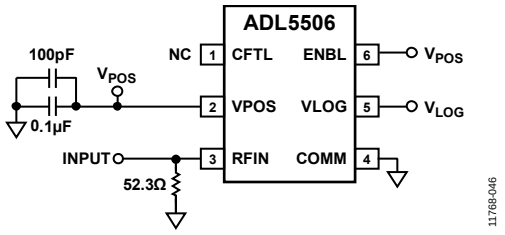

Figure 42. Basic Connections

The ADL5506 has an internal input coupling capacitor. This eliminates the need for external ac coupling. In this example, a broadband input match is achieved by connecting a 52.3 Ω resistor between RFIN and ground. This resistance combines with the internal input impedance to give an overall broadband input resistance of 50 Ω. Several other coupling methods are possible; these are described in the Input Coupling Options section.

Ensure that the load resistance on V_{LOG} is not lower than 600 Ω so that the full-scale output can be generated with the limited available sourcing current of 4 mA. Figure 43 shows the logarithmic conformance under the same conditions.

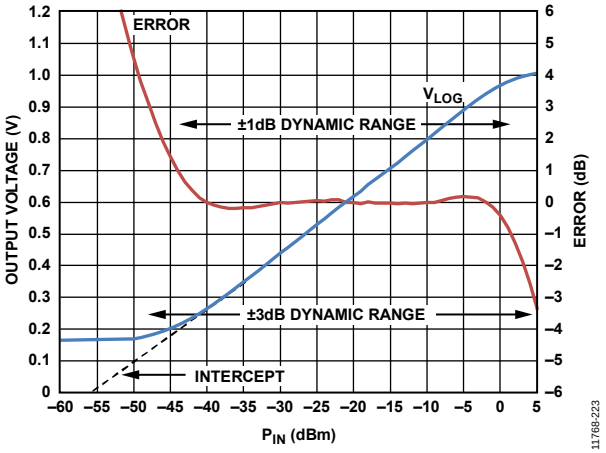

Figure 43. V_{LOG} and Log Conformance Error vs. Input Level at 900 MHz

TRANSFER FUNCTION IN TERMS OF SLOPE AND INTERCEPT

The transfer function of the ADL5506 is characterized in terms of its slope and intercept. The logarithmic slope is defined as the change in the RSSI output voltage for a 1 dB change at the input. For the ADL5506, the slope is nominally 18 mV/dB. Therefore, a 10 dB change at the input results in a change at the output of approximately 180 mV. Figure 43 shows the range over which the device maintains its constant slope. The dynamic range can be defined as the range over which the error remains within a certain band, usually ±1 dB or ±3 dB. In Figure 43 for example, the ±1 dB dynamic range is approximately 46 dB (from −44 dBm to +2 dBm).

The intercept is the point at which the extrapolated linear response intersects the horizontal axis (see Figure 43). Using the slope and intercept, calculate the output voltage for any input level within the specified input range, or calculate the input level from the output voltage by the following complementary equations:

$$V_{LOG} = V_{SLOPE} \times (P_{IN} - P_O)$$

$$P_{IN} = (V_{LOG}/V_{SLOPE}) + P_O$$

where:
V_{LOG} is the demodulated and filtered RSSI output, in V.
V_{SLOPE} is the logarithmic slope, expressed in V/dB.
P_{IN} is the input signal, expressed in decibels relative to some reference level (dBm in this case).
P_O is the logarithmic intercept, expressed in decibels relative to the same reference level.

For example, at an input level of −27 dBm, the V_{LOG} output voltage is

$$V_{LOG} = 0.018 \text{ V/dB} \times [-27 \text{ dBm} - (-56 \text{ dBm})] = 0.522 \text{ V}$$

LOG CONFORMANCE ERROR CALCULATION

Log conformance error is expressed in terms of the deviation in the output voltage between the measured V_{LOG} and the V_{LOG} calculated with an ideal log transformation function. Ideally, the measured V_{LOG} output at a particular input power, as plotted in Figure 44, must not deviate from the calculated value of V_{LOG} at that same input power. Setting the measured V_{LOG} to the right side of the preceding equation and rearranging yields

$$\frac{V_{LOG\,MEASURED}(P_{IN})}{V_{SLOPE}} - P_{IN} + P_O = 0$$

In actuality, this does not always calculate to zero. The finite calculation that results is the log conformance error, as follows:

$$Error(P_{IN}) = \frac{V_{LOG\,MEASURED}(P_{IN})}{V_{SLOPE}} - P_{IN} + P_O = 0$$

where *Error* is in dB.

When more than two calibration points are chosen to compute the error, the error computation must be done in a piece-wise fashion. For the ADL5506, three calibration points were chosen in characterization to compute the log conformance error of the ADL5506. For example, one set of calibration points used was −40 dBm, −30 dBm, and −10 dBm. With three calibration points, two regions of error are computed, Region A and Region B (see Figure 45) To compute the error, first compute two slopes and two intercepts: one slope and intercept for Region A and the other slope and intercept for Region B. Note that the error is zero at each calibration point.

$$V_{SLOPE\_A} = \frac{V_{LOG2} - V_{LOG1}}{P_{IN2} - P_{IN1}}$$

$$V_{SLOPE\_B} = \frac{V_{LOG3} - V_{LOG2}}{P_{IN3} - P_{IN2}}$$

Next, find the two intercepts. (The two intercept points can be computed with the same calibration points, middle point for both, with the slope being different for the two intercept points.)

$$P_{O\_A} = \frac{V_{LOG2}}{V_{SLOPE\_A}} + P_{IN2}$$

$$P_{O\_B} = \frac{V_{LOG3}}{V_{SLOPE\_B}} + P_{IN3}$$

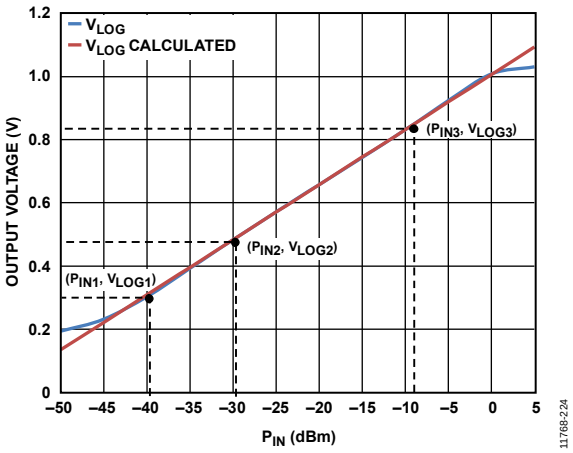

Figure 44. V_{LOG} vs. P_{IN}

The log conformance error for Region A, which is from the low end of the input power range to P_{IN2} is as follows:

$$Error_A(P_{IN}) = \frac{V_{LOG}(P_{IN})}{V_{SLOPE\_A}} - P_{IN} + P_{O\_A}$$

The log conformance error for Region B, which is from P_{IN2} to the upper end of the input power range is as follows:

$$Error_B(P_{IN}) = \frac{V_{LOG}(P_{IN})}{V_{SLOPE\_B}} - P_{IN} + P_{O\_B}$$

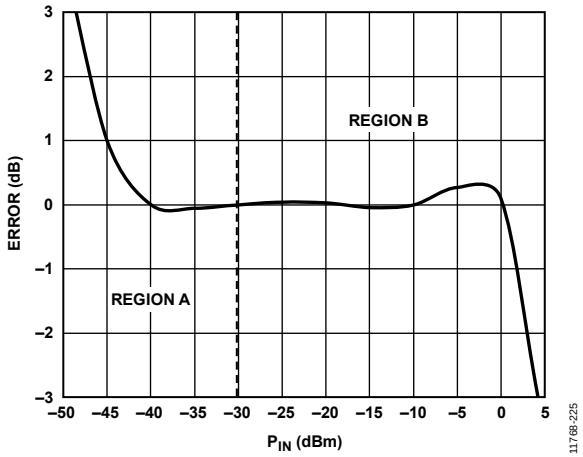

Figure 45. Error vs. P_{IN}

For four calibration points, there are three regions of error computed.

Filter Capacitor

The video bandwidth of V_{LOG} is approximately 3.5 MHz. In CW applications where the input frequency is much higher than this, no further filtering of the demodulated signal is required. Where there is a low frequency modulation of the carrier amplitude, however, reduce the low-pass corner by the addition of an external filter capacitor, C_{FLT}. The video bandwidth is related to C_{FLT} by

$$Video\ Bandwidth = \frac{1}{2\pi \times 13\,\text{k}\Omega \times (3.5\,\text{pF} + C_F)}$$

Input Coupling Options

The internal 5 pF coupling capacitor of the ADL5506, along with the low frequency input impedance of 1.7 kΩ, gives a high-pass input corner frequency of approximately 19 MHz. This sets the minimum operating frequency. Figure 46 to Figure 48 show three options for input coupling. A broadband resistive match can be implemented by connecting a shunt resistor to ground at RFIN (see Figure 46). This 52.3 Ω resistor (other values can also be used to select different overall input impedances) combines with the input impedance of the AD5506 to give a broadband input impedance of 50 Ω. While the input resistance and capacitance (R_{IN} and C_{IN}) varies by a maximum of approximately ±20% from device to device, the dominance of the external shunt resistor means that the variation in the overall input impedance is close to the tolerance of the external resistor. Achieve better return loss by placing the 52.3 Ω shunt resistor as near the device under test (DUT) as possible.

A reactive match can also be implemented, as shown in Figure 47. This is not recommended at low frequencies because device tolerances dramatically vary the quality of the match due to the large input resistance. For low frequencies, the option shown in Figure 46 or Figure 48 is recommended.

In Figure 47, the matching components are drawn as general reactances. Depending on the frequency, the input impedance at that frequency and the availability of standard value components, either a capacitor or an inductor, is used. As in the previous case, the input impedance at a particular frequency is plotted on a Smith Chart and matching components are chosen (Shunt or Series L, or Shunt or Series C) to move the impedance to the center of the chart. Matching components for specific frequencies can be calculated using the Smith Chart (see Figure 17). Table 4 outlines the input impedances for some commonly used frequencies.

The impedance matching characteristics of a reactive matching network provide voltage gain ahead of the ADL5506, which increases device sensitivity (see Table 4). The voltage gain is calculated by

$$Voltage\ Gain_{dB} = 20\log_{10}\sqrt{\frac{R2}{R1}}$$

where:
R2 is the input impedance of the ADL5506.
R1 is the source impedance to which the ADL5506 is being matched.

Note that this gain is only achieved for a perfect match. Component tolerances and the use of standard values tend to reduce gain.

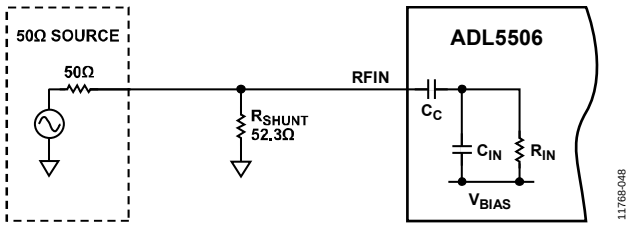

Figure 46. Broadband Resistive Method for Input Coupling

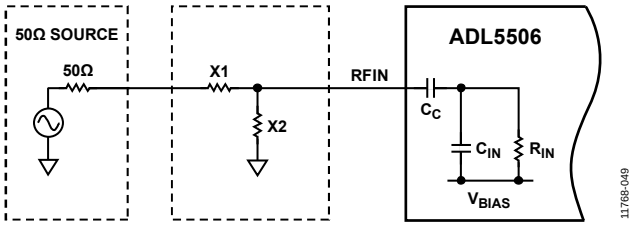

Figure 47. Narrow-Band Reactive Method for Input Coupling

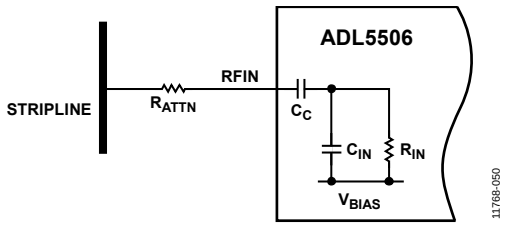

Figure 48. Series Attenuation Method for Input Coupling

Figure 48 shows a third method for coupling the input signal into the ADL5506 in applications where the input signal is larger than the input range of the log amp. A series resistor, connected to the RF source, combines with the input impedance of the ADL5506 to resistively divide the input signal being applied to the input. This has the advantage of very little power being tapped off in RF power transmission applications.

Table 4. Input Impedance with 52.3 Ω Shunt for Select Frequency

Frequency	S_{11}		Impedance Ω
(GHz)	Real	Imaginary	(Series)
0.05	+0.0023	−0.031	50.14 − j3.10
0.1	−0.014	−0.033	48.48 − j3.21
0.9	−0.144	+0.007	37.37 − j0.51
1.9	−0.052	+0.282	38.66 − j23.73
2.2	+0.074	+0.329	45.89 − j34.09
2.5	+0.233	+0.312	61.85 − j45.48
3.0	+0.467	+0.096	131.91 − j32.64
3.5	+0.394	−0.305	81.58 − j66.25

Table 5. Raw Input Impedance for Select Frequency

Frequency	S_{11}		Impedance Ω
(GHz)	Real	Imaginary	(Series)
0.1	+0.838	−0.251	131.9 − j281.59
0.9	−0.206	+0.714	11.41 − j36.33
1.9	−0.571	+0.397	9.84 + j15.11
2.2	−0.284	+0.639	12.42 + j31.05
2.5	+0.077	+0.699	18.87 − j52.17
3.0	+0.564	+0.407	72.70 + j114.52
3.5	+0.602	−0.099	186.70 − j58.55

Effect of Waveform Type on Intercept

Although specified for input levels in decibels relative to 1 mW (dBm), the ADL5506 fundamentally responds to voltage and not to power. A direct consequence of this characteristic is that input signals of equal rms power but differing crest factors, produce different results at the output of the log amplifier.

The effect of differing signal waveforms is to shift the effective value of the intercept upwards or downwards. Graphically, this looks like a vertical shift in the transfer function of the log amplifier. The logarithmic slope, however, is not affected. For example, consider the case of the ADL5506 being alternately fed by an unmodulated sine wave and by a 64 QAM signal of the same rms power. The output voltage of the ADL5506 differs by the equivalent of 1.6 dB (31 mV) over the complete dynamic range of the device (with the output for a 64 QAM input being lower).

Figure 35 and Figure 38 shows the transfer function of the ADL5506 when driven by both an unmodulated sine wave and several different signal waveforms. For precision operation, calibrate the ADL5506 for each signal type that is driving it. To measure the rms power of a 64 QAM input, for example, add the millivolt equivalent of the decibel value of the intercept shift (18.5 mV/dB × 1.5 dB) to the output voltage of the ADL5506.

Temperature Drift at High Frequencies

Figure 23 and Figure 27 show the log slope and error over temperature for a 3.5 GHz and 4.5 GHz input signal, respectively. Error due to drift over temperature consistently remains within ±0.5 dB for a temperature range of 0°C to 85°C. Temperatures below 0°C begin to exhibit error beyond 0.5 dB with error becoming no worse than −3 dB typical at −40°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

Operation Above 4.5 GHz

The ADL5506 works at high frequencies but exhibits slightly higher output voltage temperature drift, especially at cold temperatures as described in the Temperature Drift at High Frequencies section. Figure 49 and Figure 50 show V_{LOG} vs. P_{IN} over frequency from 30 MHz to 6 GHz. The ADL5506 exhibits a significant intercept shift, high power ripple, and a continued decrease of the slope, which all contribute to a decrease in dynamic range. The changes in performance that occur as frequency is increased is partly due to less energy transferring into the device and partly to the bandwidth limitation of the limiting amplifier stages.

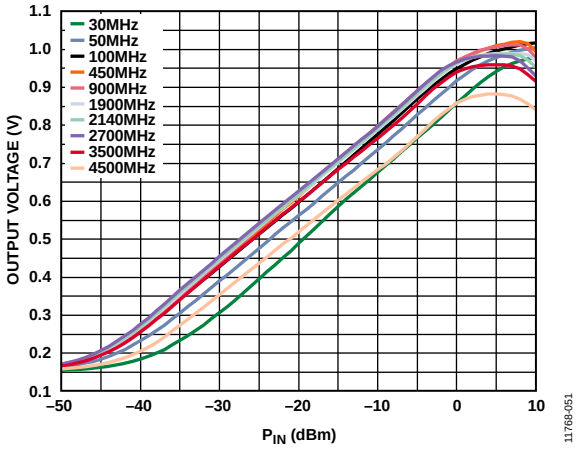

Figure 49. V_{LOG} vs. P_{IN} over Frequency (30 MHz to 4500 MHz)

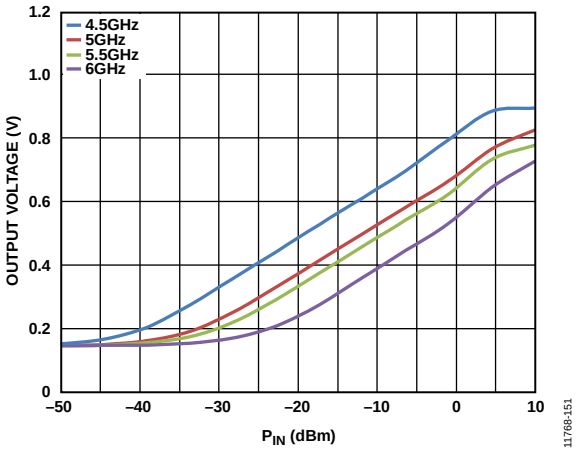

Figure 50. V_{LOG} vs. P_{IN} over Frequency (4.5 GHz to 6 GHz)

V_{LOG} Output Noise

The ADL5506 V_{LOG} output noise is shown in Figure 31 in the Typical Performance Characteristics section for Capacitor C_{FLT} = open. Placing capacitance from CFLT to VLOG decreases the noise spectral density and the integrated noise. The choice of the C_{FLT} value depends on the requirements pertaining to integrated noise and noise spectral density at a given frequency. Also, the value of C_{FLT} directly controls the video bandwidth of the output, and thus controls the output response time to an RF pulse (see the V_{LOG} Pulse Response Time section).

V_{LOG} Pulse Response Time

The ADL5506 V_{LOG} output response for rise and fall times to a given RF input pulse is quickest for C_{FLT} = open; that is, the only capacitance on the CFLT node is the internal capacitor. Adding off-chip capacitance from the CFLT pin to the VLOG pin decreases the video bandwidth and slows the output response to an RF input pulse. See the Filter Capacitor section for an approximate closed form equation for the V_{LOG} video bandwidth.

Figure 28 shows the response time when the ENBL pin is pulsed while having the VPOS pin connect to a 3.0 V supply and an RF signal applied at RFIN. The sharp pulse that is seen on VLOG preceding the actual response of the detectors, which happens approximately 0.5 µs later, is the power-up transient that occurs in the output stage. The upper voltage limit of these power-up transients is 2.25 V typical, for a 3.0 V supply. Ensure that these power-up transients do not overload the circuit that the VLOG pin drives.

Device Handling

The wafer level chip scale package consists of solder bumps connected to the active side of the die. The device is lead-free with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP package can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, take caution to avoid damaging the die. See the AN-617 Application Note for additional information. WLCSP devices are bumped die, and exposed die can be sensitive to light conditions, which can influence specified limits.

EVALUATION BOARD

Figure 51 shows the schematic of the ADL5506 evaluation board. The board is powered by a single supply in the 2.5 V to 5.5 V range. The power supply is decoupled by 100 pF and 0.1 µF capacitors. Enable the device by switching SW1 to the on position.

The RF input has a broadband match of 50 Ω using a single 52.3 Ω resistor at R7. More precise matching at spot frequencies is possible (see the Input Coupling Options section).

Table 6 details the various configuration options of the evaluation board. Figure 52 shows the layout of the evaluation board.

LAND PATTERN AND SOLDERING INFORMATION

Pad diameters of 0.20 mm are recommended with a solder mask opening of 0.30 mm. For the RF input trace, a trace width of 0.30 mm is used, which corresponds to a 50 Ω characteristic impedance for the dielectric material being used (FR4). All traces going to the pads are tapered down to 0.15 mm. For the RFIN line, the length of the tapered section is 0.20 mm.

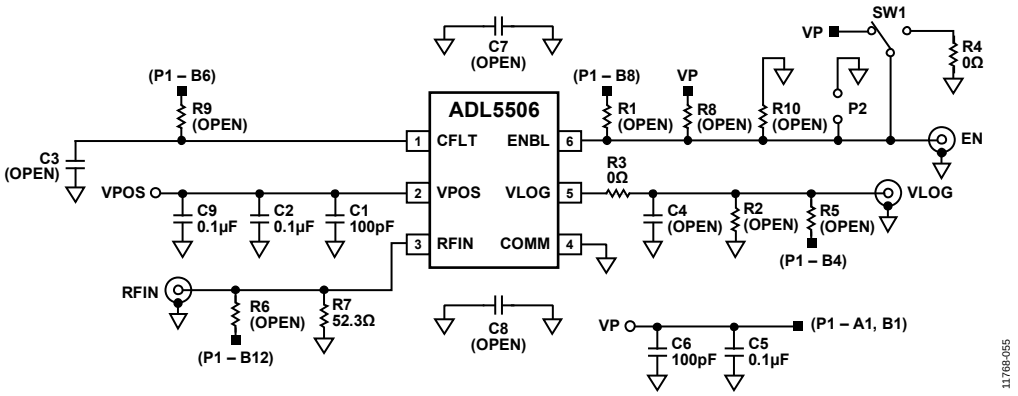

Figure 51. Evaluation Board Schematic

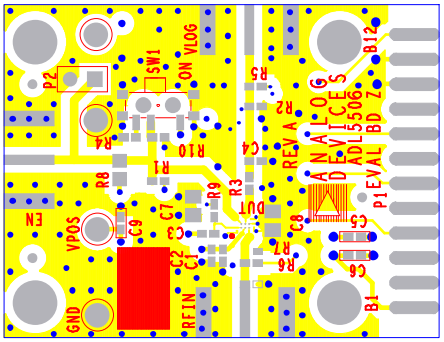

Figure 52. Layout of Evaluation Board, Component Side

Table 6. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOS, GND	Ground and supply vector pins.	Not applicable
C1, C2, C5, C6, C7, C8, C9	Power supply decoupling. Nominal supply decoupling of 0.1 µF and 100 pF.	C1, C6 = 100 pF (Size 0402), C2, C5, C9 = 0.1 µF (Size 0402), C7 = C8 = open (Size 0805)
R7	RF input interface. The 52.3 Ω resistor at R7 combines with the ADL5506 internal input impedance to give a broadband input impedance of around 50 Ω.	R7 = 52.3 Ω (Size 0402)
C3, C4, R2, R3	Output filtering. The combination of the internal 100 Ω output resistance and C4 produce a low-pass filter to reduce the output ripple of the VLOG output. The output can be scaled down using the resistor divider pads, R2 and R3.	R3 = 0 Ω (Size 0402), R2 = open (Size 0402), C3, C4 = open (Size 0402)
SW1, R4, R10, P2	Device enable. When SW1 is set to the on position, the ENBL pin is connected to the supply and the ADL5506 is in enable mode. When SW1 I set to the off position, the ENBL pin is grounded (through the 0 Ω resistor), putting the device in power-down mode.	R4 = 0 Ω (Size 0402), R10 = open (Size 0402), SW1= on position, P2 = not installed
P1, R1, R5, R6, R8, R9	Alternate interface. The end connector, P1, allows access to various ADL5506 signals. These signal paths are only used during factory test and characterization.	P1 = not installed, R1, R5, R6, R9 = open (Size 0402), R8 = open (Size 0805)

OUTLINE DIMENSIONS

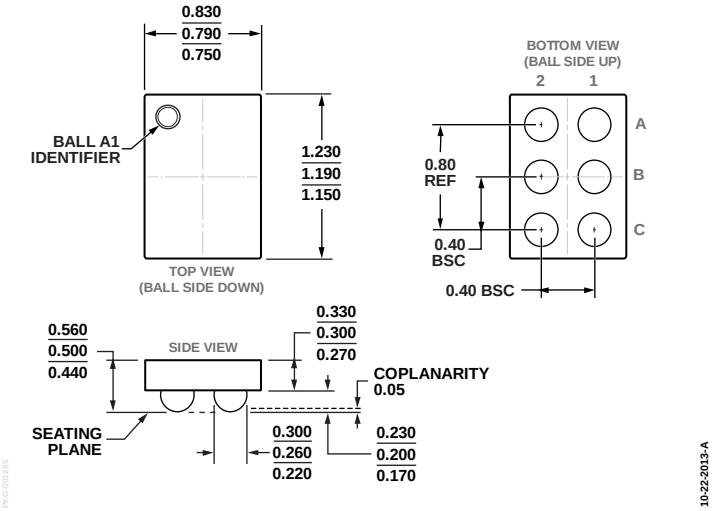

Figure 53. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5506ACBZ-R7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP], 7″ Tape and Reel	CB-6-14	CE	3,000
ADL5506-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.