

## FEATURES

**DC to >500 MHz operation**  
**Differential  $\pm 1$  V full-scale inputs**  
**Differential  $\pm 4$  mA full-scale output current**  
**Low distortion ( $\leq 0.05\%$  for 0 dBm input)**  
**Supply voltages from  $\pm 4$  V to  $\pm 9$  V**  
**Low power (280 mW typical at  $V_s = \pm 5$  V)**

## APPLICATIONS

**High speed real time computation**  
**Wideband modulation and gain control**  
**Signal correlation and RF power measurement**  
**Voltage controlled filters and oscillators**  
**Linear keyers for high resolution television**  
**Wideband true RMS**

## GENERAL DESCRIPTION

The AD834 is a monolithic, laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, with a transconductance bandwidth ( $R_L = 50 \Omega$ ) in excess of 500 MHz from either of the differential voltage inputs. In multiplier modes, the typical total full-scale error is 0.5%, dependent on the application mode and the external circuitry. Performance is relatively insensitive to temperature and supply variations due to the use of stable biasing based on a band gap reference generator and other design features.

To preserve the full bandwidth potential of the high speed bipolar process used to fabricate the AD834, the outputs appear as a differential pair of currents at open collectors. To provide a single-ended ground referenced voltage output, some form of external current-to-voltage conversion is needed. This may take the form of a wideband transformer, balun, or active circuitry such as an op amp. In some applications (such as power measurement), the subsequent signal processing may not need to have high bandwidth.

The transfer function is accurately trimmed such that when  $X = Y = \pm 1$  V, the differential output is  $\pm 4$  mA. This absolute calibration allows the outputs of two or more AD834 devices to be summed with precisely equal weighting, independent of the accuracy of the load circuit.

The AD834J, available in 8-lead PDIP and plastic SOIC packages, is specified over the commercial temperature range of  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . The AD834A is also available in 8-lead CERDIP and plastic SOIC packages operating over the industrial temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . The AD834SQ/883B, available in an 8-lead

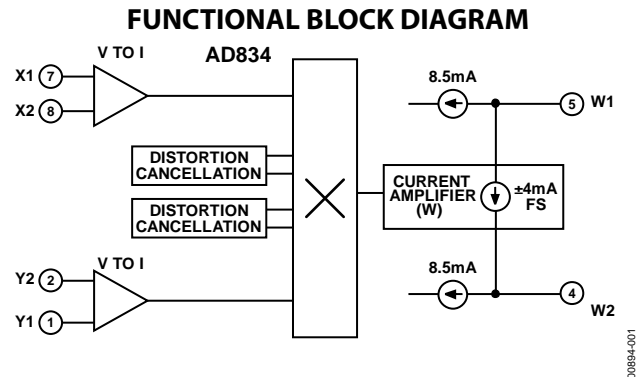


Figure 1.

CERDIP, operates over the military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . S-grade chips are also available.

Two application notes featuring the AD834 (AN-212 and AN-216) can be found at [www.analog.com](http://www.analog.com). For additional applications circuits, consult the [AD811](#) data sheet.

## PRODUCT HIGHLIGHTS

1. Combines high static accuracy (low input and output offsets and accurate scale factor) with very high bandwidth. As a four-quadrant multiplier or squarer, the response extends from dc to an upper frequency limited by packaging and external board layout considerations. Obtains a large signal bandwidth of  $>500$  MHz under optimum conditions.
2. Used in many high speed nonlinear operations, such as square rooting, analog division, vector addition, and rms-to-dc conversion. In these modes, the bandwidth is limited by the external active components.
3. Special design techniques result in low distortion levels (better than  $-60$  dB on either input) at high frequencies and low signal feedthrough (typically  $-65$  dB up to 20 MHz).
4. Exhibits low differential phase error over the input range—typically  $0.08^\circ$  at 5 MHz and  $0.8^\circ$  at 50 MHz. The large signal transient response is free from overshoot and has an intrinsic rise time of 500 ps, typically settling to within 1% in under 5 ns.
5. The nonloading, high impedance, differential inputs simplify the application of the AD834.

### Rev. F

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## REVISION HISTORY

### 6/12—Rev. E to Rev. F

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Change to Bias Current Parameter, Table 1 .....	3
Changes to Table 4 .....	6
Changes to Ordering Guide .....	19

### 5/09—Rev. D to Rev E

Updated Format .....	Universal
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### 4/02—Rev. C to Rev. D

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## SPECIFICATIONS

$T_A = 25^\circ\text{C}$  and  $\pm V_S = \pm 5\text{ V}$ , unless otherwise noted; dBm assumes  $50\ \Omega$  load. Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Table 1.

Parameters	Conditions	Min	Typ	Max	Unit
<b>MULTIPLIER PERFORMANCE</b>					
Transfer Function			$W = \frac{XY}{(1V)^2} \times 4\text{ mA}$		
Total Error <sup>1</sup>	$-1\text{ V} \leq X, Y < +1\text{ V}$		$\pm 0.5$	<b><math>\pm 2</math></b>	% FS
vs. Temperature (AD834A/AD834S Only)	$T_{\text{MIN}}$ to $T_{\text{MAX}}$		$\pm 1.5$	<b><math>\pm 3</math></b>	% FS
vs. Supplies (All Models) <sup>2</sup>	$\pm 4\text{ V}$ to $\pm 6\text{ V}$		0.1	<b>0.3</b>	% FS/V
Linearity <sup>3</sup>			$\pm 0.5$	<b><math>\pm 1</math></b>	% FS
Bandwidth <sup>4</sup>		500			MHz
Feedthrough, X	$X = \pm 1\text{ V}, Y = \text{nulled}$		0.2	<b>0.3</b>	% FS
Feedthrough, Y	$X = \text{nulled}, Y = \pm 1\text{ V}$		0.1	<b>0.2</b>	% FS
AC Feedthrough, X <sup>5</sup>	$X = 0\text{ dBm}, Y = \text{nulled}$				
	$f = 10\text{ MHz}$		-65		dB
	$f = 100\text{ MHz}$		-50		dB
AC Feedthrough, Y <sup>5</sup>	$X = \text{nulled}, Y = 0\text{ dBm}$				
	$f = 10\text{ MHz}$		-70		dB
	$f = 100\text{ MHz}$		-50		dB
<b>INPUTS (X1, X2, Y1, Y2)</b>					
Full-Scale Range	Differential	<b><math>\pm 1.1</math></b>	$\pm 1$		V
Clipping Level	Differential		$\pm 1.3$		V
Input Resistance	Differential		25		k $\Omega$
Offset Voltage			0.5	<b>3</b>	mV
vs. Temperature	$T_{\text{MIN}}$ to $T_{\text{MAX}}$		10		$\mu\text{V}/^\circ\text{C}$
vs. Supplies <sup>2</sup>	$\pm 4\text{ V}$ to $\pm 6\text{ V}$		100	<b>300</b>	mV
Bias Current			45		$\mu\text{A}$
Common-Mode Rejection	$f \leq 100\text{ kHz}; 1\text{ V p-p}$		70		dB
Nonlinearity, X	$Y = 1\text{ V}; X = \pm 1\text{ V}$		0.2	<b>0.5</b>	% FS
Nonlinearity, Y	$X = 1\text{ V}; Y = \pm 1\text{ V}$		0.1	<b>0.3</b>	% FS
Distortion, X	$X = 0\text{ dBm}, Y = 1\text{ V}$				
	$f = 10\text{ MHz}$		-60		dB
	$f = 100\text{ MHz}$		-44		dB
Distortion, Y	$X = 1\text{ V}, Y = 0\text{ dBm}$				
	$f = 10\text{ MHz}$		-65		dB
	$f = 100\text{ MHz}$		-50		dB
<b>OUTPUTS (W1, W2)</b>					
Zero Signal Current	Each output		8.5		mA
Differential Offset	$X = 0, Y = 0$		$\pm 20$	<b><math>\pm 60</math></b>	$\mu\text{A}$
vs. Temperature					$\text{nA}/^\circ\text{C}$
All Models	$T_{\text{MIN}}$ to $T_{\text{MAX}}$		40		$\mu\text{A}$
AD834A/AD834S Only				<b><math>\pm 60</math></b>	$\mu\text{A}$
Scaling Current	Differential	3.96	4	4.04	mA
Output Compliance		4.75		9	V
Noise Spectral Density	$f = 10\text{ Hz}$ to $1\text{ MHz}$		16		$\text{nV}/\sqrt{\text{Hz}}$
	Outputs into $50\ \Omega$ Load				

Parameters	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES					
Operating Range	T <sub>MIN</sub> to T <sub>MAX</sub>	±4		±9	V
Quiescent Current <sup>6</sup>					
+V <sub>S</sub>			11	<b>14</b>	mA
-V <sub>S</sub>			28	<b>35</b>	mA

<sup>1</sup> Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output. See Figure 16.

<sup>2</sup> Both supplies taken simultaneously; sinusoidal input at  $f \leq 10$  kHz.

<sup>3</sup> Linearity is defined as residual error after compensating for input offset voltage, output offset current, and scaling current errors.

<sup>4</sup> Bandwidth is guaranteed when configured in squarer mode. See Figure 12.

<sup>5</sup> Sine input; relative to full-scale output; zero input port nulled; represents feedthrough of the fundamental.

<sup>6</sup> Negative supply current is equal to the sum of positive supply current, the signal currents into each output, W1 and W2, and the input bias currents.

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Ratings
Supply Voltage (+V <sub>S</sub> to -V <sub>S</sub> )	18 V
Internal Power Dissipation	500 mW
Input Voltages (X1, X2, Y1, Y2)	+V <sub>S</sub>
Operating Temperature Ranges	
Commercial, AD834J Only	0°C to 70°C
Industrial, AD834A Only	-40°C to +85°C
Military AD834S/883B Only	-55°C to +125°C
Storage Temperature Range (Q)	-65°C to +150°C
Storage Temperature Range (R, N)	-65°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD Rating	500 V

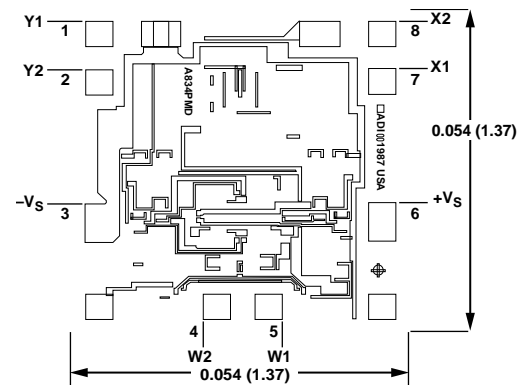
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL CHARACTERISTICS

Table 3.

Package	$\theta_{JA}$	$\theta_{JA}$	Unit
8-Lead CERDIP (Q)	110	110	°C/W
8-Lead SOIC (R)	165	165	°C/W
8-Lead PDIP (N)	99	99	°C/W

## CHIP DIMENSIONS AND BONDING DIAGRAM



NOTES  
1. DIMENSIONS SHOWN IN INCHES AND (mm). CONTACT FACTORY FOR LATEST DIMENSIONS.

00894-003

Figure 2. Metallization Photograph

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

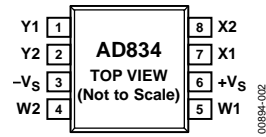


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Y1	Positive Y Input
2	Y2	Negative Y Input
3	-Vs	Negative Power Supply
4	W2	Open-Collector Output
5	W1	Open-Collector Output
6	+Vs	Positive Power Supply.
7	X1	Positive X Input
8	X2	Negative X Input

### TYPICAL PERFORMANCE CHARACTERISTICS

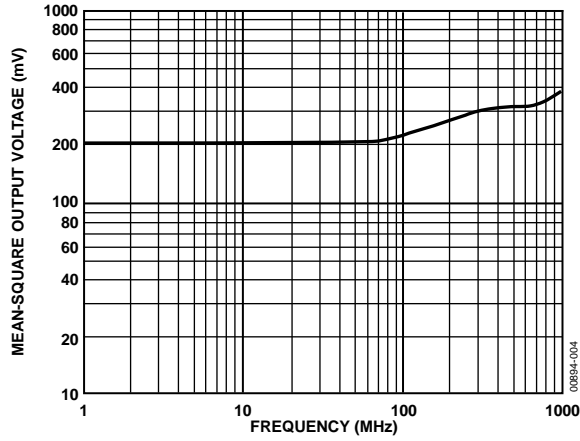


Figure 4. Mean-Square Output vs. Frequency

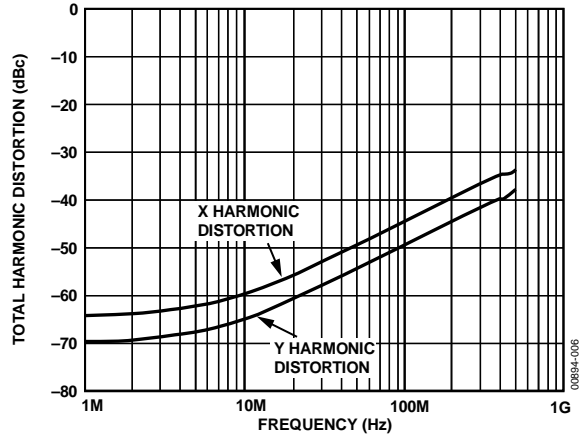


Figure 6. Total Harmonic Distortion vs. Frequency

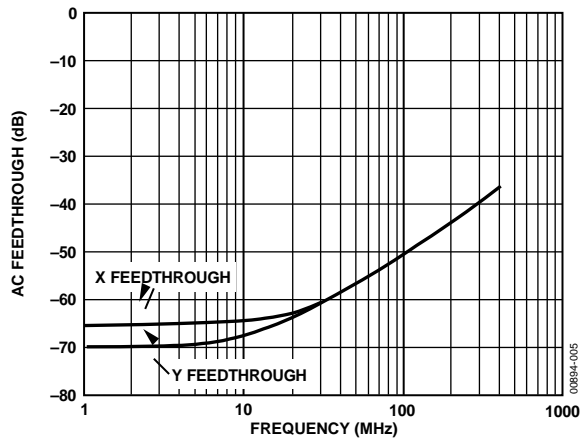


Figure 5. AC Feedthrough vs. Frequency

TEST CIRCUITS

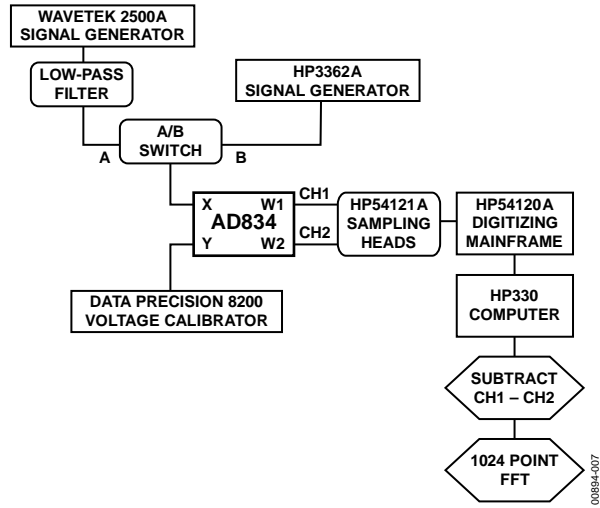


Figure 7. Test Configuration for Measuring AC Feedthrough and Total Harmonic Distortion

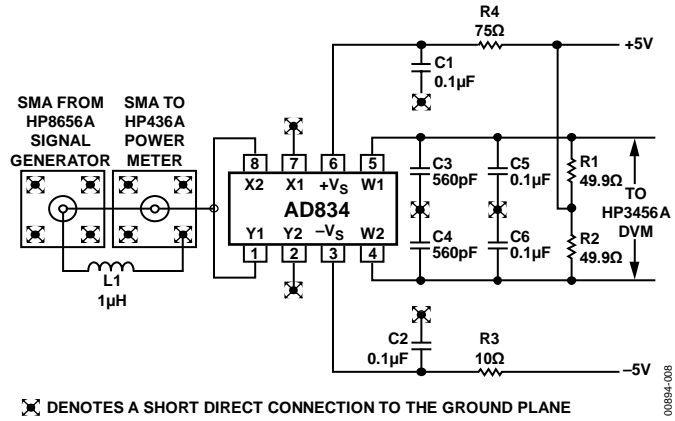
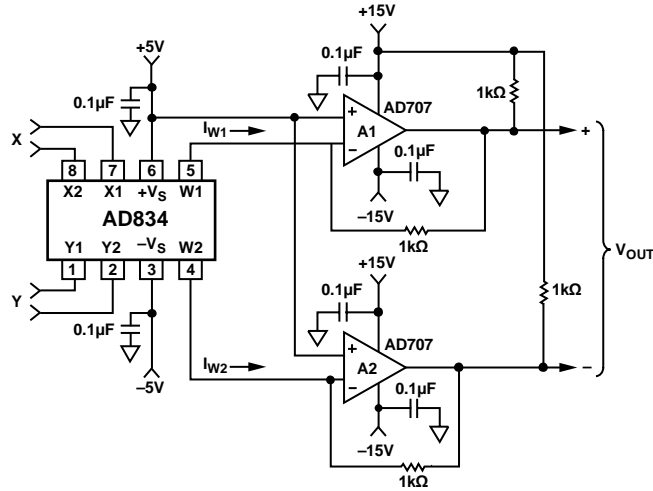


Figure 8. Bandwidth Test Circuit

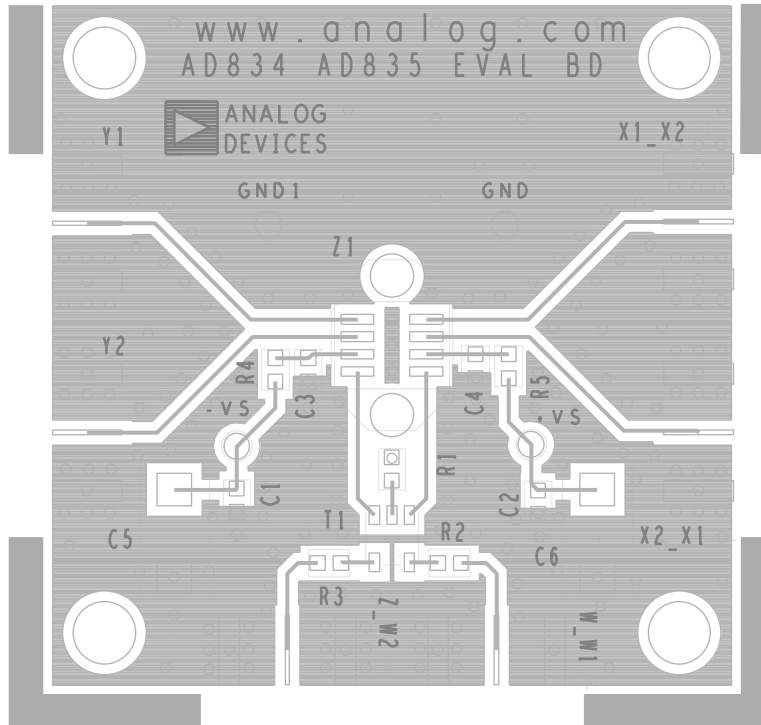




- NOTES
1. R1, R2 SHOULD BE PRECISION TYPE RESISTOR ( $\pm 0.1\%$ ).
  2. ABSOLUTE VALUE ERRORS OF R1, R2 CAUSE A SMALL FACTOR ERROR.
  3. R1, R2 MISMATCHES ARE EXPRESSED AS LINEARITY ERRORS.
  4.  $V_{OUT} = I_{W1} R1 - I_{W2} R2$   
(IF  $R1 = R2$ ,  $V_{OUT} = I_W R1$ ).

00894-009

Figure 9. Low Frequency Test Circuit



00894-109

Figure 10. Example Layout for SOIC

## EXPLANATION OF TYPICAL PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

Figure 4 is a plot of the mean-square output vs. frequency for the test circuit of Figure 8. Note that the rising response is due to package resonances.

For frequencies above 1 MHz, ac feedthrough is dominated by static nonlinearities in the transfer function and the finite offset voltages. The offset voltages cause a small fraction of the fundamental to appear at the output, and can be nulled out (see Figure 5).

THD data represented in Figure 6 is dominated by the second harmonic, and is generated with 0 dBm input on the ac input and 1 V on the dc input. For a given amplitude on the ac input, THD is relatively insensitive to changes in the dc input amplitude. Varying the ac input amplitude while maintaining a constant dc input amplitude affects THD performance.

The squarer configuration shown in Figure 8 is used to determine wideband performance because it eliminates the need for (and the response uncertainties of) a wideband measurement device at the output. The wideband output of a squarer configuration is a fluctuating current at twice the input frequency with a mean value proportional to the square of the input amplitude.

By placing the capacitors, C3/C5 and C4/C6, across the load resistors, R1 and R2, a simple low-pass filter is formed, and the mean-square value is extracted. The mean-square response can be measured using a DVM connected across R1 and R2.

Care should be taken when laying out the board. When using the DIP package, mount the IC socket on a ground plane with a clear area in the rectangle formed by the pins. This is important because significant transformer action can arise if the pins pass through individual holes in the board; improperly constructed test jigs have caused oscillation at 1.3 GHz.

### THEORY OF OPERATION

Figure 11 is a functional equivalent of the AD834. There are three differential signal interfaces: the two voltage inputs ( $X = X1 - X2$  and  $Y = Y1 - Y2$ ), and the current output ( $W$ ) which flows in the direction shown in Figure 11 when  $X$  and  $Y$  are positive. The outputs ( $W1$  and  $W2$ ) each have a standing current of typically 8.5 mA.

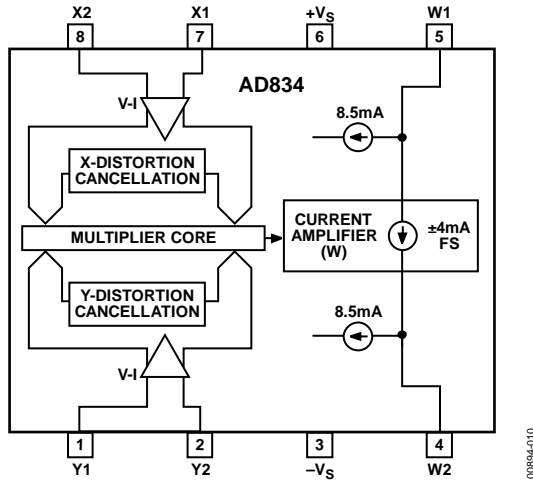


Figure 11. Functional Block Diagram

The input voltages are first converted to differential currents that drive the translinear core. The equivalent resistance of the voltage-to-current ( $V-I$ ) converters is about 285  $\Omega$ , which results in low input related noise and drift. However, the low full-scale input voltage results in relatively high nonlinearity in the  $V-I$  converters. This is significantly reduced by the use of distortion cancellation circuits, which operate by Kelvin sensing the voltages generated in the core—an important feature of the AD834.

The current mode output of the core is amplified by a special cascode stage that provides a current gain of nominally  $\times 1.6$ , trimmed during manufacturing to set up the full-scale output current of  $\pm 4$  mA. This output appears at a pair of open collectors that must be supplied with a voltage slightly above the voltage on Pin 6. As shown in Figure 12, this can be arranged by inserting a resistor in series with the supply to Pin 6 and taking the load resistors to the full supply. With  $R3 = 60 \Omega$ , the voltage drop across it is about 600 mV. Using two 50  $\Omega$  load resistors, the full-scale differential output voltage is  $\pm 400$  mV. For best performance, the voltage on the output open-collectors (Pin 4 and Pin 5) must be higher than the voltage on Pin 6 by about 200 mV, as shown in Figure 12.

The full bandwidth potential of the AD834 can be realized only when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1 GHz, and the actual upper frequency in a typical application is usually determined by the care with which the layout is affected. Note that  $R4$  (in series with the  $-V_s$  supply) carries about 30 mA and thus introduces a

voltage drop of about 150 mV. It is made large enough to reduce the  $Q$  of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may be used.

For best performance, use termination resistors at the inputs, as shown in Figure 12. Note that although the resistive component of the input impedance is quite high (about 25 k $\Omega$ ), the input bias current of typically 45  $\mu$ A can generate significant offset voltages if not compensated. For example, with a source and termination resistance of 50  $\Omega$  (net source of 25  $\Omega$ ) the offset is  $25 \Omega \times 45 \mu$ A = 1.125 mV. The offset can be almost fully cancelled by including (in this example) another 25  $\Omega$  resistor in series with the unused input. (In Figure 12, a 25  $\Omega$  resistor would be added from  $X1$  to GND and  $Y2$  to GND.) To minimize crosstalk, ground the input pins closest to the output ( $X1$  and  $Y2$ ); the effect is merely to reverse the phase of the  $X$  input and thus alter the polarity of the output.

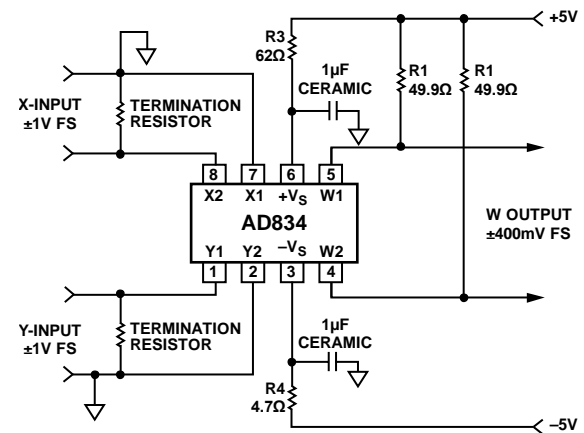


Figure 12. Basic Connections for Wideband Operation

### TRANSFER FUNCTION

The Output Current  $W$  is the linear product of input voltages ( $X$  and  $Y$ ) divided by  $(1 \text{ V})^2$  and multiplied by the scaling current of 4 mA:

$$W = \frac{XY}{(1 \text{ V})^2} 4 \text{ mA}$$

With the understanding that the inputs are specified in volts, the following simplified expression can be used:

$$W = (XY)4 \text{ mA}$$

Alternatively, the full transfer function can be written as

$$W = \frac{XY}{1 \text{ V}} \times \frac{1}{250 \Omega}$$

When both inputs are driven to their clipping level of about 1.3 V, the peak output current is roughly doubled to  $\pm 8$  mA, but distortion levels become very high.

**BIASING THE OUTPUT**

The AD834 has two open collector outputs as shown in Figure 13. The +V<sub>S</sub> pin, Pin 6, is tied to the base of the output NPN transistors. The following general guidelines maximize performance of the AD834.

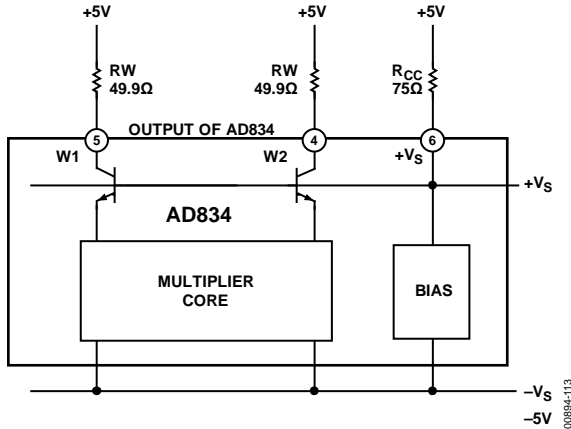


Figure 13. Output Stage Block Diagram

**SITUATION 1**

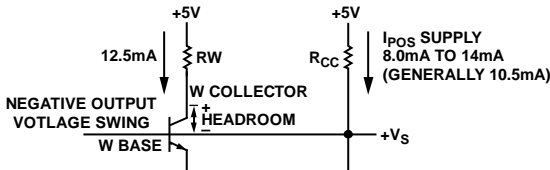


Figure 14. Negative Swing

Figure 14 shows the currents at the input when the AD834 swings negative. Generally, +V<sub>S</sub> should be biased at +4 V or higher. For best performance, use resistor values that do not saturate the output transistors. Allowing for adequate transistor headroom reduces distortion.

$$\text{Headroom} = \text{Voltage at } W_{\text{COLLECTOR}} - \text{Voltage at } W_{\text{BASE}}$$

When either output swings negative, the maximum current flows through the RW resistors. It is in this situation that headroom is at a minimum.

$$\text{Headroom}_{\text{NEGATIVE SWING}} = (I_{\text{POS SUPPLY}} \times R_{\text{CC}}) - (12.5 \text{ mA} \times R_{\text{W}})$$

Try to keep headroom at or above 200 mV to maintain adequate range.  $\text{Headroom} \geq 200 \text{ mV}$ .

This recommendation addresses the positive swing of the output as shown in Figure 15. It is sometimes difficult to meet this for negative output swing.

**SITUATION 2**

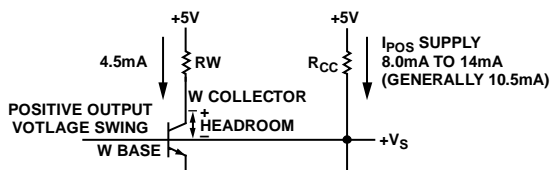


Figure 15. Positive Output Swing

The current through RW is smaller for positive output swings.

$$\text{Headroom}_{\text{POSITIVE SWING}} = (I_{\text{POS SUPPLY}} \times R_{\text{CC}}) - (4.5 \text{ mA} \times R_{\text{W}})$$

For dc applications or applications where distortion is not a concern, the headroom may be zero or as low as -200 mV. However, for most cases, size the resistors to give the output adequate headroom.

**TRANSFORMER COUPLING**

In many high frequency applications where baseband operation is not required at either inputs or the output, transformer coupling can be used. Figure 16 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs, W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design depends entirely on the application. Transformers can also be used at the inputs. Center-tapped transformers can reduce high frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

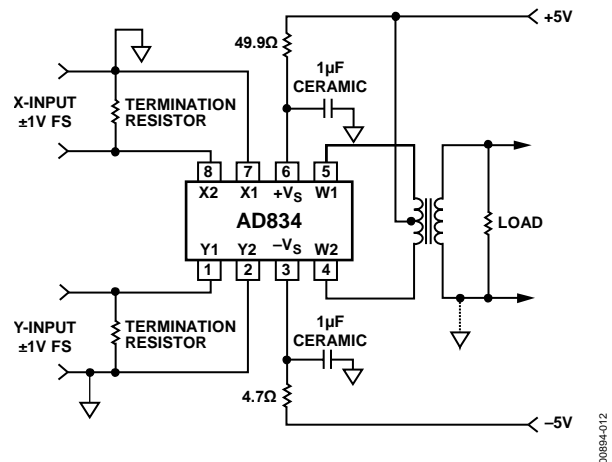


Figure 16. Transformer-Coupled Output

A particularly effective type of transformer is the balun<sup>1</sup>, which is a short length of transmission line wound onto a toroidal ferrite core. Figure 17 shows this arrangement used to convert the bal(anced) output to an un(balanced) one (therefore, the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. First, the load should now be equal to the characteristic impedance of the line (although this is usually not critical for short line lengths). The collector load resistors, R<sub>W</sub>, can also be chosen to reverse-terminate the line, but again this is only necessary when an electrically long line is used. In most cases, R<sub>W</sub> is made as large as the dc conditions allow to minimize power loss to the load. The line can be a miniature coaxial cable or a twisted pair.

<sup>1</sup> For a good treatment of baluns, see *Transmission Line Transformers* by Jerry Sevick; American Radio Relay League publication.

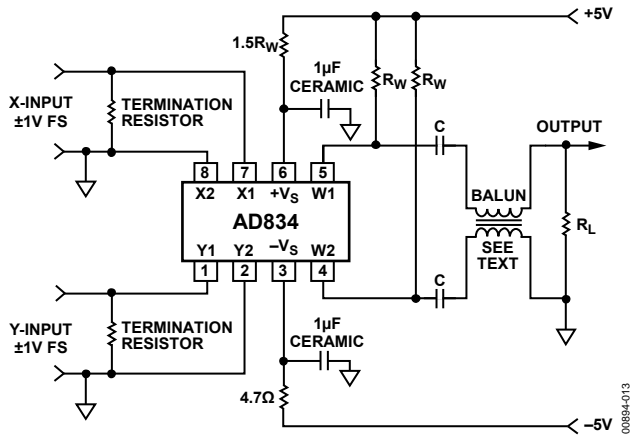


Figure 17. Using a Balun at the Output

Note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; therefore, the upper bandwidth of the balun usually exceeds that of the multiplier. This is unlike a conventional transformer where the signal is conveyed as a flux in a magnetic core and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors, C, are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

**WIDEBAND MULTIPLIER CONNECTIONS**

When operation down to dc and a ground based output are necessary, the configuration shown in Figure 18 can be used. The element values were chosen in this example to result in a full-scale output of ±1 V at the load, so the overall multiplier transfer function is

$$W = (X1 - X2)(Y1 - Y2)$$

where the X1, X2, Y1, Y2 inputs and W output are in volts. The polarity of the output can be reversed simply by reversing either the X or Y input.

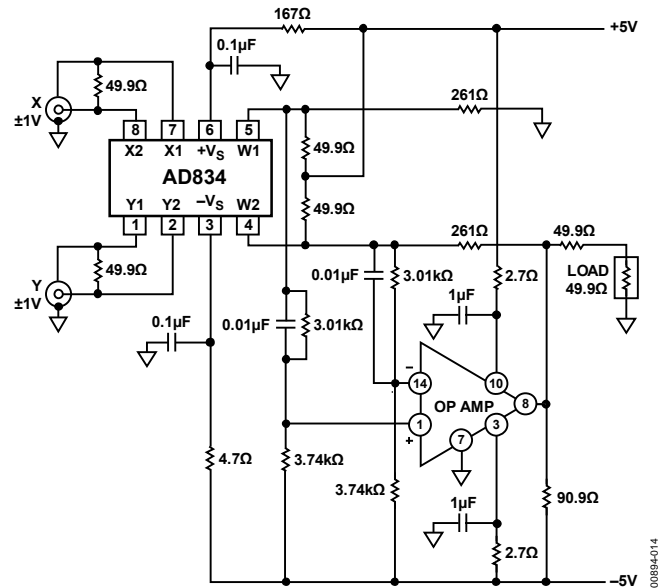


Figure 18. Sideband DC-Coupled Multiplier

Choose the op amp to support the desired output bandwidth. The op amp originally used in Figure 18 was the AD5539, providing an overall system bandwidth of 100 MHz. The AD8009 should provide similar performance. Many other choices are possible where lower post multiplication bandwidths are acceptable. The level shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset can be nulled by including a 100 Ω trim pot between each of the lower pair of resistors (3.74 kΩ) and the negative supply. The pulse response for this circuit is shown in Figure 19; the X input is a pulse of 0 V to 1 V and the Y input is 1 V dc. The transition times at the output are about 4 ns.

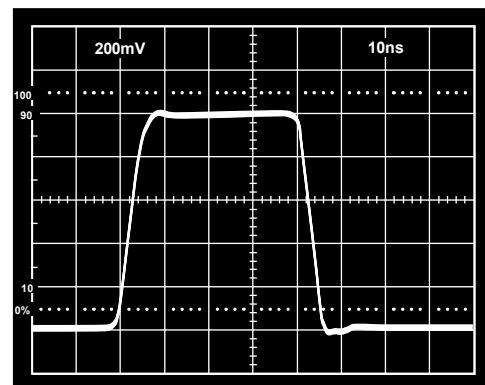


Figure 19. Pulse Response for the Circuit of Figure 18

### POWER MEASUREMENT (MEAN-SQUARE AND RMS)

The AD834 is well-suited to measurement of average power in high frequency applications, connected either as a multiplier for the determination of the  $V \times I$  product, or as a squarer for use with a single input. In these applications, the multiplier is followed by a low-pass filter to extract the long-term average value. Where the bandwidth extends to several hundred megahertz, the first pole of this filter should be formed by grounded capacitors placed directly at the output pins, W1 and W2. This pole can be at a few kilohertz. The effective multiplication or squaring bandwidth is then limited solely by the AD834, because the active circuitry that follows the multiplier is required to process only low frequency signals. Using the device as a squarer, like the circuit shown in Figure 8, the wideband output in response to a sinusoidal stimulus is a raised cosine.

$$\sin^2 \omega t = (1 - \cos 2 \omega t)/2$$

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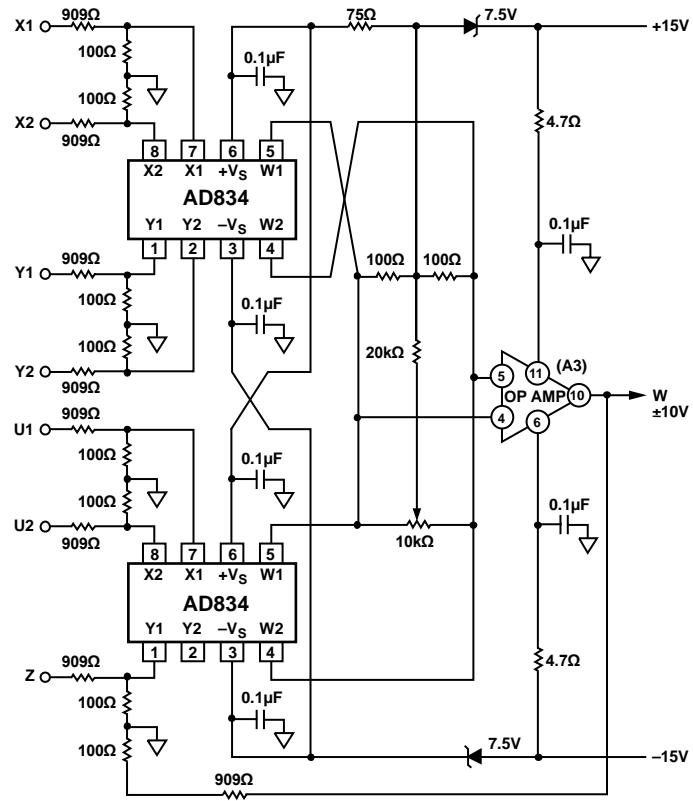
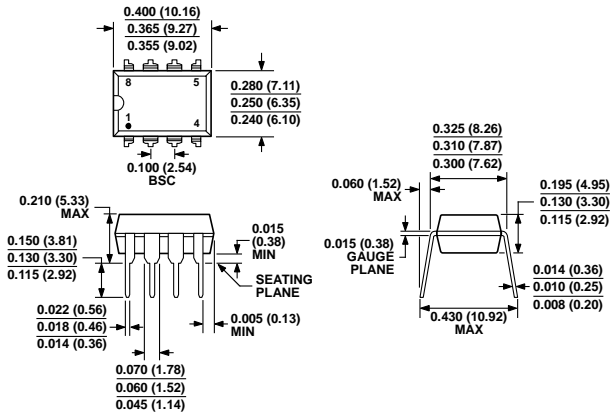


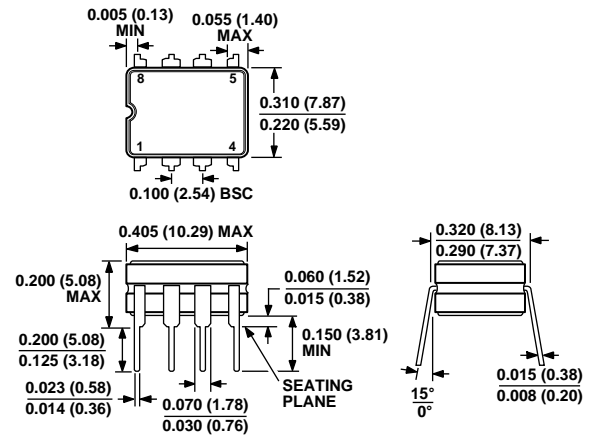
Figure 23. Wideband Three-Signal Multiplier/Divider

OUTLINE DIMENSIONS



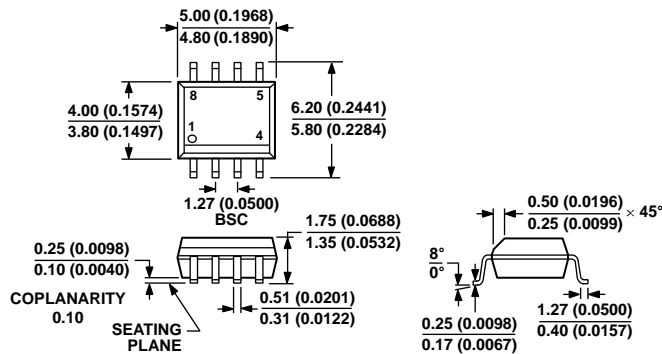
COMPLIANT TO JEDEC STANDARDS MS-001  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 24. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)  
 Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 25. 8-Lead Ceramic Dual In-Line Package [CERDIP] (Q-8)  
 Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 26. 8-Lead Standard Small Outline Package [SOIC\_N] Narrow Body (R-8)  
 Dimensions shown in millimeters and (inches)

**ORDERING GUIDE**

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD834JNZ	0°C to 70°C	8-Lead PDIP	N-8
AD834JRZ	0°C to 70°C	8-Lead SOIC_N	R-8
AD834JRZ-RL	0°C to 70°C	8-Lead SOIC_N	R-8
AD834JRZ-R7	0°C to 70°C	8-Lead SOIC_N	R-8
AD834AR-REEL	-40°C to +85°C	8-Lead SOIC_N	R-8
AD834AR-REEL7	-40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ	-40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ-RL	-40°C to +85°C	8-Lead SOIC_N	R-8
AD834ARZ-R7	-40°C to +85°C	8-Lead SOIC_N	R-8
AD834AQ	-40°C to +85°C	8-Lead Cerdip	Q-8
AD834SQ/883B	-55°C to +125°C	8-Lead Cerdip	Q-8

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**