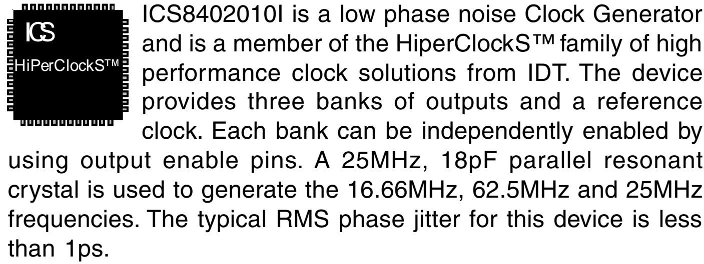
FEMTOCLOCK™ CRYSTAL-TO-LVDS/LVCMOS CLOCK GENERATOR

ICS8402010I

General Description

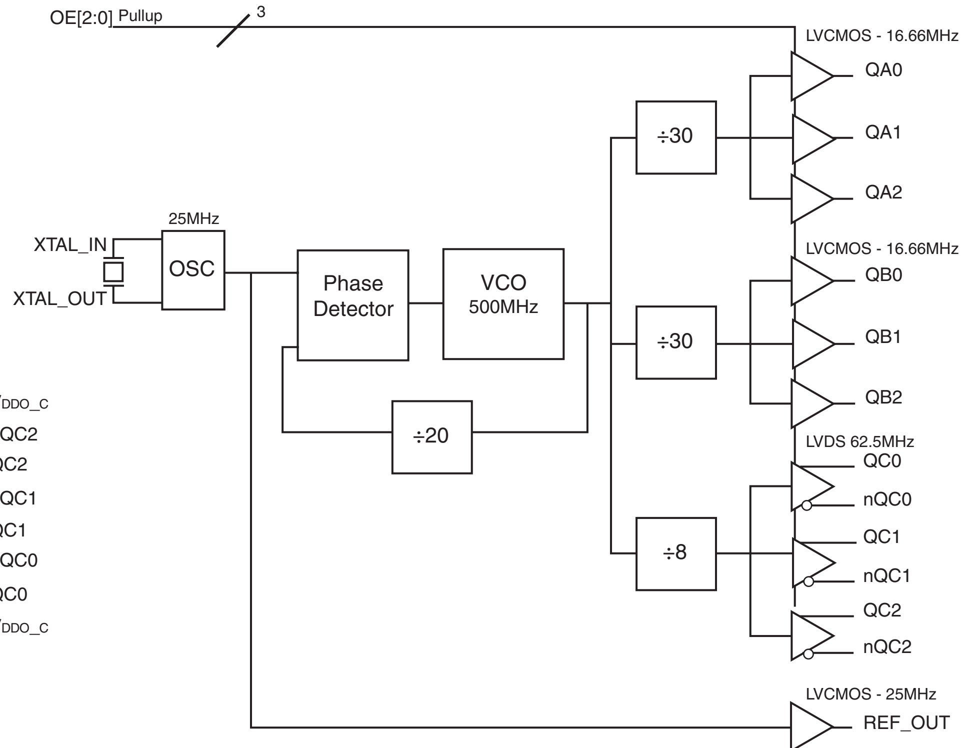


ICS8402010I is a low phase noise Clock Generator and is a member of the HiperClockS™ family of high performance clock solutions from IDT. The device provides three banks of outputs and a reference clock. Each bank can be independently enabled by using output enable pins. A 25MHz, 18pF parallel resonant crystal is used to generate the 16.66MHz, 62.5MHz and 25MHz frequencies. The typical RMS phase jitter for this device is less than 1ps.

Features

- Three banks of outputs:
  Bank A/B: three single-ended LVCMOS outputs at 16.66MHz
  Bank C: three differential LVDS outputs at 62.5MHz
  One single-ended reference clock output at 25MHz
- Crystal input frequency: 25MHz
- Maximum output frequency: 62.5MHz
- RMS phase jitter @ 62.5MHz, using a 25MHz crystal, Integration Range (1.875MHz - 20MHz): 0.375ps (typical)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS6) packages

Block Diagram



Pin Assignment

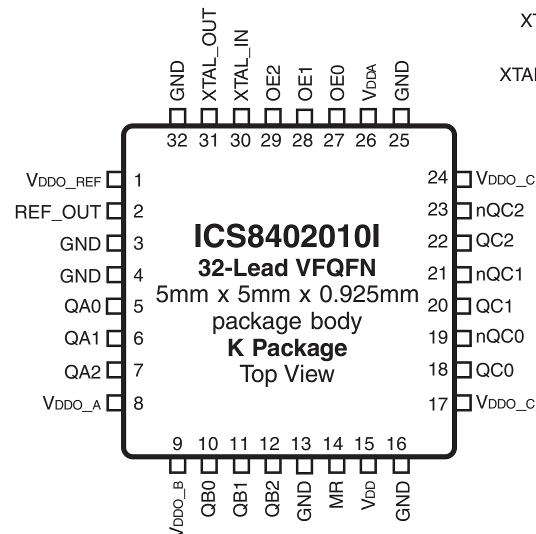


Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDO_REF}	Power		Output power supply pin for REF_OUT output.
2	REF_OUT	Output		Single-ended reference clock output. LVCMOS/LVTTL interface levels.
3, 4, 13, 16, 25, 32	GND	Power		Power supply ground.
5, 6, 7	QA0, QA1, QA2	Output		Single-ended Bank A clock outputs. LVCMOS/LVTTL interface levels.
8	V_{DDO_A}	Power		Output power supply pin for Bank A LVCMOS outputs.
9	V_{DDO_B}	Power		Output power supply pin for Bank B LVCMOS outputs.
10, 11, 12	QB0, QB1, QB2	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels.
14	MR	Input	Pulldown	Master reset, resets the internal dividers. During reset, LVCMOS outputs are pulled LOW and LVDS outputs are pulled LOW and HIGH, (QCx pulled LOW, nQCx pulled HIGH). LVCMOS/LVTTL interface levels.
15	V_{DD}	Power		Core supply pin.
17, 24	V_{DDO_C}	Power		Output power supply pin for Bank C LVDS outputs.
18, 19	QC0, nQC0	Output		Differential Bank C clock outputs. LVDS interface levels.
20, 21	QC1, nQC1	Output		Differential Bank C clock outputs. LVDS interface levels.
22, 23	QC2, nQC2	Output		Differential Bank C clock outputs. LVDS interface levels.
26	V_{DDA}	Power		Analog supply pin.
27, 28, 29	OE0, OE1, OE2	Input	Pullup	Output enable pins. See Table 3. LVCMOS/LVTTL interface levels.
30, 31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance (per output)	QA[0:2], QB[0:2], REF_OUT	V_{DD}, $V_{DDO_A} = V_{DDO_B} = V_{DDO_REF} = 3.465V$		15		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QA[0:2], QB[0:2], REF_OUT			20		Ω

Table 3. OE Function Table

Inputs			
OE2	OE1	OE0	Output States
X	X	0	QA0, QB0, QC0 disabled
X	X	1	QA0, QB0, QC0 enabled
X	0	X	QA1, QB1, QC1 disabled
X	1	X	QA1, QB1, QC1 enabled
0	X	X	QA2, QB2, QC2 disabled
1	X	X	QA2, QB2, QC2 enabled

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to $V_{DDO_A, _B}$ + 0.5V
Outputs, I_O (LVDS, V_{DDO_C})	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} Junction-to-Ambient	37.0°C/W (0 mps)
Package Thermal Impedance, θ_{JB} Junction-to-Board	0.5°C/W
Package Thermal Impedance, θ_{JC} Junction-to-Case	29.6°C/W

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_REF} = V_{DDO_C}$ = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.15	3.3	V_{DD}	V
V_{DDO_A}, V_{DDO_B}, V_{DDO_C}, V_{DDO_REF}	Output Supply Voltage		3.135	3.3V	3.465	V
I_{DD}	Power Supply Current				25	mA
I_{DDA}	Analog Supply Current				15	mA
$I_{DDO_A} + I_{DDO_B} + I_{DDO_C} + I_{DDO_REF}$	Output Supply Current				30	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_REF}$ = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	OE0, OE1, OE2	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		MR	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	OE0, OE1, OE2	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		MR	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{OH}	Output High Voltage; NOTE 1	REF_OUT, QA[0:2], QB[0:2]	V_{DDO_X} = 3.465V	2.6			V
V_{OL}	Output Low Voltage; NOTE 1	REF_OUT, QA[0:2], QB[0:2]	V_{DDO_X} = 3.465V			0.5	V

NOTE: V_{DDO_X} denotes V_{DDO_A}, V_{DDO_B} and V_{DDO_REF}.

NOTE 1: Outputs terminated with 50Ω to $V_{DDO_A, _B, _REF}/2$. See Parameter Measurement Information, Output Load Test Circuit diagram.

TABLE 3C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO_C}$ = 3.3V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	450	550	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.325	1.450	1.575	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

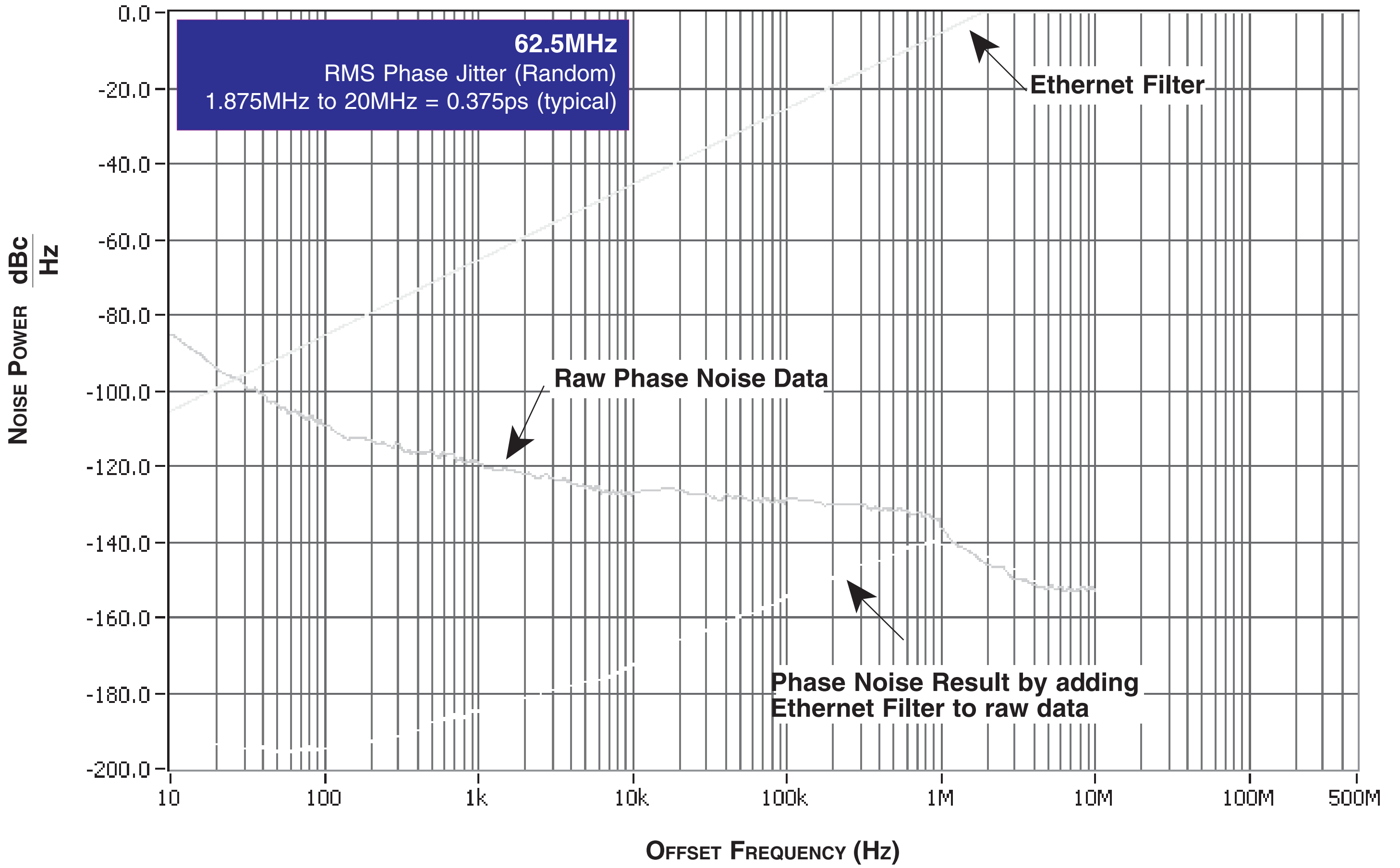
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDO_A} = V_{DDO_B} = V_{DDO_REF} = V_{DDO_C}$ = 3.3V ± 5%, TA = -40°C TO 85°C

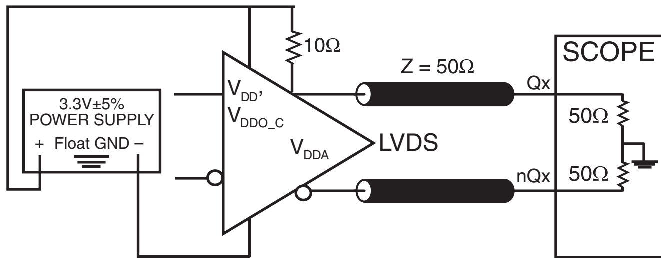
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QC[0:2]/ nQC[0:2]			62.5		MHz
		REF_OUT			25		MHz
		QA[0:2], QB[0:2]			16.66		MHz
*t*sk(o)	Output Skew; NOTE 1, 2	QA[0:2], QB[0:2]				125	ps
*t*sk(b)	Bank Skew; NOTE 2, 3	QC[0:2]/ nQC[0:2]				60	ps
		QA[0:2]				100	ps
		QB[0:2]				125	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 4	QC[0:2]/ nQC[0:2]	62.5MHz, Integration Range: 1.875MHz – 20MHz		0.375		ps
t_R / t_F	Output Rise/Fall Time	QC[0:2]/ nQC[0:2]	20% to 80%	165		450	ps
		QA[0:2], QB[0:2]	20% to 80%	450		1000	ps
odc	Output Duty Cycle	QC[0:2]/ nQC[0:2]		47		53	%
		QA[0:2], QB[0:2]		45		55	%

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO_X}/2$.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.
NOTE 4: Please refer to the Phase Noise Plot.

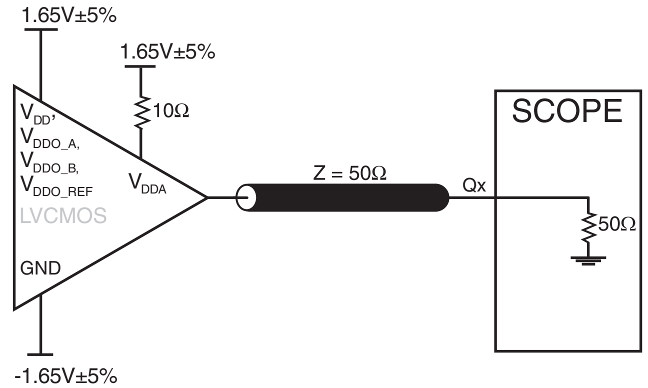
Typical Phase Noise at 62.5MHz (LVDS)



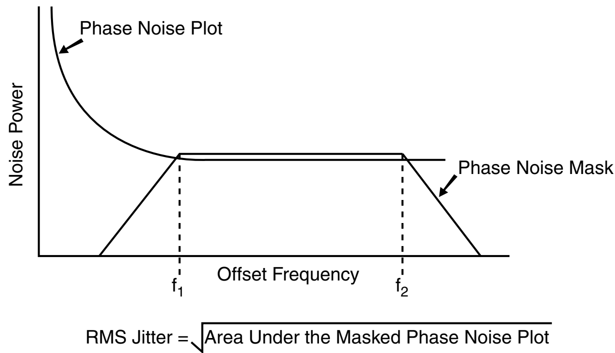
Parameter Measurement Information



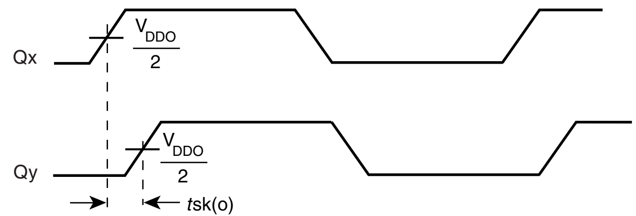
3.3V LVDS Output Load AC Test Circuit



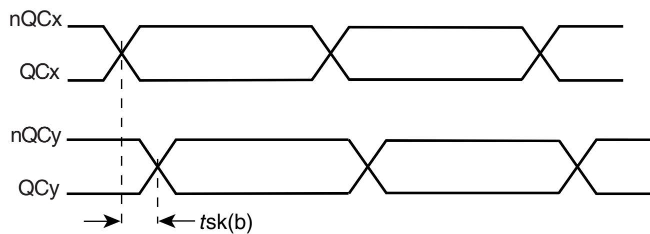
3.3V LVCMOS Output Load AC Test Circuit



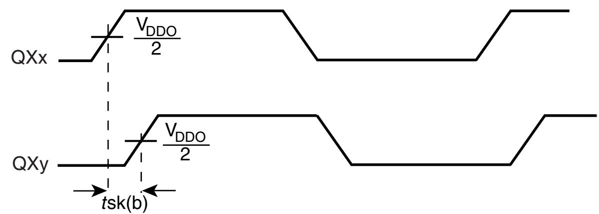
RMS Phase Jitter



LVCMOS Output Skew

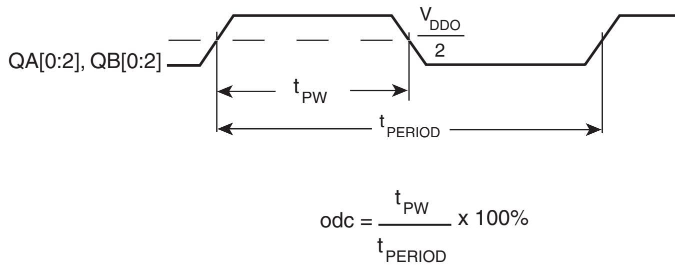


LVDS Bank Skew

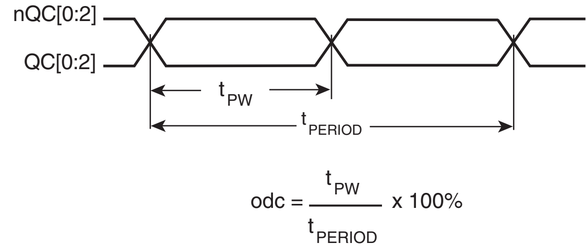


LVCMOS Bank Skew

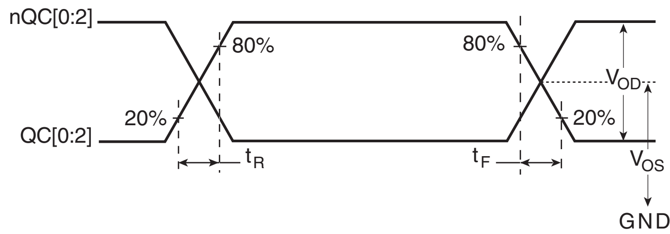
PARAMETER MEASUREMENT INFORMATION, CONTINUED



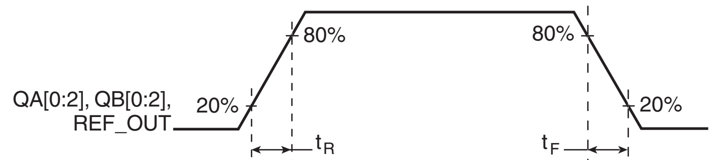
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



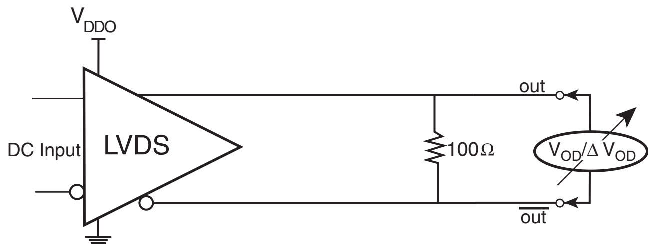
LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



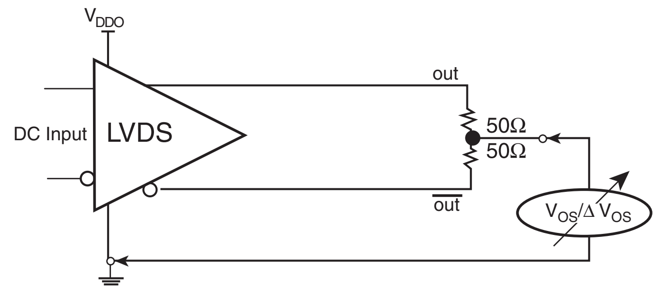
LVDS OUTPUT RISE/FALL TIME



LVCMOS OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8402010I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO_X} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

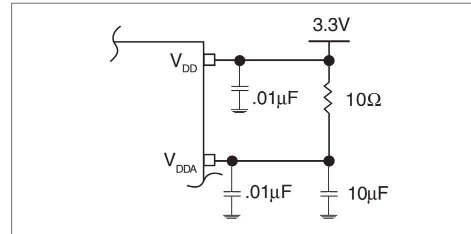


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

Control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

LVDS Outputs

All unused LVDS outputs should be terminated with 100Ω resistor between the differential pair.

Crystal Input Interface

The ICS8402010I has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

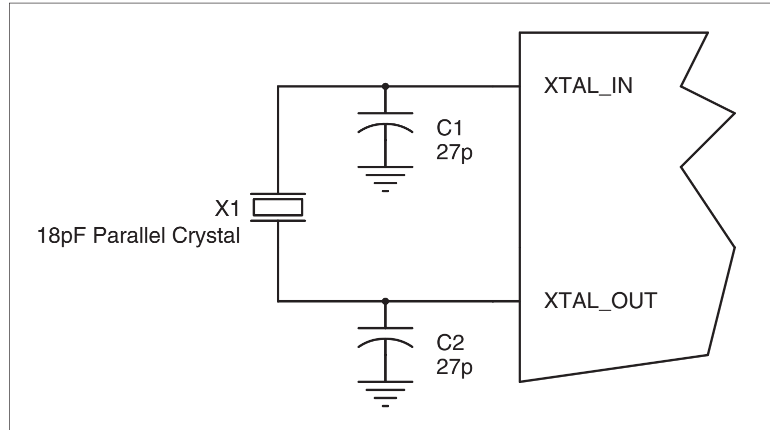


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

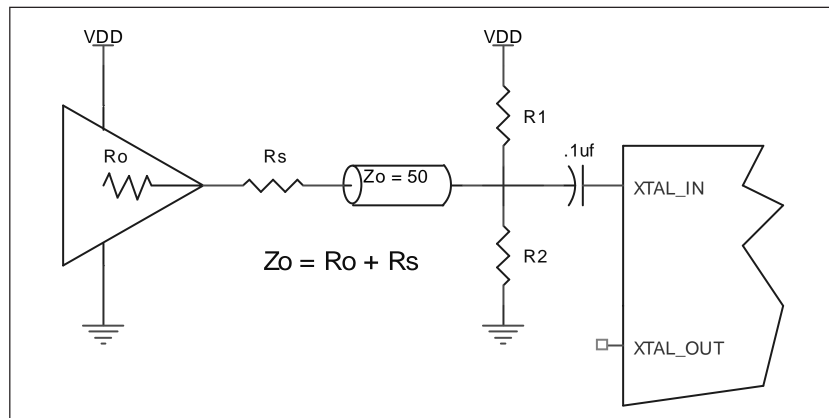


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

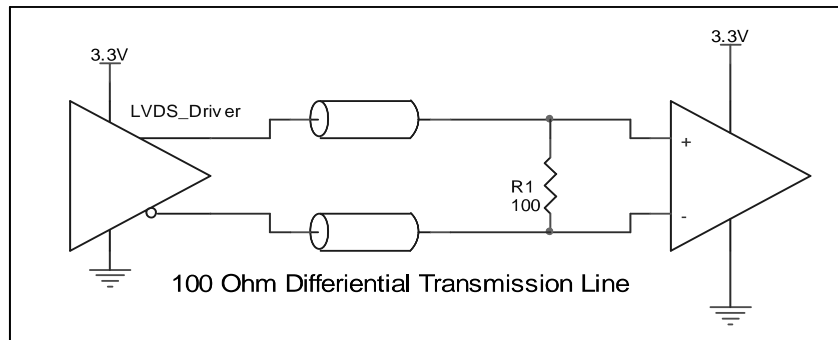


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

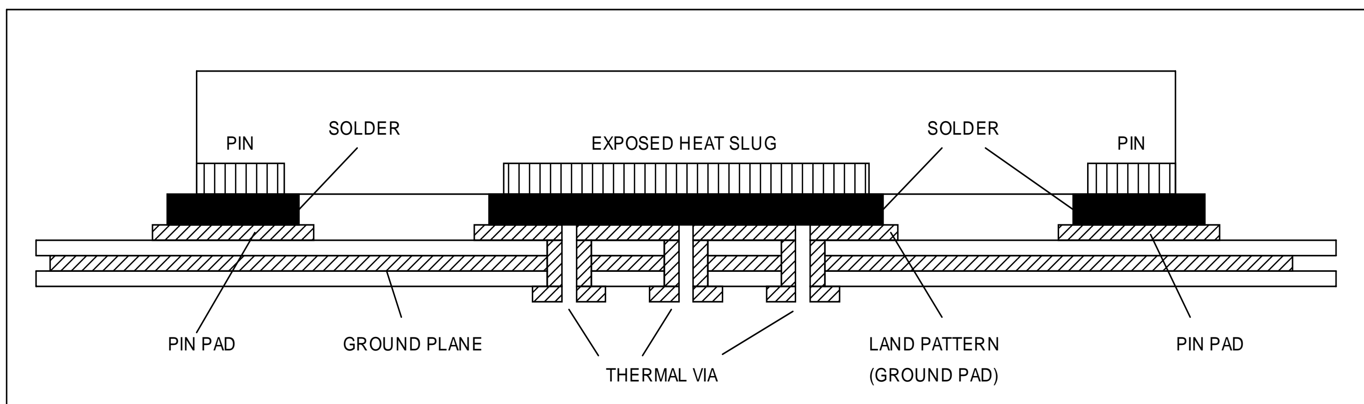


Figure 5. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8402010I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8402010I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and Output Power Dissipation

- Power (core, output) = V_{DD_MAX} * (I_{DD} + I_{DDO_X} + I_{DDA}) = 3.465V * (25mA + 30mA + 15mA) = **242.6mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDO}/2$

  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 20Ω)] = **24.7mA**

- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 20Ω * $(24.7mA)^2$ = **12.25mW per output**

- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 12.25mW * 6 = **73.5mW**

Total Power Dissipation

- **Total Power**
  = Power (core, output) + Power Dissipation (R_{OUT})
  = 242.6mW + 73.5mW
  = 316.1mW

2. *Junction Temperature.*

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.316W * 37°C/W = 96.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board.

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Reliability Information

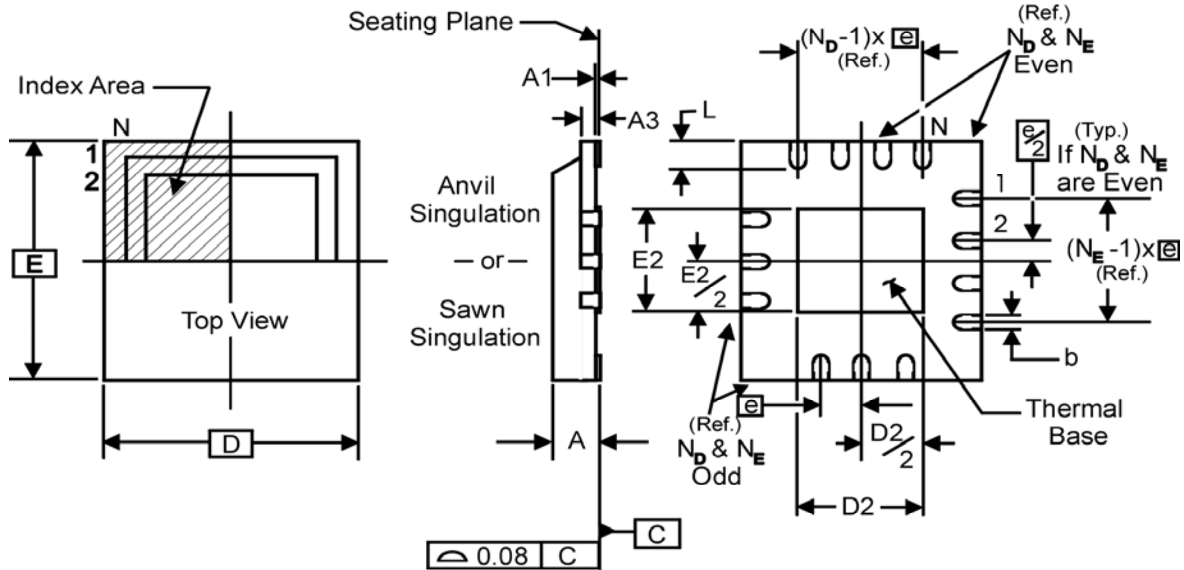
Table 7. θ_{JA} vs. Air Flow Table for 32 Lead VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

Transistor Count

The transistor count for ICS8402010I is: 7782

Package Outline - K Suffix for 32 Lead VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

Table 7. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	**Minimum**	**Maximum**
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8402010AKI	ICS402010AI	32 Lead VFQFN	Tray	-40°C to 85°C
8402010AKIT	ICS402010AI	32 Lead VFQFN	1000 Tape & Reel	-40°C to 85°C
8402010AKILF	ICS02010AIL	32 Lead "Lead-Free" VFQFN	Tray	-40°C to 85°C
8402010AKILFT	ICS02010AIL	32 Lead "Lead-Free" VFQFN	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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