10-Quad RapidIO® Switch

Datasheet 80KSW0005

1 Device Overview

The CPS-10Q (80KSW0005) is a serial RapidIO switch whose functionality is central to routing packets for distribution among DSPs, processors, FPGAs, other switches, or any other sRIO-based devices. The CPS-10Q supports serial RapidIO packet switching (unicast, multicast, and an optional broadcast) from any of its 16 input ports to any of its 16 output ports.

2 Features

- Interfaces - sRIO
  - *40 bidirectional serial RapidIO (sRIO) lanes v 1.3*
  - *Port Speeds selectable: 3.125Gbps, 2.5Gbps, or 1.25Gbps*
  - *All lanes support short haul or long haul reach for each PHY speed*
  - *Configurable port count to up to 16 ports*
  - *Two enhanced quads can be configured as 4 1x ports or 1 4x ports*
  - *Supports standard 4 levels of priority*
  - *Error handling support: It allows error detection, logging and response from all major functional blocks on the device.*
- Interfaces - I^2C
  - *Provides I^2C port for maintenance and error reporting*
  - *Master or Slave Operation*
  - *Master allows power-on configuration from external ROM*
  - *Master mode configuration with external image compressing and checksum*
- Performance
  - *100 Gbps of peak switching bandwidth*
  - *Non-blocking data flow architecture within each sRIO priority*
  - *low latency for all packet length and load condition*
  - *Internal queuing buffer and retransmit buffer*
  - *Standard receiver based physical layer flow control*
- Features
  - *Configurable for cut-thru and store-and-forward modes*
  - *Device configurable through any of sRIO ports, I^2C, or JTAG*
  - *Packet Trace function: It allows copying or filtering packets on a per-port basis. Each port provides the ability to match the first 160 bits of any packet against up to 4 programmable comparison values to copy the packet to a programmable output trace port or drop it.*
  - *Supports up to 40 simultaneous multicast masks per each port*
  - *Support Broadcast*
  - *Port Loopback Debug Feature*
  - *Software assisted error recovery, supporting hot swap*
  - *Ports may be individually turned off to reduce power*
  - *PMON counters for monitor and diagnostics per port*
  - *Serdes physical diagnostic registers*
  - *Embedded PRBS generation and detection with programmable polynomial cover error rate under all conditions*
  - *0.13um technology*
  - *Low power dissipation*
  - *Full JTAG Boundary Scan support (IEEE1149.1 & 1149.6)*
  - Package: FCBGA 676-ball grid array, 27mm x 27mm, 1.0mm ball pitch

3 Block Diagram

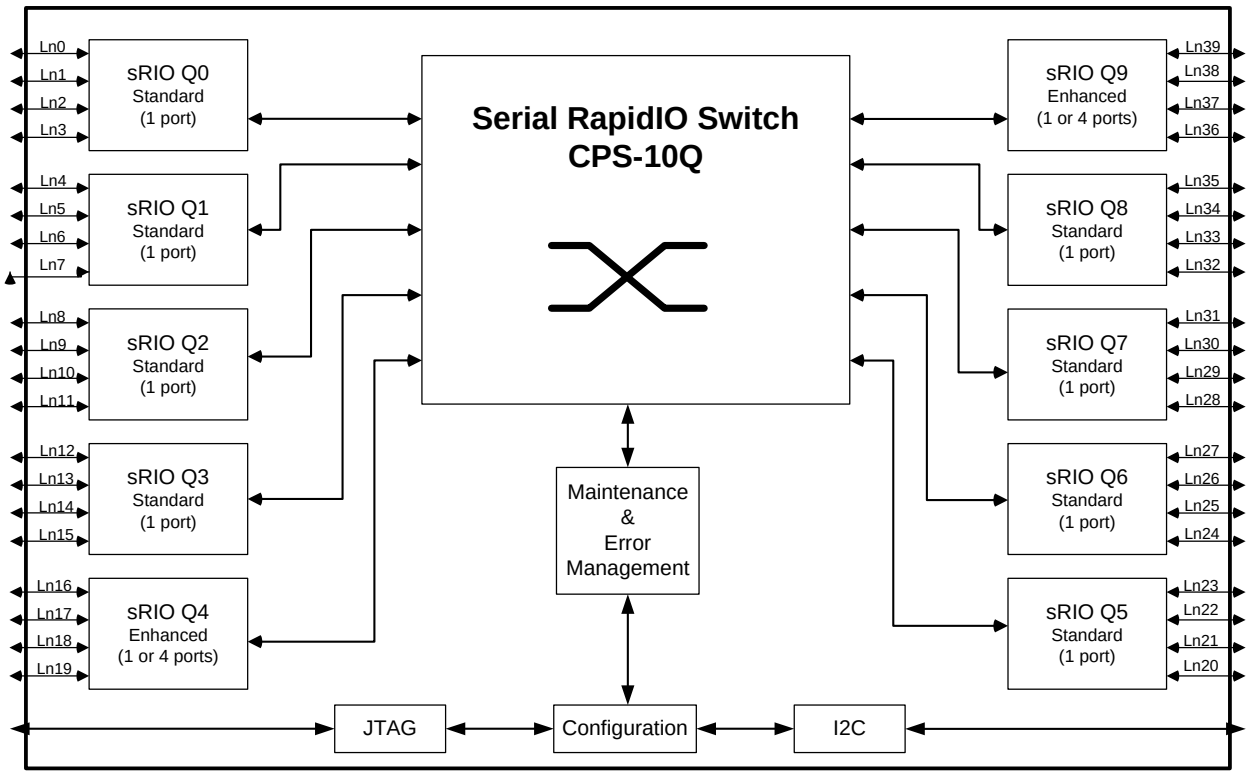

Figure 1 Block diagram

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5 Applications

Central switch baseband system wireless processing

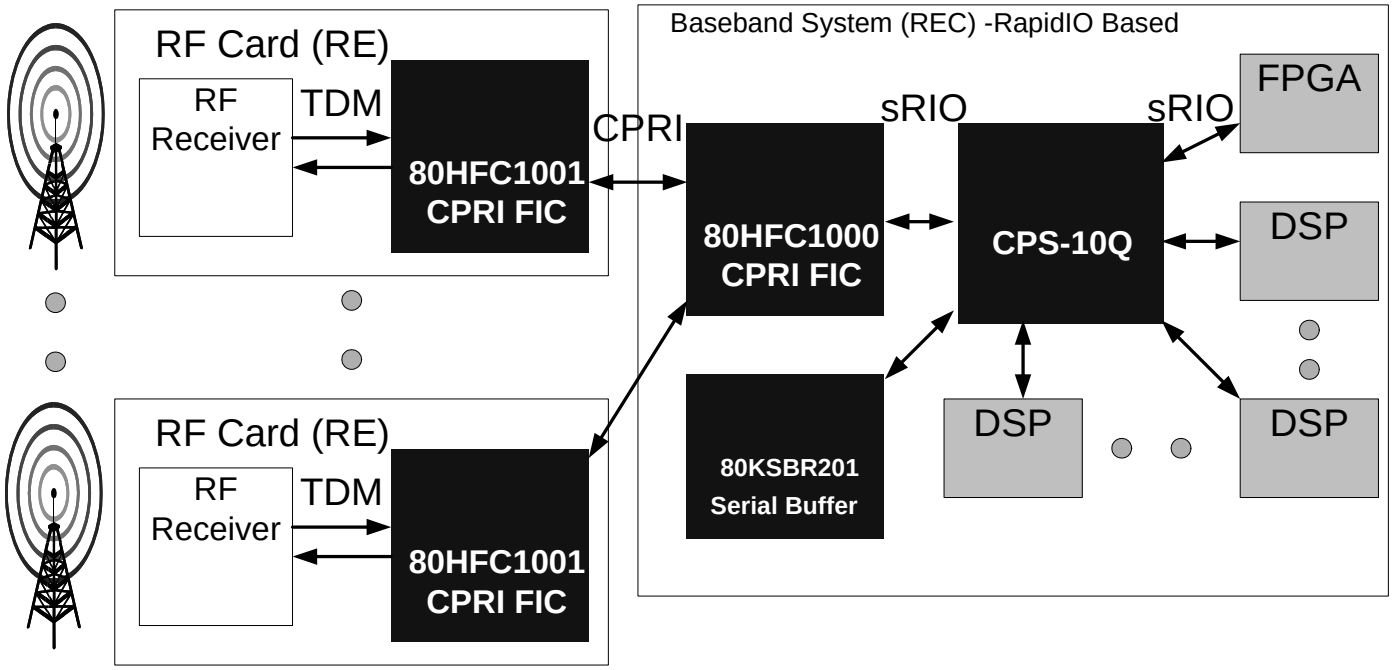

Figure 1 Application Overview

Note: The CPS-10Q provides direct support for backplane connections using the serial RapidIO standard. The addition of an appropriate bridge (e.g., CPRI sRIO) allows for further backplane flexibility, accommodating designs based on a wide range of standards such as CPRI, OBSAI, GbE or PCIe.

In a macro wireless station, a switch-based raw data combination and distribution architecture is widely adopted. Switch based architecture provides high flexibility and high resource efficiency. The raw data from the Radio Unit is distributed to one or more processing cards by unicast or multicast. Aggregating raw data from processing cards to a buffer-less chain can be done by a fast non-blocking switch.

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Media Gateway and general processing

Figure 2 Application Overview

Note: The CPS-10Q provides direct support for backplane connections using the serial RapidIO standard.

A low jitter switch enables fully DSP processing power. Priority support, fast switching, and multicasting will differentiate class of traffic to provide QoS.

6 Functional Overview

The CPS-10Q is optimized for either board-level DSP/ASIC cluster applications or module-level distributed processing application. Up to 16 serial RapidIO ports fully meet standard v1.3. The physical lanes may be configured to operate at 3.125Gbps, 2.5Gbps or 1.25Gbps. All lanes independently work in short haul or long haul. The switch has a sustained 80Gbps bandwidth. It is non-blocking within a given sRIO priority.

The CPS-10Q can be programmed through a CPU or a DSP connected to one of the sRIO ports of the device or with a CPU connected to an I^2C or JTAG bus, it can also work along with a I^2C configuration memory. This option allows the device work in “remote stand alone” mode.

Each sRIO port provides a packet trace capability. For any packet received by a port, a comparison between the first 160 bits and up to four configurable values can be performed. A match against any of these parameters will result in a copy of the packet and a route of the packet to a configurable ouput port. This feature can be used as a tactical function to track user data or in a debug environment to test how specific packets are moving through the platform.

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7 Interfaces Overview

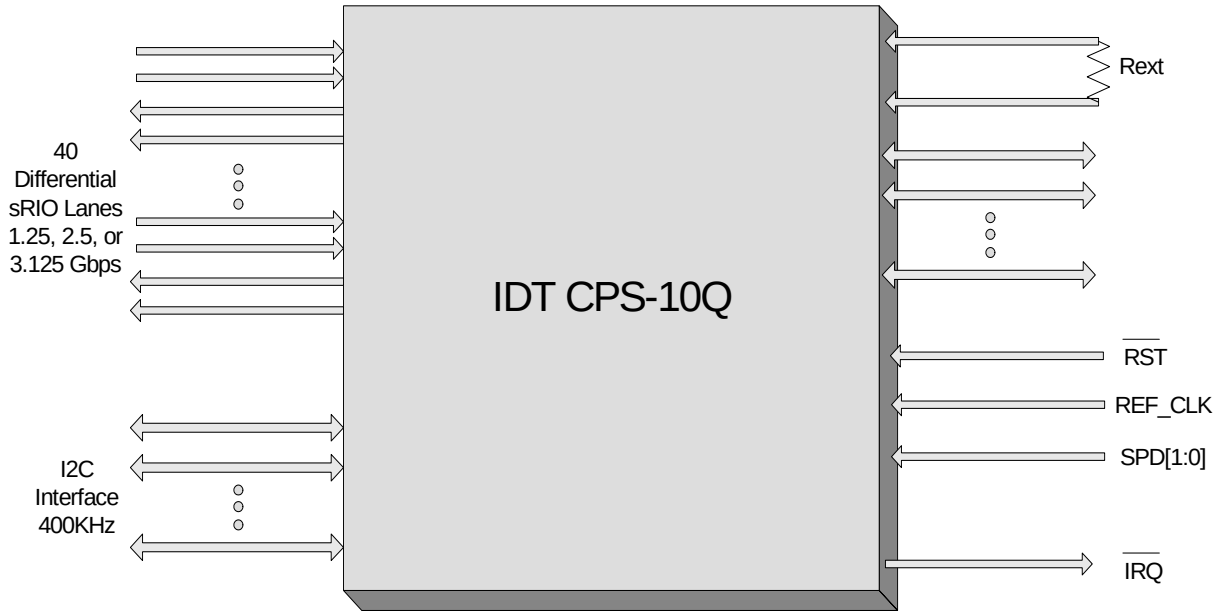

Figure 3 Interface Diagram

sRIO Ports

The sRIO interfaces are the main communication ports on the switch. These ports are compliant with the serial RapidIO v. 1.3 specifications. Please refer to the serial RapidIO specifications for full detail [2-10].

The CPS-10Q provides 40 differential dual simplex transceivers dedicated to sRIO I/O. In addition to standard quads that act as a single 1x or 4x port, two enhanced quads can be independently configured to run in various configurations as 4 1x-ports or 1 4x-ports. The device supports a maximum of 16 1x-ports, or 10 4x-ports. Each port can be programmed to run independently at 1.25, 2.5, or 3.125Gbps. Each lane is able to handle long- or short-haul serial transmission per RIO serial spec.

In the CPS-10Q there are 8 “Standard Quads” which follow the standard sRIO physical interface implementation. These ports either operate in 4x-mode or as a single 1x-port. For example Lanes 0 - 3 are programmable into one 4x- or one 1x-port. Per sRIO standard, either the 1st or 3rd lanes in a given 4x group may be used as a valid link for a 1x port. For example, either lane 0 or lane 2 may be connected in support of a 1x-port.

The CPS-10Q also has a proprietary implementation which we refer to as an “Enhanced Quad” for Quad4 and Quad9. An Enhanced Quad can be operated in standard sRIO mode like the standard quads. Additionally the Enhanced Quad can be register-configured to run as 4 independent 1x-ports. In this manner, the user has the flexibility to use one, multiple, or two lanes in 1x-mode. For example, lanes 16 - 19 of the CPS-10Q are programmable into one 4x- or four 1x-ports. This is unlike the standard sRIO port implementation that, when configured as a 1x-port, renders the remaining possible connections unused.

I^2C Bus

This interface may be used as an alternative to the standard sRIO or JTAG ports to program the switch and to check the status of registers - including the error reporting registers. It is fully compliant with the I^2C specification, it supports master mode and slave mode, also supports both Fast- and Slow-mode buses [1]. Refer to the “I^2C” section for full detail.

JTAG TAP Port

This TAP interface is IEEE1149.1 (JTAG) and 1149.6 (AC Extest) compliant [10, 11]. It may also be used as an alternative to the standard sRIO or I^2C ports to program the switch and to check the status of registers - including the error reporting registers. It has 5 pins. Refer to the JTAG chapter for full detail.

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Interrupt ($\overline{IRQ}$)

An interrupt output is provided in support of Error Management functionality. This output may be used to flag a host processor in the event of error conditions within the device. Refer to the Error Handling chapter for full detail.

Reset

A single Reset pin is used for full reset of the CPS-10Q, including setting all registers to power-up defaults. Refer to the Reset & Initialization chapter for full detail.

Clock

The single system clock (REF_CLK+ / -) is a 156.25MHz differential clock.

Rext (Rextn & Rextp)

These pins are used to establish the drive bias on the SerDes output. An external bias resistor is required. The two pins must be connected to one another with a 12k Ohm resistor. This provides CML driver stability across process and temperature.

SPD[1:0]

Speed Select Pins. These pins define the sRIO port speed at RESET for all ports. The RESET setting may be overridden by subsequent programming of the QUAD_CTRL register. SPD[1:0] = {00 = 1.25G, 01 = 2.5G, 10 = 3.125G, 11 = RESERVED}. These pins must remain STATICALLY BIASED after power-up.

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8 Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Unit
V_{TERM} ($V_{DD}3$)	$V_{DD}3$ Terminal Voltage with Respect to GND	-0.5 to 3.6	V
V_{TERM}(2) ($V_{DD}3$-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GND	-0.3 to $V_{DD}3$+0.3	V
V_{TERM} (V_{DD})	V_{DD} Terminal Voltage with Respect to GND	-0.5 to 1.5	V
V_{TERM}(2) (V_{DD}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GND	-0.3 to V_{DD}+0.3	V
V_{TERM} (V_{DDS})	V_{DDS} Terminal Voltage with Respect to GND	-0.5 to 1.5	V
V_{TERM}(2) (V_{DDS}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GNDS	-0.3 to V_{DDS}+0.3	V
V_{TERM} (V_{DDA})	V_{DDA} Terminal Voltage with Respect to GND	-0.5 to 1.5	V
V_{TERM}(2) (V_{DDA}-supplied interfaces)	Input or I/O Terminal Voltage with Respect to GNDS	-0.3 to V_{DDA}+0.3	V
T_{BIAS}(3)	Temperature Under Bias	-55 to +125	C
T_{STG}	Storage Temperature	-65 to +150	C
T_{JN}	Junction Temperature	+125	C
I_{OUT} (For $V_{DD}3$ = 3.3V)	DC Output Current	30	mA
I_{OUT} (For $V_{DD}3$ = 2.5V)	DC Output Current	30	mA

Table 1 Absolute Maximum Ratings

Notes:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp up.
3. Ambient Temperature under DC Bias. No AC Conditions.

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9 Recommended Temperature and Operating Voltage(1)

Grade	Ambient Temperature	Ground(2)	Supply Voltage(4)
Commercial	0°C to 70°C	GND = 0V GNDS = 0V	V_{DD} = 1.2 +/- 5% V_{DDS} = 1.2 +/- 5% $V_{DD}3$(3) = 3.3 +/- 5% or 2.5V +/- 100mV V_{DDA} = 1.2 +/- 5%
Industrial	-40°C to 85°C	GND = 0V GNDS = 0V	V_{DD} = 1.2 +/- 5% V_{DDS} = 1.2 +/- 5% $V_{DD}3$(3) = 3.3 +/- 5% or 2.5V +/- 100mV V_{DDA} = 1.2 +/- 5%

Table 2 Recommended Temperature and Operating Voltage

Notes:

1. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed its corresponding supply voltage during power supply ramp up. The device is not sensitive to supply rise and fall times, and thus these are not specified.
2. VDD3, VDDA, and VDDS share a common ground (GNDS). Core supply and ground are VDD and GND respectively.
3. VDD3 may be operated at either 3.3V or 2.5V simply by providing that supply voltage. For those interfaces operating on this supply, this datasheet provides input and output specifications at each of these voltages.
4. VDDS & VDDA may be tied to a common power plane. VDD (core, digital supply) should have its own supply and plane. A ferrite bead may be used to supply VDDS/ VDDA from VDD. The bead should be chosen to provide a low DC resistance in order to maintain the rail voltage spec. To keep within the specified low VDDA / VDDS limit, a 0.06 Ohm (DC) resistance is the max allowable. A bead with 10 Ohm impedance provides sufficient AC block while still meeting DC resistance requirements.

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10 AC Test Conditions

Input Pulse Levels	GND to 3.0V / GND to 2.4V
Input Rise / Fall Times	2ns
Input Timing Reference Levels	1.5V / 1.25V
Output Reference Levels	1.5V / 1.25V
Output Load	Figures 4

Table 3 AC Test Conditions (V_{DD3}=3.3V / 2.5V): JTAG, I^2C, RST

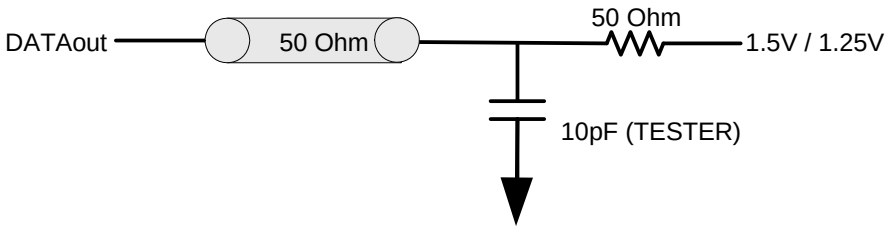

Figure 4 AC Output Test Load (JTAG)

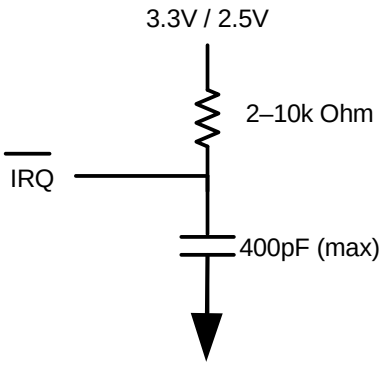

Figure 5 AC Output Test Load ($\overline{IRQ}$)

Note: The $\overline{IRQ}$ pin is an open-drain driver. IDT recommends a weak pull-up resistor (2-10k Ohm) be placed on this pin to V_{DD3}.

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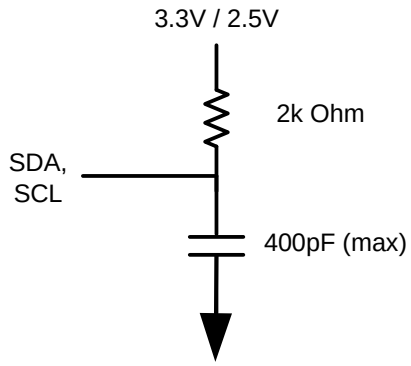

Figure 6 AC Output Test Load (I^2C)

Note: The SDA and SCL pins are open-drain drivers. Refer to the Philips I^2C specification [1] for appropriate selection of pull-up resistors for each.

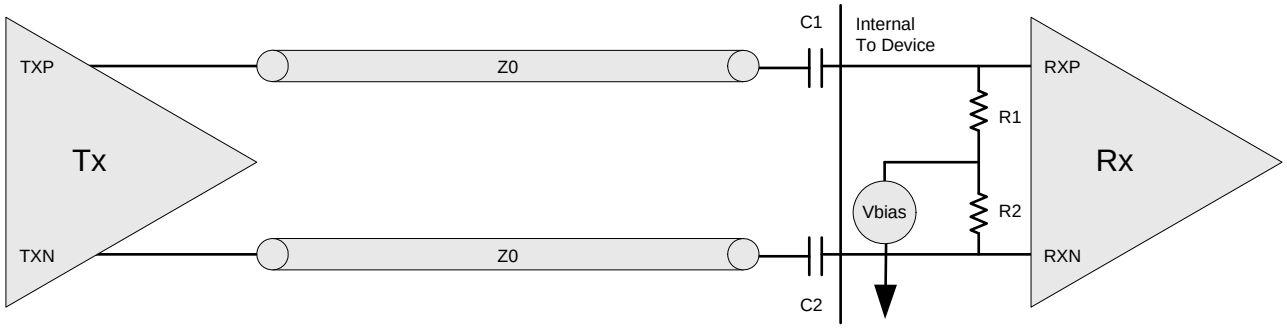

Figure 7 sRIO Lanes Test Load

The characteristic impedance Z0 should be designed for 100 Ohms. An inline capacitor C1 and C2 at each input of the receiver provides AC-coupling and a DC-block. The IDT recommended and test value is 100nF for each. Thus, any DC bias differential between the two devices on the link is negated. The differential input resistance at the receiver is designed to be 100 Ohms (per sRIO specification). Thus, R1 and R2 are 50 Ohms each. Note that V_{BIAS} is the internal bias voltage of the device's receiver.

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11 Device Performance Figures

11.1 Performance Figures

The following table lists the CPS-10Q's performance figures. Figures provided here are guaranteed by design and characterization, but are not production tested.

Description	Min	Typ	Max	Units	Comments
Throughput (Peak)	—	—	100	Gbps	
Throughput (Sustained)	—	80	—	Gbps	Value shown is for device configured for 10 4X ports, each running at 3.125Gbps, 276 byte packets at priority 0. Please contact IDT technical support for figures related to a specific usage case and traffic conditions.
Per Port throughput (Peak)	—	—	10	Gbps	Value shown is for device configured for each port with 4X 3.125G mode. The sustained throughput is shown in other table below.
Switch Latency Jitter (70% switch load)(2)	—	60	—-	ns	Latency Jitter for the switch lock is the sum of the Physical layer jitter plus one maintenance packet of contention delay for a given output port. Worst case for the physical layer is the jitter caused by the port sync process. This requires 6 32-bit control symbols plus 2 cycle times the port rate. The figures shown here are for priority 2 packets under 70% switch loading with an even mix of packets of each priority. It assumes that no maintenance packets contend on the output port.
Soft Reset to Receipt of Valid Packets	—	—	26	us	This includes reset time as well as link establishment.
Hard Reset to Receipt of Valid Packets	—	—	26	us	This includes reset time as well as link establishment.
Multicast Map Update Delay	25	—	2000	cycles(3)	

Table 4 80KSW0005 Performance Figures

Notes:

1. Values are guaranteed by characterization, but are not production tested.
2. For those specifications associated with an sRIO transaction, it should be noted that the upper limit to a specification may be dictated by sRIO priority handling. For example, a maintenance read packet having lower priority may be held off until higher priority packets in queue are serviced. The user should take into consideration this additional priority-induced delay when examining these specifications. I^2C and JTAG configuration register access transactions are always deterministic and follow these specifications identically.
3. "Cycles" refer to internal core clock cycles which are two times the external reference clock (REF_CLK) frequency = 312.5 MHz.

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11.2 Sustained Per-Port Throughput (Typical)

Pay Load Size	1.25GHz		2.5GHz		3.125GHz	
	1X	4X	1X	4X	1X	4X
16 Byte	0.70 G	2.33 G	1.38 G	4.42 G	1.93 G	4.67
32 Byte	0.79 G	2.4 G	1.57 G	5.48 G	2.1 G	5.89
64 Byte	0.86 G	2.92 G	1.73 G	6.32 G	2.24 G	7.02 G
128 Byte	0.94 G	3.38 G	1.87 G	6.76 G	2.28 G	8.19 G
256 Byte	0.97 G	3.66 G	1.93 G	7.30 G	2.39 G	8.93 G

Table 5 Sustained Per-Port Throughput (Typical)

Notes:

1. Values are guaranteed by characterization, but are not production tested.
2. Throughput values are for 8bit destination ID packet, Header + Pay Load + CRC. The (Header + CRC) size changes depending on payload size. For payloads less then 80 Bytes, the (Header + CRC) is 12 bytes. For payloads bigger than 80 Bytes, the (Header + CRC) is 14 bytes.
3. As payload size increases, the physical layer control symbols (sRIO required overhead) become a smaller percentage of the overall per-port throughput figure. The physical layer symbols include one SoP and one EoP for every packet. There is a status control symbol for every 1024 transmitted code-group as well as synchronization sequences required by sRIO. For two way traffic, packet acknowledgment control symbols will occur between the packets.

11.3 Data Packet Latency in “Store-and-Forward” Mode (Typical)

Pay Load Size	**1.25GHz**		**2.5GHz**		**3.125GHz**	
	1X	4X	1X	4X	1X	4X
8 Byte	454 ns	328 ns	271 ns	228 ns	240 ns	211 ns
16 Byte	518 ns	348 ns	304 ns	234 ns	266 ns	216 ns
32 Byte	646 ns	380 ns	367 ns	246 ns	316 ns	227 ns
64 Byte	905 ns	441 ns	493 ns	271 ns	419 ns	253 ns
128 Byte	1449 ns	580 ns	770 ns	336 ns	641 ns	307 ns
256 Byte	2473 ns	833 ns	1282 ns	457 ns	1049 ns	409 ns
Multicast Event Control Symbol	126 ns	115 ns	66 ns	60 ns	55 ns	49 ns

Table 6 Switch Latency Table (Store-and-Forward Mode, Typical)

Notes:

1. Values are guaranteed by characterization, but are not production tested.
2. For those specifications associated with an sRIO transaction, it should be noted that the upper limit to a specification may be dictated by sRIO priority handling. For example, a maintenance read packet having lower priority may be held off until higher priority packets in queue are serviced. The user should take into consideration this additional priority-induced delay when examining these specifications. I2C and JTAG transactions are always deterministic and follow these specifications identically.
3. Switch latency is a statistical function, which typically increases with increased traffic loading on the switch. Values shown in Table 6 are typical for single input port to single output port with matching input and output port rates in “Store-and-Forward” mode, no other switch loading. The switch latency in “Store-and-Forward” packet forward methodology is also a strong function of port rate. For specific values under other specific application usage scenarios and traffic conditions, please contact IDT technical support.

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11.4 Data Packet Latency in "Cut-Through" Mode (Typical)

Pay Load Size	1.25GHz		2.5GHz		3.125GHz	
	1X	4X	1X	4X	1X	4X
8 Byte	369 ns	322 ns	233 ns	217 ns	205 ns	195 ns
16 Byte	366 ns	320 ns	225 ns	217 ns	204 ns	197 ns
32 Byte	354 ns	320 ns	224 ns	218 ns	204 ns	195 ns
64 Byte	351 ns	322 ns	223 ns	220 ns	203 ns	196 ns
128 Byte	351 ns	318 ns	224 ns	218 ns	203 ns	196 ns
256 Byte	351 ns	317 ns	222 ns	216 ns	205 ns	195 ns

Table 7 Switch Latency Table (Cut-Through Mode)

Note:

1. Values shown in Table 7 are typical for single input port to single output port with matching input and output port rates in "Cut-Through" mode, no other switch loading. For specific values under other specific application usage scenarios and traffic conditions, please contact IDT technical support.

In "Store-and-Forward" mode and "Cut-Through" mode when trace and filter are enabled at the same time, only the latency for packets sending to the trace port will increase by the time taken to send 20 bytes into the port (20bytes * 1/[port_speed * 0.8]) The latency for other traffic flow will be unaffected.

11.5 Maintenance Packet Latency (Typical)

	1.25GHz	1.25GHz	2.5GHz	2.5GHz	3.125GHz	3.125GHz
Mode	**1X**	**4X**	**1X**	**4X**	**1X**	**4X**
Store-and-forward	571 ns	460 ns	395 ns	344 ns	352 ns	315 ns
Cut-Through	566 ns	449 ns	386 ns	334 ns	344 ns	315 ns

Table 8 Maintenance Packet (20 words) Latency

Note:

1. Values are guaranteed by characterization, but are not production tested.

11.6 Doorbell packet latency (Typical)

	1.25GHz	1.25GHz	2.5GHz	2.5GHz	3.125GHz	3.125GHz
Mode	**1X**	**4X**	**1X**	**4X**	**1X**	**4X**
Store-and-forward	395 ns	323 ns	246 ns	225 ns	219 ns	208 ns
Cut-Through	378 ns	317 ns	230 ns	221 ns	209 ns	208 ns

Table 9 Doorbell Packet Latency

Note:

1. Values are guaranteed by characterization, but are not production tested.

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12 Power Figures

Typical power draw for the 80KSW0005 is approximately 5.3W total for all ports enabled as 10 4x @ 3.125G under 50% switch load. The following table provides power figures on a per-block basis. An estimate of the device power figure for a given application usage can be determined by using the "CPS-10Q Power Calculator" modeling tool.

Description	Typical	Units	Supply	Comments
Serdes 1x @ 1.25G	66, 33	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
SerDes 1x @ 2.5G	78, 36	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
SerDes 1x @ 3.125G	82, 49	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
Serdes 4x @ 1.25G	149, 226	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
SerDes 4x @ 2.5G	178, 82	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
SerDes 4x @ 3.125G	187, 110	mW	VDDS, VDDA	Analog SerDes power consumption (VDDS and VDDA). This does not include the sRIO quad power consumption.
JTAG Block Enable	100	mW	VDD3	Configuration Register Access only. Max interface speed(10MHz).
I2C Block Enable	86	mW	VDD3	Configuration Register Access only. Max interface speed (400KHz).
Quiescent Power	1700	mW	VDD	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Quiescent Power	86	mW	VDD3	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Quiescent Power	75, 47	mW	VDDS, VDDA	Minimum possible operational power draw. All ports disable, I2C and JTAG signals static.
Reset Power	15	mW	VDD	Peak power during RESET of the device.
Reset Power	32	mW	VDD3	Peak power during RESET of the device.
Reset Power	8, 39	mW	VDDS, VDDA	Peak power during RESET of the device.
Standby Power @1.25G	2000	mW	VDD	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @1.25G	86	mW	VDD3	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @1.25G	1700, 1000	mW	VDDS, VDDA	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @2.5G	2200	mW	VDD	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @2.5G	86	mW	VDD3	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @2.5G	2000, 1000	mW	VDDS, VDDA	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @3.125G	2200	mW	VDD	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @3.125G	86	mW	VDD3	Part powered up, reset, all links up (reset configuration), no traffic
Standby Power @3.125G	2200, 1300	mW	VDDS, VDDA	Part powered up, reset, all links up (reset configuration), no traffic
Peak sustained Power	2500	mW	VDD	All sRIO ports enabled at maximum speed, maximum traffic to the switch.
Peak sustained Power	100	mW	VDD3	All sRIO ports enabled at maximum speed, maximum traffic to the switch.
Peak sustained Power	2300, 1500	mW	VDDS, VDDA	All sRIO ports enabled at maximum speed, maximum traffic to the switch

Table 10 Typical Power Figures

Condition: VDD = 1.2V, VDDS = 1.2V, VDDA = 1.2V, VDD3 = 3.3V @ Room temperature $25^{o}C$

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Worst power draw for the 80KSW0005 is approximately 7W total. The condition is all ports @ 3.125G under 100% switch load at the max driving strength and all trace function are enable.

13 I2C-Bus

The CPS-10Q is compliant with the I2C specification [1]. This specification provides all functional detail and electrical specifications associated with the I2C bus. This includes signaling, addressing, arbitration, AC timing, DC specifications, and other details.

The device supports both master mode and slave mode, it's selected by MM pin.

The I2C bus is comprised of Serial Data (SDA) and Serial Clock (SCL) pins. It can be used to attach a CPU or a configuration memory. The I2C interface supports Fast/Standard (F/S) mode (400/ 100 kHz).

I2C master mode and slave mode

The CPS-10Q devices support both master mode and slave mode. It's selected by MM static configuration pin. Refer to the below for signaling and operation.

I2C Device Address

The device address for the CPS-10Q is fully pin-defined by 10 external pins while in slave mode. This provides full flexibility in defining the slave address to avoid conflicting with other I2C devices on a given bus. The device can be operated as either a 10-bit addressable device or a 7-bit addressable device based on another external pin, address select (ADS). If the ADS pin is tied to VDD, then the CPS-10Q operates as a 10-bit addressable device and the device address will be defined as ID[9:0]. If the ADS pin is tied to GND, then the device operates as a 7-bit addressable device with the device address defined by ID[6:0]. The addressing mode must be established at power-up and remain static throughout operation. Dynamic changes will result in undetermined behavior.

Pin	I2C Address Bit (pin_addr)
ID0	0
ID1	1
ID2	2
ID3	3
ID4	4
ID5	5
ID6	6
ID7	7 (don't care in 7-bit mode)
ID8	8 (don't care in 7-bit mode)
ID9	9 (don't care in 7-bit mode)

Table 11 I2C Static Address Selection Pin Configuration

All of the CPS-10Q's registers are addressable through I2C. These registers are accessed via 22-bit addresses and 32-bit word boundaries though standard reads and writes. These registers may also be accessed through the sRIO and JTAG interfaces.

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Signaling

Communication with the CPS-10Q on the I^2C bus follows these three cases:

1) Suppose a master device wants to send information to the CPS-10Q:
   - Master device addresses CPS-10Q (slave)
   - Master device (master-transmitter), sends data to CPS-10Q (slave- receiver)
   - Master device terminates the transfer

2) If a master device wants to receive information from the CPS-10Q:
   - Master device addresses CPS-10Q (slave)
   - Master device (master-receiver) receives data from CPS-10Q (slave- transmitter)
   - Master device terminates the transfer.

3) If CPS-10Q polls configuration image from external memory
   - CPS-10Q addresses the memory.
   - Memory transmits the data.
   - CPS-10Q gets the data.

All signaling is fully compliant with I^2C. Full detail of signaling can be found in the Philips I^2C specification [1]. Standard signaling and timing waveforms are shown below.

Interfacing to Standard-, Fast-, and Hs-mode Devices

The CPS-10Q supports Fast / Standard (F/S) modes of operation. Per I^2C specification, in mixed speed communication the CPS-10Q supports Hs- and Fast-mode devices at 400 kbit/s, and Standard-mode devices at 100 kbit/s. Please refer to the I^2C specification for detail on speed negotiation on a mixed speed bus.

CPS-10Q-Specific Memory Access (Slave mode)

There is a CPS-10Q-specific I^2C memory access implementation. This implementation is fully I^2C compliant. It requires the memory address to be explicitly specified during writes. This provides directed memory accesses through the I^2C bus. Subsequent reads always begin at the address specified during the last write.

The write procedure requires the 3-Bytes (22-bits) of memory address to be provided following the device address. Thus, the following are required: device address – one or two bytes depending on 10-bit / 7-bit addressing, memory address – 3 bytes yielding 22-bits of memory address, and a 32-bit data payload – 4 byte words. To remain consistent with sRIO standard maintenance packet memory address convention, the I^2C memory address provided must be the 22MSBs. Since I^2C writes to memory apply to double words (32-bits), the 2 LSBs are DON'T CARE as the LSBs correspond to word and byte pointers.

The read procedure has the memory address section of the transfer removed. Thus, to perform a read, the proper access would be to perform a write operation and issue a repeated start after the acknowledge bit following the third byte of memory address. Then, the master would issue a read command selecting the CPS-10Q through the standard device address procedure with the R/W bit high. Note that in 10-bit device address mode (ADS=1), only the two MSBs need be provided during this read. Data from the previously loaded address would immediately follow the device address protocol. It is possible to issue a stop or repeated start anytime during the write data payload procedure, but must be before the final acknowledge (i.e. canceling the write before the actual write operation is completed and performed). Also, the master would be allowed to access other devices attached to the I^2C bus before returning to select the CPS-10Q for the subsequent read operation from the loaded address.

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Read/Write Figures

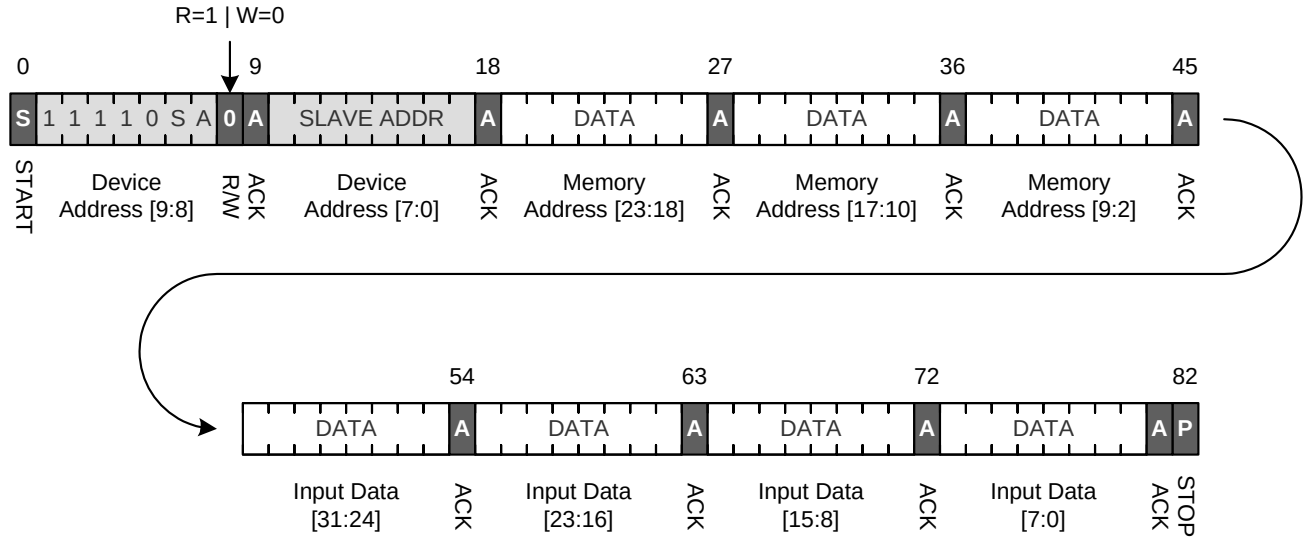

Figure 8 Write protocol with 10-bit Slave Address (ADS =1).

I^2C writes to memory align on 32-bit word boundaries, thus the 24 address MSBs must be provided while the 2 LSB's associated with word and byte pointers are DON'T CARE and are therefore not transmitted.

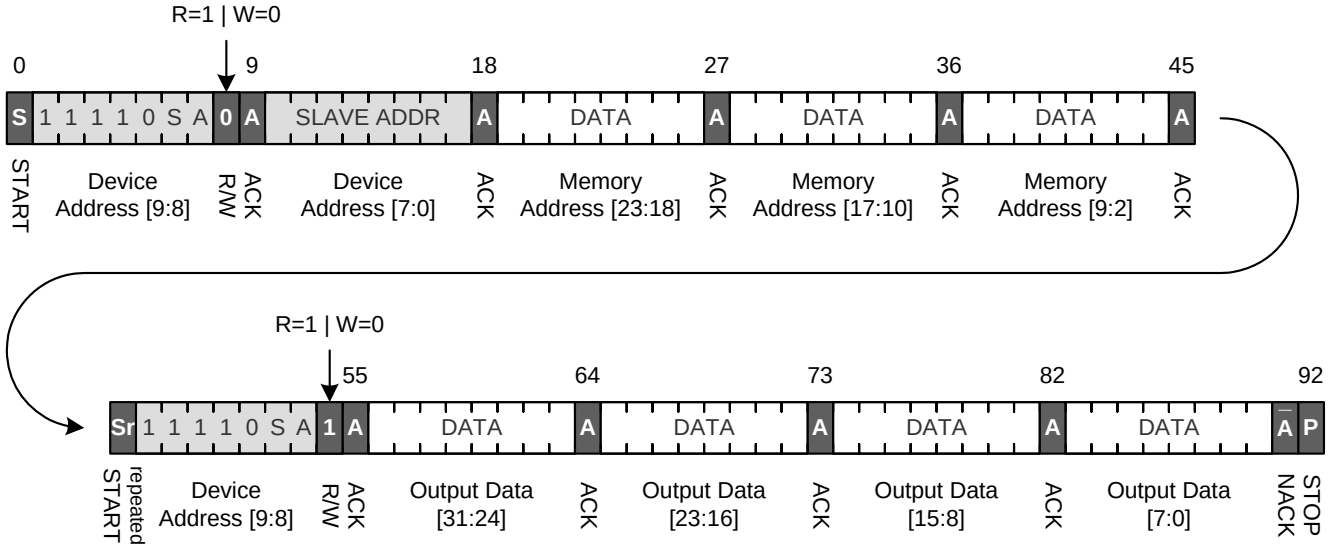

Figure 9 Read Protocol with 10-bit Slave Address (ADS=1)

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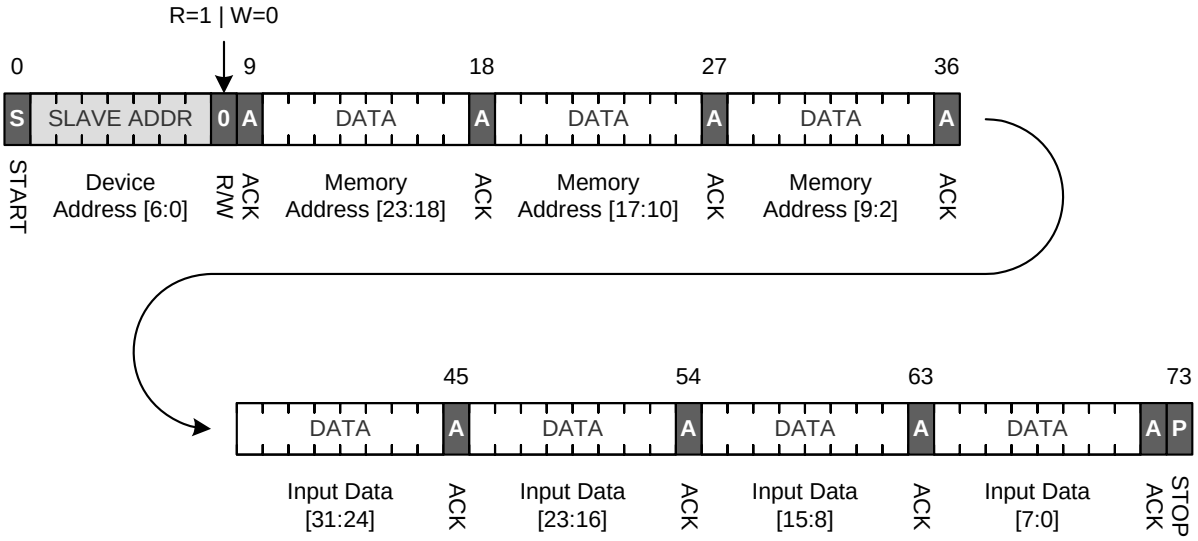

Figure 10 Write protocol with 7-bit Slave Address (ADS=0).

I^2C writes to memory align on 32-bit word boundaries, thus the 24 address MSBs must be provided while the 2 LSB's associated with word and byte pointers are DON'T CARE and are therefore not transmitted.

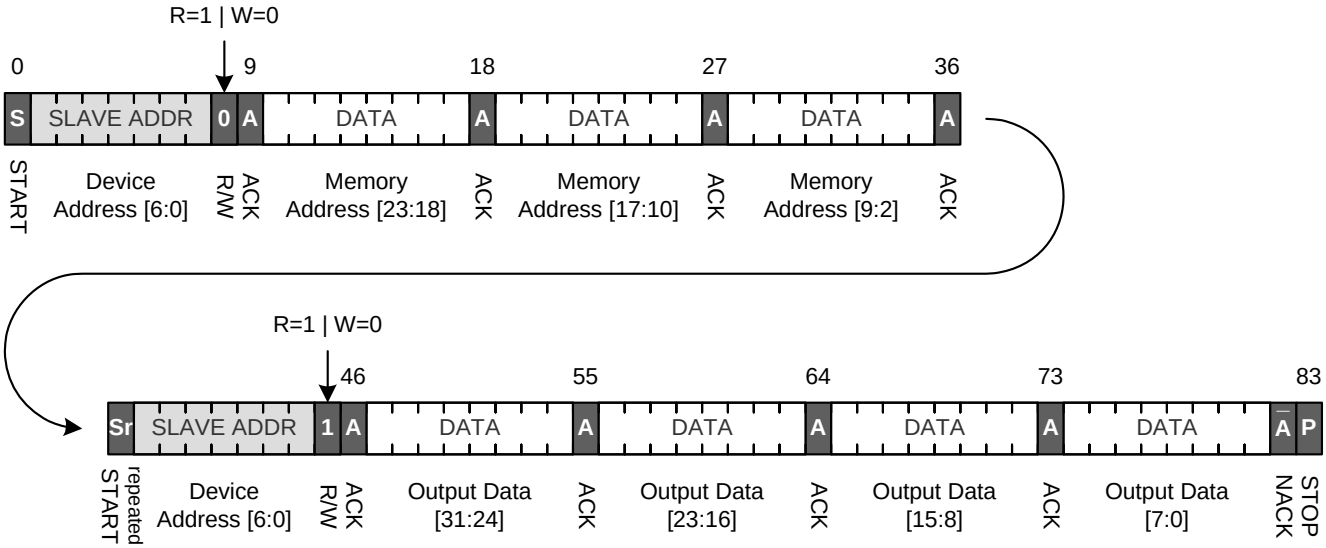

Figure 11 Read protocol with 7-bit Slave Address (ADS=0)

CPS-10Q Configuration and Image (Master mode)

There is both a power up master and a command master mode. If powered up in master mode, the CPS-10Q polls configuration image from external memory after the device reset sequence has completed. Once the device has completed its configuration sequence, it will revert to slave mode. Through a config register write, the device can be commanded to enter master mode, which provides more configuration sequence flexibility. Refer to "CPS-10Q User Manual" for details.

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I²C DC Electrical Specifications

Note that the ADS and ID pins will all run off the core (1.2V) power supply, and these pins are required to be fixed during operation. Thus, these pins must be statically tied to the 1.2V supply or GND.

Tables 12 through 14 below list the SDA and SCL electrical specifications for F/S-mode I²C devices.

At recommended operating conditions with V_{DD3} = 3.3V ± 5%

Parameter	Symbol	Minimum	Maximum	Unit
Input high voltage level	V_{IH}	0.7 x VDD3	VDD3 (MAX)+ 0.5	V
Input low voltage level	V_{IL}	-0.5	0.3 x VDD3	V
Hysteresis of Schmitt trigger inputs:	Vhys	0.05 x VDD3	-	
Low level output voltage	V_{OL}	0	0.4	V
Output fall time from VIH(MIN) to VIL(MAX) with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x VDD3 and 0.9 x VDD3 (MAX))	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF

Table 12 I²C SDA & SCL DC Electrical Specifications

At recommended operating conditions with V_{DD3} = 2.5V ± 100mV

Parameter	Symbol	Minimum	Maximum	Unit
Input high voltage level	V_{IH}	0.7 x VDD3	VDD3 (MAX)+ 0.1	V
Input low voltage level	V_{IL}	-0.5	0.3 x VDD3	V
Hysteresis of Schmitt trigger inputs:	Vhys	0.05 x VDD3	-	-
Low level output voltage	V_{OL}	0	0.4	V
Output fall time from VIH(MIN) to VIL(MAX) with a bus capacitance from 10pF to 400pF	t_{OF}	20 + 0.1 x C_b	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
Input current each I/O pin (input voltage is between 0.1 x VDD3 and 0.9 x VDD3 (MAX))	I_I	-10	10	uA
Capacitance for each I/O pin	C_I	-	10	pF

Table 13 I²C SDA & SCL DC Electrical Specifications

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I²C AC Electrical Specifications

Signal	Symbol	Reference Edge	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
I²C(1,4)							
SCL	f_{SCL}	none	0	100	0	400	kHz
	$t_{HD;STA}$		4.0	—	0.6	—	us
	t_R		—	1000	—	300	us
	t_F		—	300	—	300	us
SDA(2,3)	$t_{SV;DAT}$	SCL rising	250	—	100	—	us
	$t_{HD;DAT}$		0	3.45	0	0.9	us
	t_R		—	1000	10	300	us
	t_F		—	300	10	300	us
Start or repeated start condition	$t_{SU;STA}$	SDA falling	4.7	—	0.6	—	us
	$t_{SU;STO}$		4.0	—	0.6	—	us
Stop condition	$t_{SU;STO}$	SDA rising	4.0	—	0.6	—	us
Bus free time between a stop and start condition	t_{BUF}		4.7	—	1.3	—	us
Capacitive load for each bus line	C_B		—	400	—	400	pF

Table 14 Specifications of the SDA and SCL Bus Lines for F/S-mode I²C -bus Devices

Notes:

1. For more information, see the I ²C-Bus specification by Philips Semiconductor [1].
2. A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released.

I²C Timing Waveforms

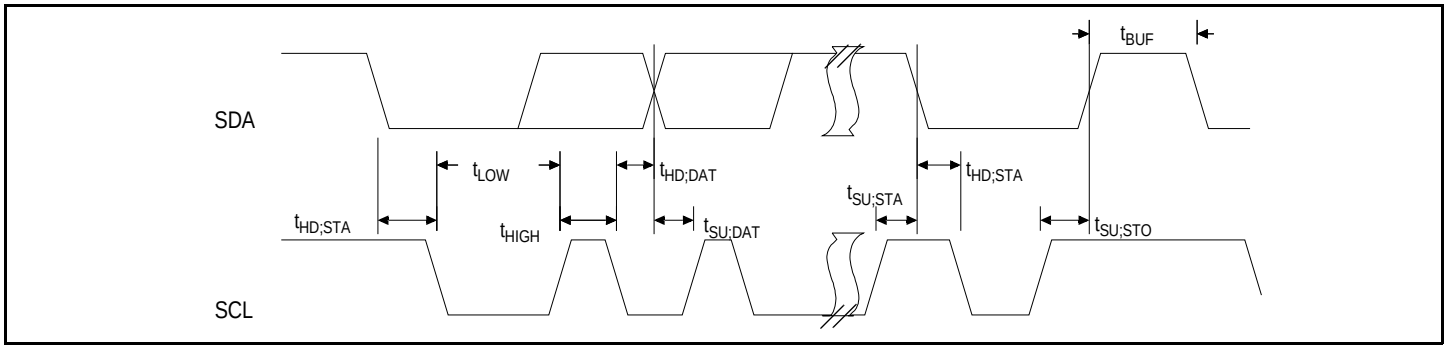

Figure 12 I²C Timing Waveforms

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14 Interrupt ($\overline{IRQ}$) Electrical Specifications

At recommended operating conditions with V_{DD3} = 3.3V ± 5%

Parameter	Symbol	Min	Max	Unit
Output low voltage (I_{OL} = 4mA, V_{DD3} = Min.)	V_{OL}	0	0.4	V
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	-	25	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for IRQ_N	C_I	-	10	pF

Table 15 $\overline{IRQ}$ Electrical Specifications (V_{DD3} = 3.3V ± 5%)

At recommended operating conditions with V_{DD3} = 2.5V ± 100mV

Parameter	Symbol	Min	Max	Unit
Output low voltage (I_{OL} = 2mA, V_{DD3} = Min.)	V_{OL}	0	0.4	V
Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$ with a bus capacitance from 10pF to 400pF	t_{OF}	-	25	ns
Input current each I/O pin (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_I	-10	10	uA
Capacitance for IRQ_N	C_I	-	10	pF

Table 16 $\overline{IRQ}$ Electrical Specifications (V_{DD3} = 2.5V ± 100mV)

Figure 13 $\overline{IRQ}$ Timing Diagram

The $\overline{IRQ}$ pin is an open-drain driver. IDT recommends a weak pull-up resistor (2-10k Ohm) be placed on this pin to V_{DD3}. The $\overline{IRQ}$ pin goes active low when any special error filter error flag is set, and is cleared when all error flags are reset. Please refer to the device user's manual for full detail.

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15 Serial RapidIO Ports

Overview

The CPS-10Q's SERDES are in full compliance to the RapidIO AC specifications for the LP-Serial physical layer [5]. This section provides those specifications for reference. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates, 1.25, 2.50, and 3.125 GBaud.

Two transmitter specifications allow for solutions ranging from simple chip-to-chip interconnect to driving two connectors across a backplane. A single receiver specification is given that will accept signals from both the short run and long run transmitter specifications.

The short run transmitter setting should be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane. The CPS-10Q can drive beyond the specification distance of at least 50 cm at all baud rates. Please use IDT's Simulation Kit IO models to determine reach and signal quality for a given PCB design.

Signal Definitions

LP-Serial links uses differential signaling. This section defines terms used in the description and specification of differential signals. Differential Peak-Peak Voltage of Transmitter or Receiver shows how the signals are defined. The figure shows waveforms for either a transmitter output (TD and $\overline{TD}$) or a receiver input (RD and $\overline{RD}$). Each signal swings between A Volts and B Volts where A > B. Using these waveforms, the definitions are as follows:

1. The transmitter output signals and the receiver input signals TD, $\overline{TD}$, RD and $\overline{RD}$ each have a peak-to-peak swing of A - B Volts
2. The differential output signal of the transmitter, V_{OD}, is defined as V_{TD}-$V_{\overline{TD}}$.
3. The differential input signal of the receiver, V_{ID}, is defined as V_{RD}-$V_{\overline{RD}}$.
4. The differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) Volts.
5. The peak value of the differential transmitter output signal and the differential receiver input signal is A - B Volts
6. The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 * (A - B) Volts

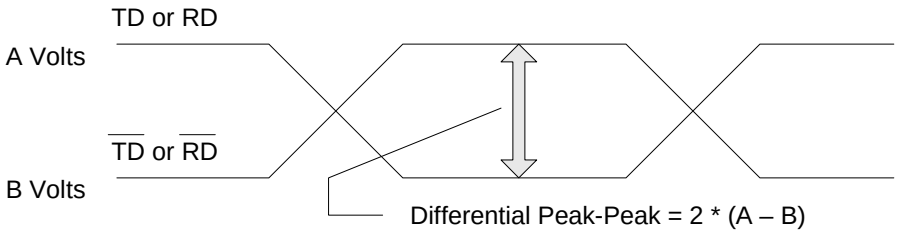

Figure 14 Differential Peak-Peak Voltage of Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of the signals TD and $\overline{TD}$ is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

Equalization

With the use of high speed serial links, the interconnect media will cause degradation of the signal at the receiver. Effects such as Inter-Symbol Interference (ISI) or data dependent jitter are produced. This loss can be large enough to degrade the eye opening at the receiver beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The equalization technique implemented in the CPS-10Q is Pre-emphasis on the transmitter (under register control).

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Explanatory Note on Transmitter and Receiver Specifications

AC electrical specifications are given for transmitter and receiver. Long run and short run interfaces at three baud rates (a total of six cases) are described.

The parameters for the AC electrical specifications are guided by the XAUI electrical interface specified in Clause 47 of IEEE 802.3ae-2002.

XAUI has similar application goals to serial RapidIO. The goal of this standard is that electrical designs for serial RapidIO can reuse electrical designs for XAUI, suitably modified for applications at the baud intervals and reaches described herein.

Transmitter Specifications

LP-Serial transmitter electrical and timing specifications are stated in the text and tables of this section.

The differential return loss, S11, of the transmitter in each case shall be better than

-10 dB for (Baud Frequency)/10 < Freq(f) < 625 MHz, and

-10 dB + 10log(f/625 MHz) dB for 625 MHz <= Freq(f) <= Baud Frequency

The reference impedance for the differential return loss measurements is 100 Ohm resistive. Differential return loss includes contributions from on-chip circuitry, chip packaging and any off-chip components related to the driver. The output impedance requirement applies to all valid output levels.

The CPS-10Q satisfies the specification requirement that the 20%-80% rise/fall time of the transmitter, as measured at the transmitter output, in each case has a minimum value 60 ps.

Similarly the timing skew at the output of an LP-Serial transmitter between the two signals that comprise a differential pair does not exceed 25 ps at 1.25 GB, 20 ps at 2.50GB and 15 ps at 3.125 GB.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{ODIFF\ PP}$	Differential Output Voltage	500	1000	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 17 Short Run Transmitter AC Timing Specifications - 1.25 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{ODIFF\ PP}$	Differential Output Voltage	500	1000	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 18 Short Run Transmitter AC Timing Specifications - 2.5 GBaud

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Symbol	Parameter	Range		Unit	Notes
		Min	Max		
VO	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
VODIFF PP	Differential Output Voltage	500	1000	mV p-p	
JD	Deterministic Jitter	-	0.17	UI p-p	
JT	Total Jitter	-	0.35	UI p-p	
SMO	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 19 Short Run Transmitter AC Timing Specifications - 3.125 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
VO	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
VODIFF PP	Differential Output Voltage	800	1600	mV p-p	
JD	Deterministic Jitter	-	0.17	UI p-p	
JT	Total Jitter	-	0.35	UI p-p	
SMO	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 20 Long Run Transmitter AC Timing Specifications - 1.25 GBaud

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
VO	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
VODIFF PP	Differential Output Voltage	800	1600	mV p-p	
JD	Deterministic Jitter	-	0.17	UI p-p	
JT	Total Jitter	-	0.35	UI p-p	
SMO	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 21 Long Run Transmitter AC Timing Specifications - 2.5 GBaud

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Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_O	Output Voltage	-0.40	2.30	Volts	Voltage relative to COMMON of either signal comprising a differential pair.
$V_{ODIFF\ PP}$	Differential Output Voltage	800	1600	mV p-p	
J_D	Deterministic Jitter	-	0.17	UI p-p	
J_T	Total Jitter	-	0.35	UI p-p	
S_{MO}	Multiple Output Skew	-	1000	ps	Skew at the transmitter output between lanes of a multilane link
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 22 Long Run Transmitter AC Timing Specifications - 3.125 GBaud

For each baud rate at which an LP-Serial transmitter is specified to operate, the output eye pattern of the transmitter falls entirely within the unshaded portion of the Transmitter Output Compliance Mask shown in Transmitter Output Compliance Mask (Figure 15) with the parameters specified in Transmitter Differential Output Eye Diagram Parameters (Table 17) when measured at the output pins of the device and the device is driving a 100 Ohm +/- 5% differential resistive load. The specification allows the output eye pattern of a LP-Serial transmitter that implements pre-emphasis (to equalize the link and reduce inter-symbol interference) to only comply with the Transmitter Output Compliance Mask when pre-emphasis is disabled or minimized.

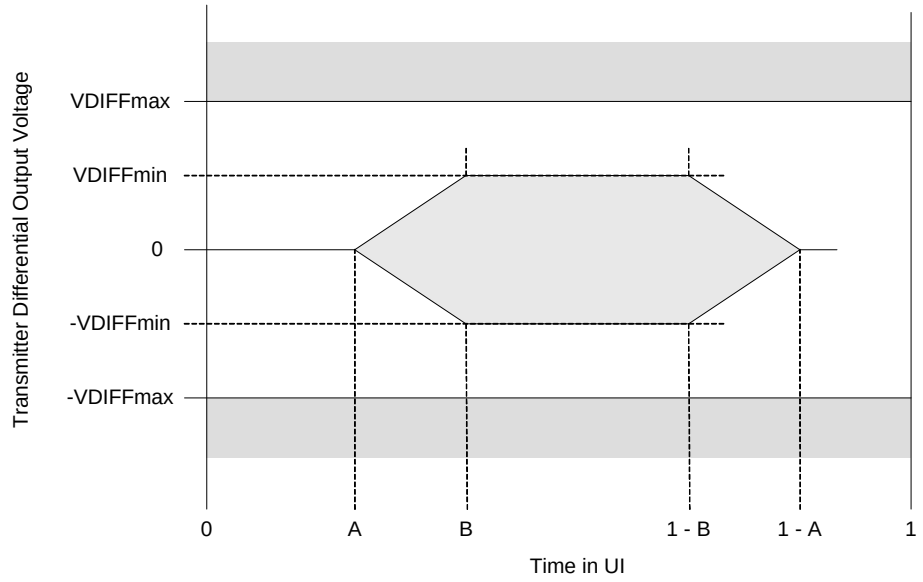

Figure 15 Transmitter Output Compliance Mask

Transmitter Setting	V_{DIFF}min (mV)	V_{DIFF}max (mV)	A (UI)	B (UI)
1.25 GBaud Short Range	250	500	0.175	0.39
1.25 GBaud Long Range	400	800	0.175	0.39
2.5 GBaud Short Range	250	500	0.175	0.39
2.5 GBaud Long Range	400	800	0.175	0.39
3.125 GBaud Short Range	250	500	0.175	0.39
3.125 Gbaud Long Range	400	800	0.175	0.39

Table 23 Transmitter Differential Output Eye Diagram Parameters

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Receiver Specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

The receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8)*(Baud Frequency). This includes contributions from on-chip circuitry, the chip package and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100 Ohm resistive for differential return loss and 25 Ohm resistive for common mode.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	24	ns	Skew at the receiver input between lanes of a multilane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	800	800	ps	+/- 100 ppm

Table 24 Receiver AC Timing Specifications - 1.25 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	24	ns	Skew at the receiver input between lanes of a multilane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	400	400	ps	+/- 100 ppm

Table 25 Receiver AC Timing Specifications - 2.5 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

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Symbol	Parameter	Range		Unit	Notes
		Min	Max		
V_{IN}	Differential Input Votlage	200	1600	mV p-p	Measured at receiver
J_D	Deterministic Jitter Tolerance	0.37	-	UI p-p	Measured at receiver
J_{DR}	Combined Deterministic and Random Jitter Tolerance	0.55	-	UI p-p	Measured at receiver
J_T	Total Jitter Tolerance(1)	0.65	-	UI p-p	Measured at receiver
S_{MI}	Multiple Input Skew	-	22	ns	Skew at the receiver input between lanes of a multilane link
BER	Bit Error Rate		10^{-12}		
UI	Unit Interval	320	320	ps	+/- 100 ppm

Table 26 Receiver AC Timing Specifications - 3.125 GBaud

NOTE:

1. Total jitter is composed of three components, deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 16. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

Figure 16 Single Frequency Sinusoidal Jitter Limits

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Receiver Eye Diagrams

For each baud rate at which an LP-Serial receiver is specified to operate, the receiver meets the corresponding Bit Error Rate specification (Receiver AC Timing Specifications - 1.25 GBaud, Receiver AC Timing Specifications - 2.5 GBaud, and Receiver AC Timing Specifications - 3.125 GBaud) when the eye pattern of the receiver test signal (exclusive of sinusoidal jitter) falls entirely within the unshaded portion of the Receiver Input Compliance Mask shown in (Figure 17) with the parameters specified in Receiver Input Compliance Mask Parameters exclusive of Sinusoidal Jitter. The eye pattern of the receiver test signal is measured at the input pins of the receiving device with the device replaced with a 100 Ohm +/- 5% differential resistive load.

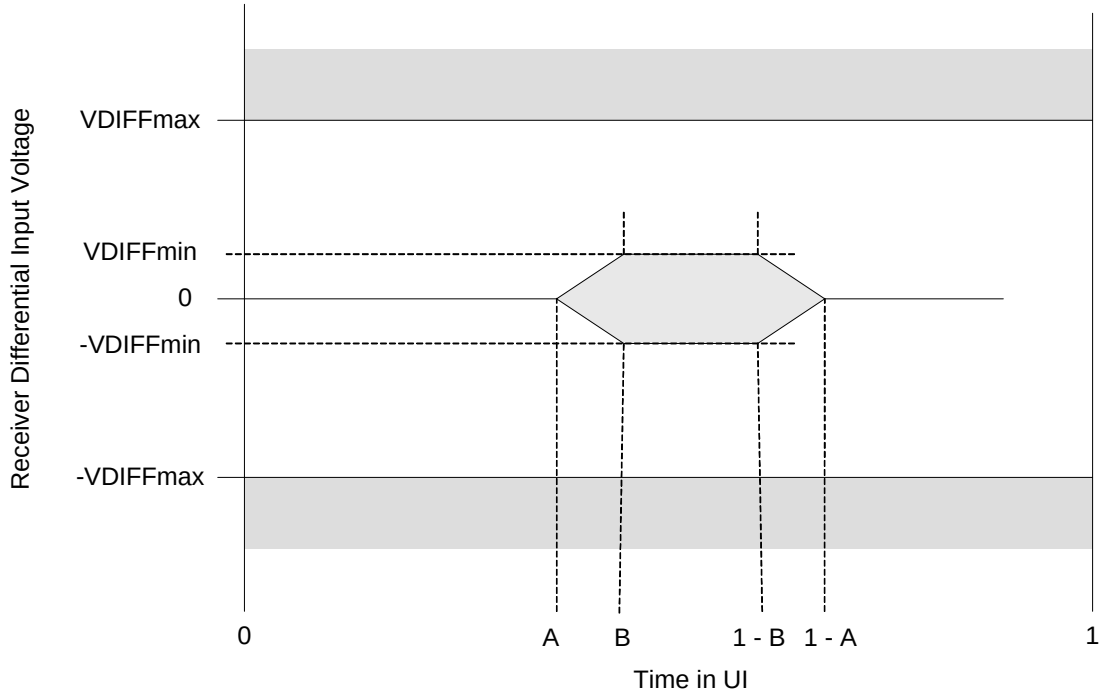

Figure 17 Receiver Input Compliance Mask

Receiver Rate	$V_{DIFFmin}$ (mV)	$V_{DIFFmax}$ (mV)	A (UI)	B (UI)
1.25 GBaud	100	800	0.275	0.400
2.5 GBaud	100	800	0.275	0.400
3.125 GBaud	100	800	0.275	0.400

Table 27 Receiver Input Compliance Mask Parameters Exclusive of Sinusoidal Jitter

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16 Reference Clock

The differential reference clock (REF_CLK+/-) is used to generate the sRIO PHY and internal clocks used in the CPS-10Q. This is a CML-based differential input.

Reference Clock Electrical Specifications

The reference clock is 156.25 MHz, and is AC-coupled with the following electrical specifications:

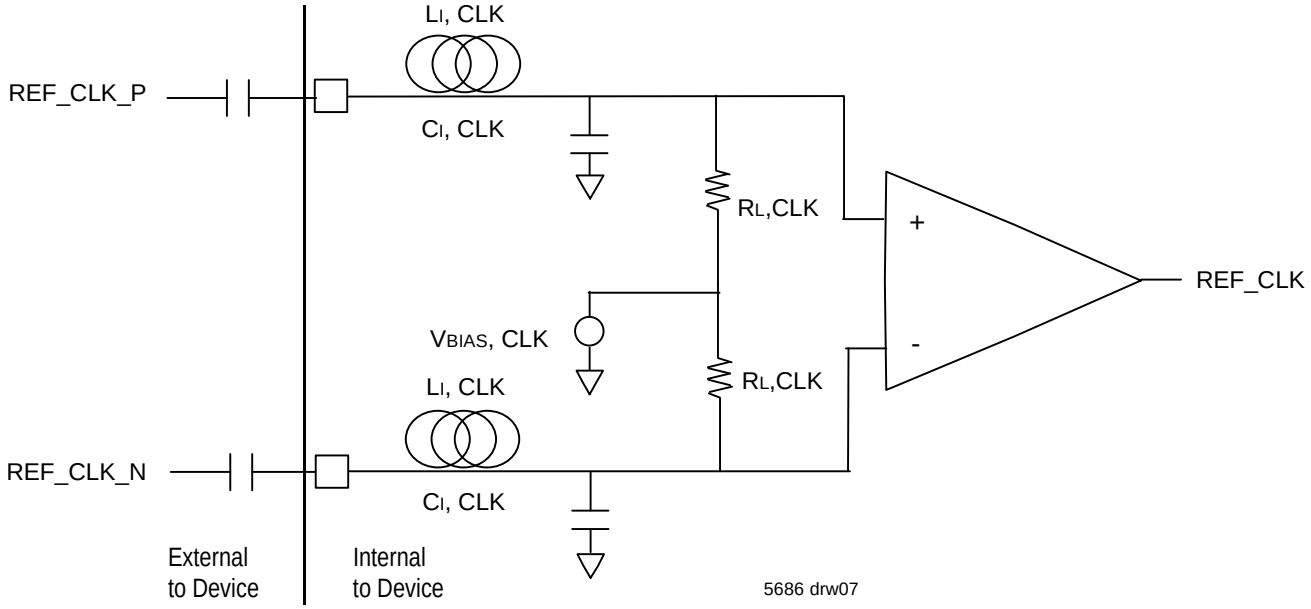

Figure 18 REF_CLK Representative Circuit

Name	Description	Min	Nom	Max	Units
REF_CLK	REF_CLK clock running at 156.25Mhz	-100	—	+100	ppm
Phase Jitter (rms)	Phase Jitter (rms) (1MHz - 20MHz)	—	—	2	ps
tDUTY_REF	REF_CLK duty cycle	40	50	60	%
tRCLK/tFCLK	Input signal rise/fall time (20%-80%)	200	500	650	ps
vIN_CML	Differential peak-peak REF_CLK input swing	400	—	2400	mV
RL_CLK	Input termination resistance	40	50	60	ohm
LI_CLK	Input inductance	—	—	4	nH
CI_CLK	Input capacitance	—	—	5	pF

Table 28 Input Reference Clock Jitter Specifications

The reference clock wander should not be more than 100ppm (for 156.25 MHz, this is +/-15.625 KHz). This requirement comes from the sRIO specification that outgoing signals from separate links which belong to the same port should not be separated more than 100ppm. We recommend the following device as reference clock device: ICS843001I-23 LVPECL, ICS8416641, ICS843256, ICS 87949, etc. Please contact IDT technical support for further clock support.

Note that the series capacitors are discrete that must be placed external to the device's receivers. All other elements are associated with the input structure internal to the device. VBIAS is generated internally.

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17 JTAG Interface

Description

The CPS-10Q offers full JTAG (Boundary Scan) support for both its slow speed and high speed pins. This allows “pins-down” testing of newly manufactured printed circuit boards as well as troubleshooting of field returns. The JTAG TAP interface also offers an alternative method for Configuration Register Access (CRA) (along with the sRIO and I^2C ports). Thus this port may be used for programming the device’s registers.

Boundary scan testing of the AC-coupled IOs is performed in accordance with IEEE 1149.6 (AC Extest).

IEEE 1149.1 (JTAG) & IEEE 1149.6 (AC Extest) Compliance

All DC pins are in full compliance with IEEE 1149.1 [10]. All AC-coupled pins fully comply with IEEE 1149.6 [11]. All 1149.1 and 1149.6 boundary scan cells are on the same chain. No additional control cells are provided for independent selection of negative and/or positive terminals of the TX- or RX-pairs.

System Logic TAP Controller Overview

The system logic utilizes a 16-state, six-bit TAP controller, a four-bit instruction register, and five dedicated pins to perform a variety of functions. The primary use of the JTAG TAP Controller state machine is to allow the five external JTAG control pins to control and access the CPS-10Q's many external signal pins. The JTAG TAP Controller can also be used for identifying the device part number. The JTAG logic of the device is depicted in the figure below.

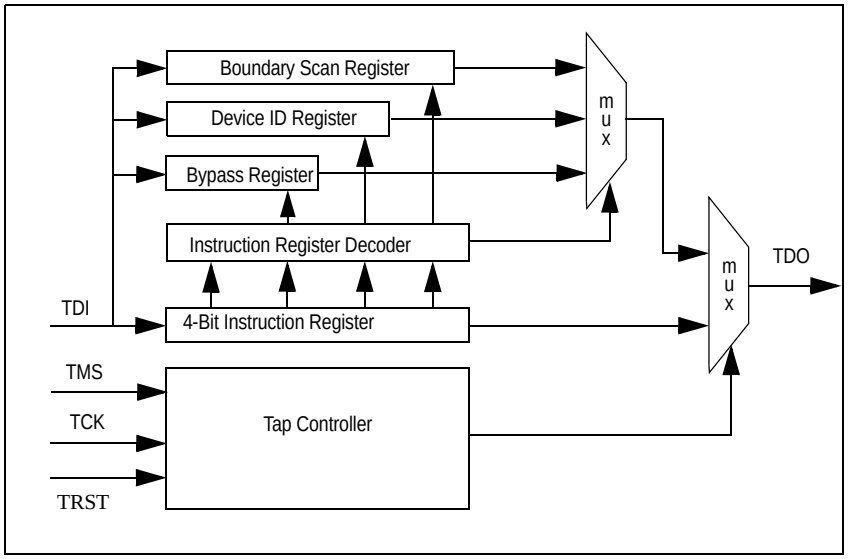

Figure 19 Diagram of the JTAG Logic

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Signal Definitions

JTAG operations such as Reset, State-transition control and Clock sampling are handled through the signals listed in the table below. A functional overview of the TAP Controller and Boundary Scan registers is provided in the sections following the table.

Pin Name	Type	Description
TRST	Input	JTAG RESET Asynchronous reset for JTAG TAP controller (internal pull-up)
TCK	Input	JTAG Clock Test logic clock. JTAG_TMS and JTAG_TDI are sampled on the rising edge. JTAG_TDO is output on the falling edge.
TMS	Input	JTAG Mode Select. Requires an external pull-up. Controls the state transitions for the TAP controller state machine (internal pull-up)
TDI	Input	JTAG Input Serial data input for BSC chain, Instruction Register, IDCODE register, and BYPASS register (internal pull-up)
TDO	Output	JTAG Output Serial data out. Tri-stated except when shifting while in Shift-DR and SHIFT-IR TAP controller states.

Table 29 JTAG Pin Descriptions

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The system logic TAP controller transitions from state to state, according to the value present on TMS, as sampled on the rising edge of TCK. The Test-Logic Reset state can be reached either by asserting TRST or by applying a 1 to TMS for five consecutive cycles of TCK. A state diagram for the TAP controller appears in Figure 5.2. The value next to state represent the value that must be applied to TMS on the next rising edge of TCK, to transition in the direction of the associated arrow.

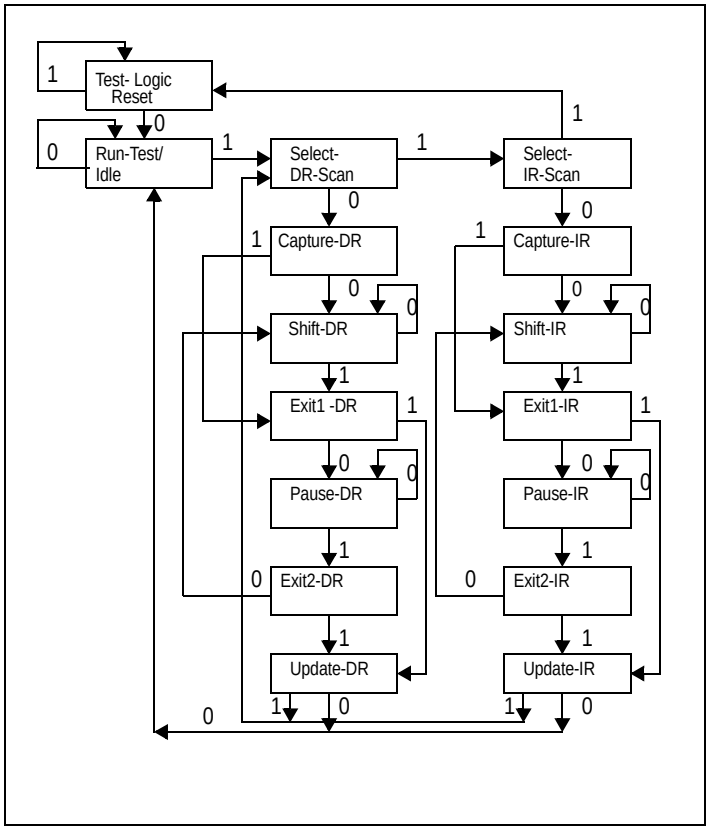

Figure 20 State Diagram of the TAP Controller

Test Data Register (DR)

The Test Data register contains the following:

- *The Bypass register*
- *The Boundary Scan registers*
- *The Device ID register*

These registers are connected in parallel between a common serial input and a common serial data output, and are described in the following sections. For more detailed descriptions, refer to IEEE Standard Test Access port (IEEE Std. 1149.1-1990).

Boundary Scan Registers

The CPS-10Q boundary scan chain is 142 bits long. The five JTAG pins do not have scan elements associated with them. Full boundary scan details can be found in the associated BSDL file which may be found on our web site (www.IDT.com). The boundary scan chain is connected between TDI and TDO when the EXTEST or SAMPLE/PRELOAD instructions are selected. Once EXTEST is selected and the TAP controller passes through the UPDATE-IR state, whatever value that is currently held in the boundary scan register's output latches is immediately transferred to the corresponding outputs or output enables.

Therefore, the SAMPLE/PRELOAD instruction must first be used to load suitable values into the boundary scan cells, so that inappropriate values are not driven out onto the system pins. All of the boundary scan cells feature a negative edge latch, which guarantees that clock skew cannot cause incorrect data to be latched into a cell. The input cells are sample-only cells. The simplified logic configuration is shown in the figure below.

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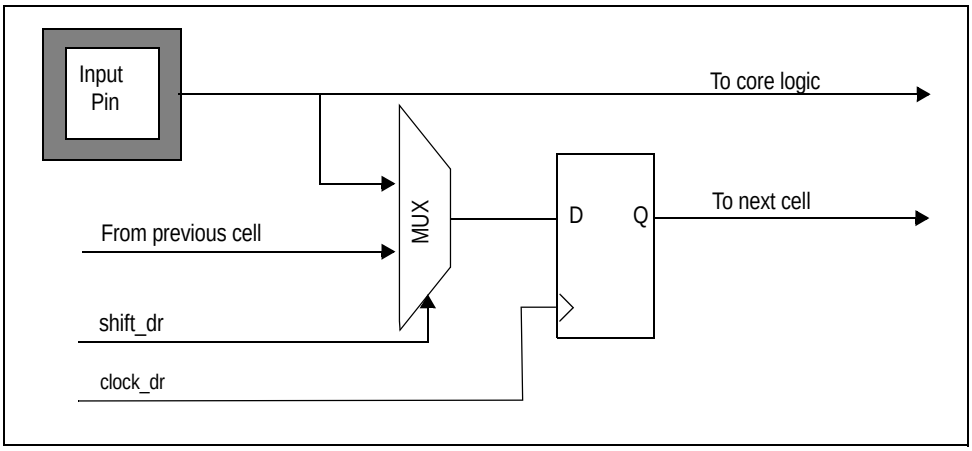

Figure 21 Diagram of Observe-only Input Cell

The simplified logic configuration of the output cells is shown in the figure below.

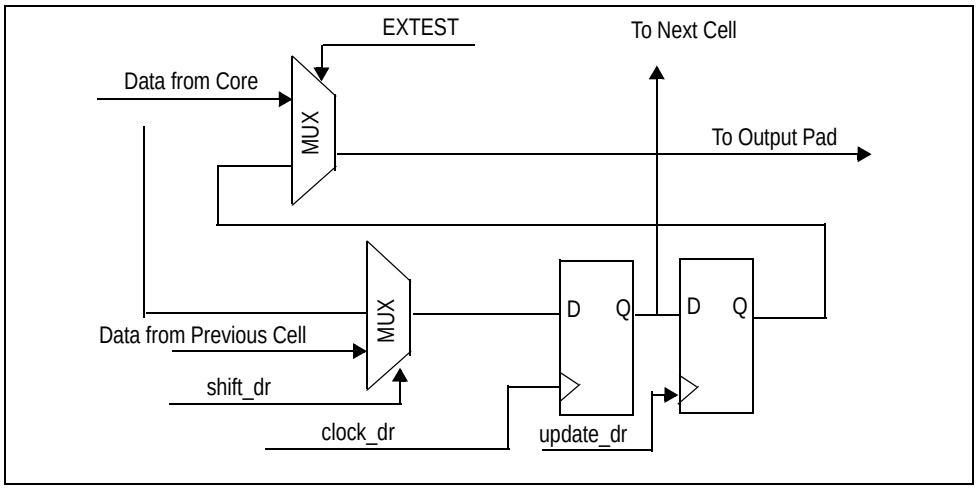

Figure 22 Diagram of Output Cell

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The output enable cells are also output cells. The simplified logic appears in the figure below.

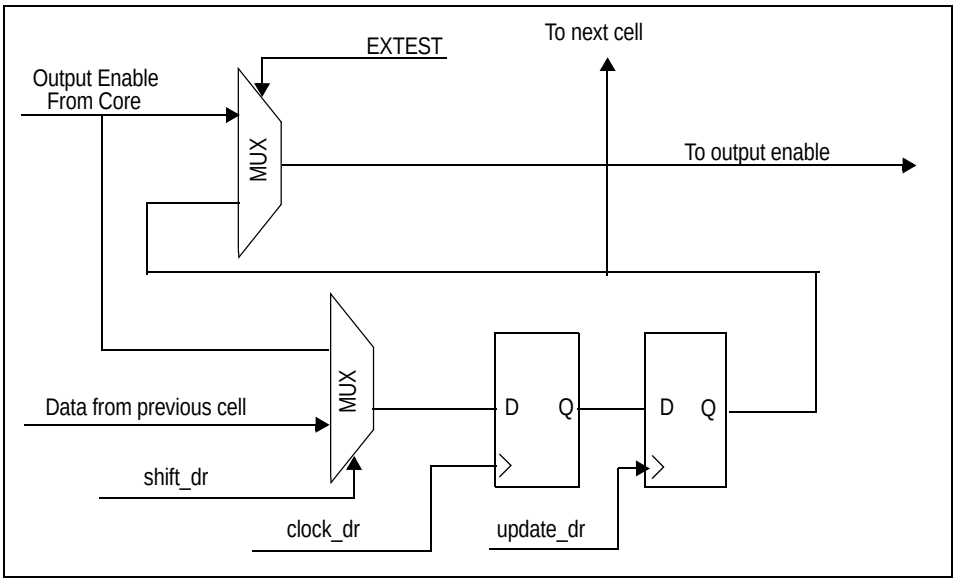

Figure 23 Diagram of Output Enable Cell

The bidirectional cells are composed of only two boundary scan cells. They contain one output enable cell and one capture cell, which contains only one register. The input to this single register is selected via a mux that is selected by the output enable cell when EXTEST is disabled. When the Output Enable Cell is driving a high out to the pad (which enables the pad for output) and EXTEST is disabled, the Capture Cell will be configured to capture output data from the core to the pad.

However, in the case where the Output Enable Cell is low (signifying a tri-state condition at the pad) or EXTEST is enabled, the Capture Cell will capture input data from the pad to the core. The configuration is shown graphically in the figure below.

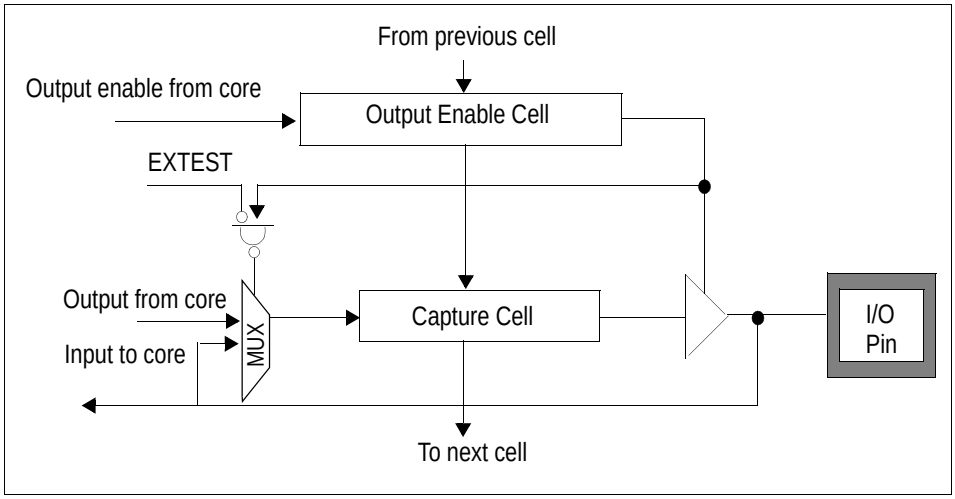

Figure 24 Diagram of Bidirectional Cell

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Instruction Register (IR)

The Instruction register allows an instruction to be shifted serially into the CPS-10Q at the rising edge of TCK. The instruction is then used to select the test to be performed or the test register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process, when the TAP controller is at the Update-IR state.

The Instruction Register contains four shift-register-based cells that can hold instruction data. This register is decoded to perform the following functions:

- To select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and selected data registers.
- To define the serial test data register path used to shift data between TDI and TDO during data register scanning.

The Instruction Register is comprised of 4 bits to decode instructions, as shown in the table below.

Instruction	Definition	OPcode [3:0]
EXTEST	Mandatory instruction allowing the testing of board level interconnections. Data is typically loaded onto the latched parallel outputs of the boundary scan shift register using the SAMPLE/PRELOAD instruction prior to use of the EXTEST instruction. EXTEST will then hold these values on the outputs while being executed. Also see the CLAMP instruction for similar capability.	0000
SAMPLE/ PRELOAD	Mandatory instruction that allows data values to be loaded onto the latched parallel output of the boundary-scan shift register prior to selection of the other boundary-scan test instruction. The Sample instruction allows a snapshot of data flowing from the system pins to the on-chip logic or vice versa.	0001
IDCODE	Provided to select Device Identification to read out manufacturer's identity, part, and version number.	0010
HIGHZ	Tri-states all output and bidirectional boundary scan cells.	0011
CLAMP	Provides JTAG user the option to bypass the part's JTAG controller while keeping the part outputs controlled similar to EXTEST.	0100
EXTEST_PULSE	AC Extest instruction implemented in accordance with the requirements of the IEEE std. 1149.6 specification.	0101
EXTEST_TRAIN	AC Extest instruction implemented in accordance with the requirements of the IEEE std. 1149.6 specification.	0110
RESERVED	Behaviorally equivalent to the BYPASS instruction as per the IEEE std. 1149.1 specification. However, the user is advised to use the explicit BYPASS instruction.	0111 — 1001
CONFIGURATION REGISTER ACCESS (CRA)	CPS-10Q-specific opcode to allow reading and writing of the configuration registers. Reads and writes must be 32-bits. See further detail below.	1010
PRIVATE	For internal use only. Do not use.	1011 — 1100
RESERVED	Behaviorally equivalent to the BYPASS instruction as per the IEEE std. 1149.1 specification. However, the user is advised to use the explicit BYPASS instruction.	1101
PRIVATE	For internal use only. Do not use.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

Table 30 Instructions Supported by CPS-10Q JTAG Boundary Scan

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EXTEST

The external test (EXTEST) instruction is used to control the boundary scan register, once it has been initialized using the SAMPLE/PRELOAD instruction. Using EXTEST, the user can then sample inputs from or load values onto the external pins of the CPS-10Q. Once this instruction is selected, the user then uses the SHIFT-DR TAP controller state to shift values into the boundary scan chain. When the TAP controller passes through the UPDATE-DR state, these values will be latched onto the output pins or into the output enables.

SAMPLE/PRELOAD

The sample/preload instruction has a dual use. The primary use of this instruction is for preloading the boundary scan register prior to enabling the EXTEST instruction. Failure to preload will result in unknown random data being driven onto the output pins when EXTEST is selected. The secondary function of SAMPLE/PRELOAD is for sampling the system state at a particular moment.

BYPASS

The BYPASS instruction is used to truncate the boundary scan register to a single bit in length. During system level use of the JTAG, the boundary scan chains of all the devices on the board are connected in series. In order to facilitate rapid testing of a given device, all other devices are put into BYPASS mode. Therefore, instead of having to shift 140 times to get a value through the CPS-10Q, the user only needs to shift one time to get the value from TDI to TDO. When the TAP controller passes through the CAPTURE-DR state, the value in the BYPASS register is updated to be 0.

If the device being used does not have an IDCODE register, then the BYPASS instruction will automatically be selected into the instruction register whenever the TAP controller is reset. Therefore, the first value that will be shifted out of a device without an IDCODE register is always 0. Devices such as the CPS-10Q that include an IDCODE register will automatically load the IDCODE instruction when the TAP controller is reset, and they will shift out an initial value of 1. This is done to allow the user to easily distinguish between devices having IDCODE registers and those that do not.

CLAMP

This instruction, listed as optional in the IEEE 1149.1 JTAG Specifications, allows the boundary scan chain outputs to be clamped to fixed values. When the clamp instruction is issued, the scan chain will bypass the CPS-10Q and pass through to devices further down the scan chain.

IDCODE

The IDCODE instruction is automatically loaded when the TAP controller state machine is reset either by the use of the TRST signal or by the application of a '1' on TMS for five or more cycles of TCK as per the IEEE Std 1149.1 specification. The least significant bit of this value must always be 1. Therefore, if a device has a IDCODE register, it will shift out a 1 on the first shift if it is brought directly to the SHIFT-DR TAP controller state after the TAP controller is reset. The board- level tester can then examine this bit and determine if the device contains a DEVICE_ID register (the first bit is a 1), or if the device only contains a BYPASS register (the first bit is 0).

However, even if the device contains an IDCODE register, it must also contain a BYPASS register. The only difference is that the BYPASS register will not be the default register selected during the TAP controller reset. When the IDCODE instruction is active and the TAP controller is in the Shift-DR state, the 32-bit value (0x0035E067) will be shifted out of the device-ID register.

Bit(s)	Mnemonic	Description	R/W	Reset
0	reserved	reserved 0x1	R	1
11:1	Manuf_ID	**Manufacturer Identity** (11 bits) IDT 0x33	R	0x33
27:12	Part_number	**Part Number** (16 bits) This field identifies the part number of the processor derivative. CPS-10Q = 0x035E	R	impl. dep.
31:28	Version	**Version** (4 bits) This field identifies the version number of the processor derivative. CPS-10Q = 0x0035E067	R	impl. dep.

Table 31 System Controller Device Identification Register

Version	Part Number	Vendor ID	LSB
0000	0000|0011|0101|1110	0000|0110|011	1

Table 32 System Controller Device ID Instruction Format

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EXTEST PULSE

This IEEE 1149.6 instruction applies only to the AC-coupled pins. All DC pins will perform as if the IEEE Std 1149.1 EXTEST instruction is operating whenever the EXTEST_PULSE instruction is effective.

The EXTEST_PULSE instruction enables edge-detecting behavior on signal paths containing AC pins, where test receivers reconstruct the original waveform created by a driver even when signals decay due to AC-coupling.

As the operation name suggests, enabling EXTEST_PULSE causes a pulse to be issued which can be detected even on AC-coupled receivers. Refer to the IEEE Std 1149.6 for full details. Below is a short synopsis.

If enabled, the output signal is forced to the value in its associated Boundary-Scan Register data cell for its driver (true and inverted values for a differential pair) at the falling edge of TCK in the Update-IR and Update-DR TAP Controller states. The output subsequently transitions to the opposite of that state (an inverted state) on the first falling edge of TCK that occurs after entering the Run-Test/Idle TAP Controller state. It then transitions back again to the original state (a noninverted state) on the first falling edge of TCK after leaving the Run-Test/Idle TAP Controller state.

EXTEST TRAIN

This IEEE 1149.6 instruction applies only to the AC-coupled pins. All DC pins will perform as if the IEEE Std 1149.1 EXTEST instruction is operating whenever the EXTEST_PULSE instruction is effective.

The EXTEST_TRAIN instruction enables edge-detecting behavior on signal paths containing AC pins, where test receivers reconstruct the original waveform created by a driver even when signals decay due to AC-coupling.

As the operation name suggests, enabling EXTEST_TRAIN causes a pulse train to be issued which can be detected even on AC-coupled receivers. Once in an enabled state, the train will be sent continuously in response to the TCK clock. No other signaling is required to generate the pulse train while in this state. Refer to the IEEE Std 1149.6 for full details. Below is a short synopsis.

First, the output signal is forced to the state matching the value (a noninverted state) in its associated Boundary-Scan Register data cell for its driver (true and inverted values for a differential pair), at the falling edge of TCK in update-IR. Then the output signal transitions to the opposite state (an inverted state) on the first falling edge of TCK that occurs after entering the Run-Test/Idle TAP Controller state. While remaining in this state, the output signal will continue to invert on every falling edge of TCK, thereby generating a pulse train.

RESERVED

Reserved instructions are not implemented, but default to a BYPASS mode. IDT recommends using the standard BYPASS opcode rather than RESERVED opcodes if BYPASS functionality is desired.

PRIVATE

Private instructions implement various test modes used in the device manufacturing process. The user should not enable these instructions.

Usage Considerations

As previously stated, there are internal pull-ups on TRST, TMS, and TDI. However, TCK also needs to be driven to a known value. It is best to either drive a zero on the TCK pin when it is not being used or to use an external pull-down resistor. In order to guarantee that the JTAG does not interfere with normal system operation, the TAP controller should be forced into the Test-Logic-Reset controller state by continuously holding TRST low and/or TMS high when the chip is in normal operation. If JTAG will not be used, externally pull-down TRST low to disable it.

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JTAG Configuration Register Access

As previously mentioned, the JTAG port may be used to read and write to the CPS-10Q's configuration registers. The same JTAG instruction (4b1010) is used for both writes and reads.

Bits	Field Name	Size	Description
0	jtag_config_wr_n	1	1 – read configuration register 0 – write configuration register
Bits	**Field Name**	**Size**	**Description**
[22:1]	jtag_config_addr	22	Starting address of the memory mapped configuration register. 22 address bits map to a unique double-word aligned on a 32-bit boundary. This provides accessibility to and is consistent with the sRIO memory mapping.
[54:23]	jtag_config_data	32	Reads: Data shifted out (one 32-bit word per read) is read from the configuration register at address jtag_config_addr. Writes: Data shifted in (one 32-bit word per write) is written to the configuration register at address jtag_config_addr.

Table 33 Data Stream for JTAG Configuration Register Access Mode

Writes during Configuration Register Access

A write is performed by shifting the CRA OPcode into the Instruction Register (IR), then shifting in first a read / write select bit, then both the 22-bit target address and 32-bit data into the Data Register (DR). When bit 0 of the data stream is 0, data shifted in after the address will be written to the address specified in jtag_config_addr. The TDO pin will transmit all 0s. See the figure below for the associated timing diagram.

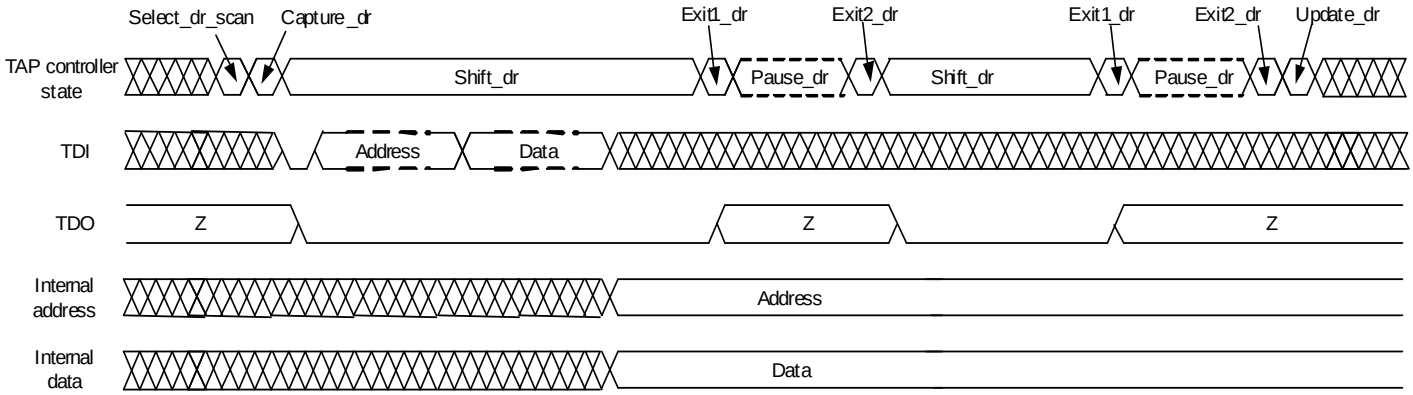

Figure 25 Implementation of write during configuration register access

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Reads during Configuration Register Access

Reads are much like writes except that target data is not provided. When bit 0 of the data stream is 1, data shifted out will be read from the address specified in jtag_config_addr. TDI will not be used after the address is shifted in. As a function of read latency in the architecture, the first 16 bits will be 0's and must be ignored. The following bits will contain the actual register bits.

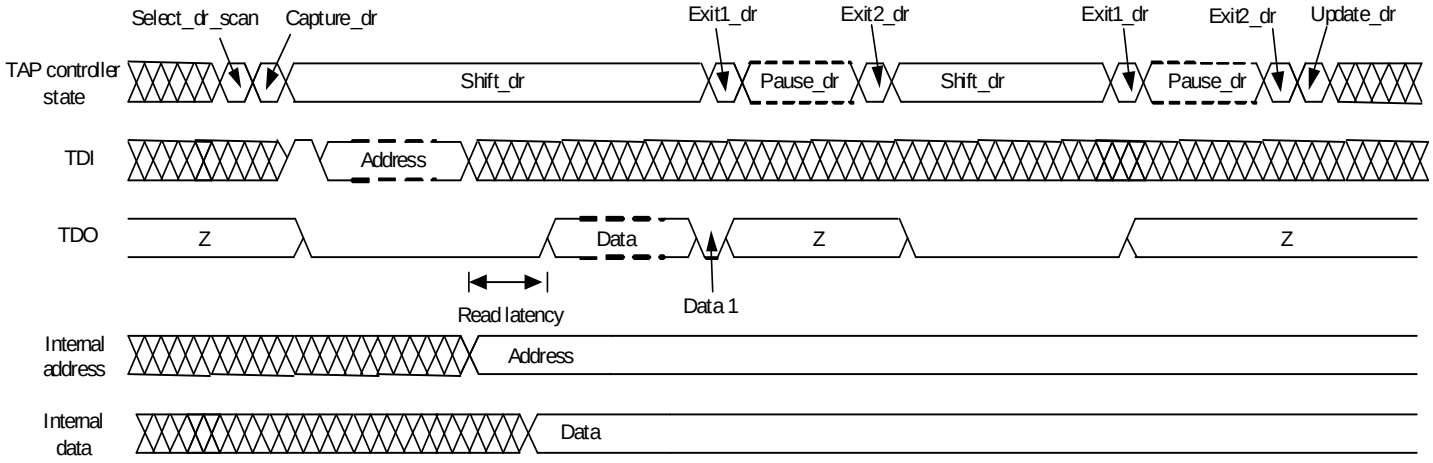

Figure 26 Implementation of read during configuration register access

JTAG DC Electrical Specifications

At recommended operating conditions with V_{DD3} = 3.3V ± 5%

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	2.0	$V_{DD3(max)}$ + 0.15	V
Input low voltage level	V_{IL}	-0.3	0.8	V
Output high voltage (I_{OH} = -4mA, V_{DD3} = Min.)	V_{OH}	2.4	-	V
Output low voltage (I_{OL} = 4mA, V_{DD3} = Min.)	V_{OL}	-	0.4	V
Input current for JTAG pins (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_{LI}	-30	30	uA
Capacitance for each Input pin	C_{IN}	-	8	pF
Capacitance for each I/O or Output pin	C_{OUT}	-	10	pF

Table 34 JTAG DC Electrical Specifications (V_{DD3} = 3.3V ± 5%)

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At recommended operating conditions with V_{DD3} = 2.5V ± 100mV

Parameter	Symbol	Min	Max	Unit
Input high voltage level	V_{IH}	1.7	$V_{DD3(max)}$ + 0.1	V
Input low voltage level	V_{IL}	-0.3	0.7	V
Output high voltage (I_{OH} = -2mA, V_{DD3} = Min.)	V_{OH}	2.0	-	V
Output low voltage (I_{OL} = 2mA, V_{DD3} = Min.)	V_{OL}	-	0.4	V
Input current for JTAG pins (input voltage is between 0.1 x V_{DD3} and 0.9 x V_{DD3} (max))	I_{LI}	-30	30	uA
Capacitance for each Input pin	C_{IN}	-	8	pF
Capacitance for each I/O or Output pin	C_{OUT}	-	10	pF

Table 35 JTAG DC Electrical Specifications (V_{DD3} = 2.5V ± 100mV)

JTAG AC Electrical Specifications(2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	0	25	MHz
t_{JCH}	JTAG Clock HIGH	16	-	ns
t_{JCL}	JTAG Clock LOW	16	-	ns
t_{JR}	JTAG Clock Rise Time	-	3(1)	ns
t_{JF}	JTAG Clock Fall Time	-	3(1)	ns
t_{JRST}	JTAG Reset	50	-	ns
t_{JRSR}	JTAG Reset Recovery	50	-	ns
t_{JCD}	JTAG Data Output	-	25	ns
t_{JDC}	JTAG Data Output Hold	0	-	ns
t_{JS}	JTAG Setup	15	-	ns
t_{JH}	JTAG Hold	15	-	ns

Table 36 JTAG AC Electrical Specifications

Notes:
1. Guaranteed by design.
2. Refer to AC Electrical Test Conditions stated earlier in this document.
3. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

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JTAG Timing Waveforms

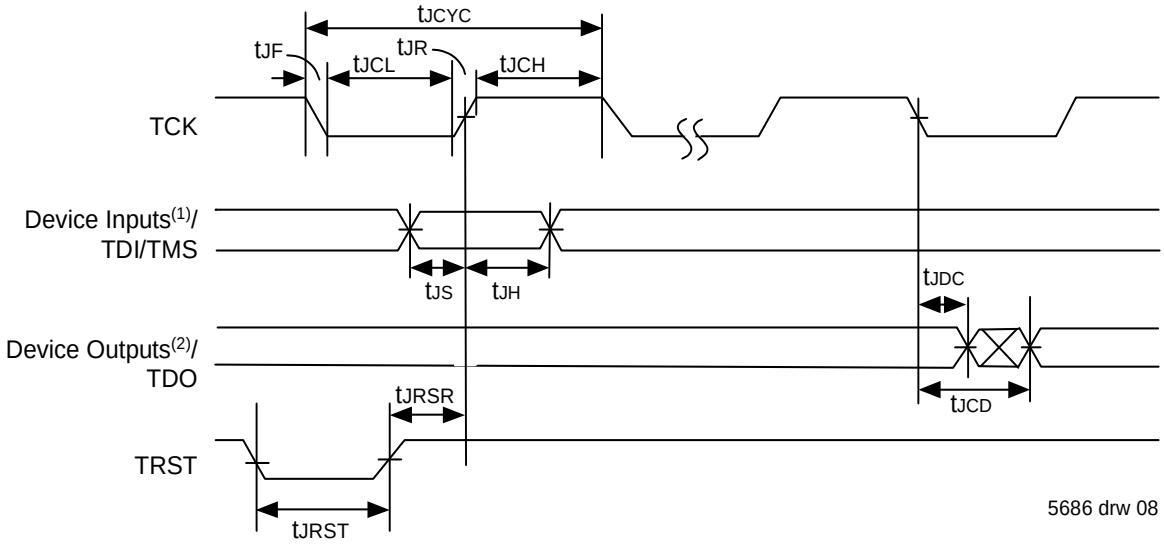

Figure 27 JTAG Timing Specifications

Notes:
1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

18 Reset & Initialization

Power Supply Sequencing

The CPS-10Q does not require specific power sequencing between any of the core and I/O supplies.

Reset Pin and Timing

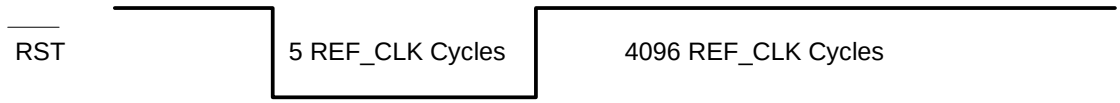

Figure 28 Reset Timing

To reset the device, first reset signal has to be de-asserted (Reset Low), and it is asserted after 5 REF_CLK cycles. 4096 REF_CLK cycles later, the device completes the reset process. Once completed, access to the CPS-10Q from any and all interfaces is possible and the device is fully functional. Control and data traffic will not be accepted by the CPS-10Q until this process is fully completed.

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80KSW0005 Quad Type and Configuration

Lane#	Quad#	Quad Type	Default on Reset	1x-Ports Only Port Numbering	4x-Ports Only Port Numbering
3 - 0	0	Standard	Standard	0	0
7 - 4	1	Standard	Standard	1	1
11 - 8	2	Standard	Standard	2	2
15 - 12	3	Standard	Standard	3	3
16	4	Enhanced	Enhanced	4	4
17				5	
18				6	
19				7	
23 - 20	5	Standard	Standard	8	5
27 - 24	6	Standard	Standard	9	6
31 - 28	7	Standard	Standard	10	7
35 - 32	8	Standard	Standard	11	8
36	9	Enhanced	Enhanced	12	9
37				13	
38				14	
39				15	

Table 37 Reset Port Configuration

Speed Select (SPD[1:0])

There are 2 port speed select pins. These pins are used to chose the initial speed on sRIO ports. The selection table is given below:

Value on the Pins (SPD1, SPD0)	Ports Rate
00	1.25Gbps
01	2.5Gbps
10	3.125Gbps
11	Reserved

Table 38 Port Speed Selection Pin Values

At power-up the CPS-10Q is configured as a 16-port device. 8 ports are configured as x4 ports and 8 ports are configured as x1 ports with each link running at 1.25, 2.5, or 3.125 Gbps (depending on the SPD[1:0] pins) on each link.

An end-point connected to the CPS-10Q can then reprogram all the ports to the desired configuration. All ports are configured as long run at start up because it will allow the port to communicate to either a short run or long run port on the CPU.

Initialization of sRIO Switching

At the initialization all values in the route table are programmed as default route. But the CPS-10Q accepts maintenance packets. These maintenance packets may be used to configure the device.

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19 Pinout

Figure 29 Pinout (TOP VIEW)

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20 Pin Summary

Pin Name	Function	Supply	Interface	Pin Function Description
ADS	I^2C	(V_{DD}, GND)	CMOS Input	I^2C address width select. Set ADS = GND for 7-bit CPS-10Q slave address. ADS = Vdd for 10-bit. NOTE: SUPPLY / LEVELS REQUIREMENTS ARE UNIQUE FROM THE OTHER I^2C PINS.
DNC				Do Not Connect. This pin should be left FLOATING. It should not be connected to any other signal or power rail.
GND	Digital Ground (CMOS)			Digital GND. All pins must be tied to single potential power supply ground plane.
GNDS	Analog Ground (CMOS)			Analog GND. All pins must be tied to single potential ground supply plane.
ID0 - ID9	I^2C	(V_{DD}, GND)	CMOS Input	I^2C Slave ID addresses. This should be set statically to Vdd or GND at power-up. NOTE: SUPPLY / LEVELS REQUIREMENTS ARE UNQUE FROM THE OTHER I^2C PINS.
MM	I^2C	(V_{DD}, GND)	CMOS Input	Select the I^2C Master or Slave mode. Logic high for Master mode
$\overline{IRQ}$	Interrupt	($V_{DD}3$, GND)	CMOS Open Drain Output	This is interrupt output pin whose value is given by the Error Management Block. Note: This is an open drain and requires an external pull-up resistor.
REF_CLK +/-	SERDES Clock	(V_{DD}, GND)	CML Differential Input	This clock is used as the 156.25 MHz reference for standard SERDES operation.
REXTN, REXTP	Rext			External bias resistor. Rextn must be connected to Rextp with a 12k Ohm resistor. This establishes the drive bias on the SERDES output. This provides CML driver stability across process and temperature.
$\overline{RST}$	Reset	($V_{DD}3$, GND)	CMOS Input	Global Reset. Sets all internal registers to default values. Resets all PLLs. Resets all port configurations. This is a HARD Reset.
RX0+/- to RX39+/-	sRIO Receive	(V_{DDS}, GNDS)	RIO Differential Input	Differential receiver inputs, Lanes 0 to 39
SCL	I^2C	($V_{DD}3$, GND)	CMOS Input	I^2C Clock.
SDA	I^2C	($V_{DD}3$, GND)	CMOS IO	I^2C Serial Data IO. Data direction is determined by the I^2C Read/Write bit. See I^2C section for further detail.
SPD[1:0]	SPD	(V_{DD}, GND)	CMOS Input	Speed Select Pins. These pins define sRIO port speed at RESET for all ports. The RESET setting may be overridden by subsequent programming of the QUAD_CTRL register. SPD[1:0] = {00 = 1.25G, 01 = 2.5G, 10 = 3.125G, 11 = RESERVED}. These pins must remain STATICALLY BIASED after power-up.
TCK	JTAG	($V_{DD}3$, GND)	CMOS Input	JTAG Tap Port Clock
TDI	JTAG	($V_{DD}3$, GND)	CMOS Input	JTAG Tap Port Input
TDO	JTAG	($V_{DD}3$, GND)	CMOS output	JTAG Tap Port Output
TMS	JTAG	($V_{DD}3$, GND)	CMOS Input	JTAG Tap Port Mode Select
$\overline{TRST}$	JTAG	($V_{DD}3$, GND)	CMOS Input	JTAG Tap Port Asynchronous Reset
TX0+/- to TX39+/-	sRIO Transmit	(V_{DDS}, GNDS)	RIO Differential Output	Differential transmitter outputs, Lanes 0 to 39
V_{DD}	1.2V Digital Power (CMOS)			Digital VDD. All pins must be tied to single potential power supply plane.
$V_{DD}3$	3.3V Digital Power (CMOS)			Digital Interface V_{DD}. All pins must be tied to single potential power supply plane.

Table 39 Pin Summary (Alphabetical)

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Pin Name	Function	Supply	Interface	Pin Function Description
V_{DDA}	Analog Power (CMOS)			Analog power. V_{DDS} & V_{DDA} may be tied to a common power plane. V_{DD} (core, digital supply) should have its own supply and plane.
V_{DDS}	SERDES Power (CMOS)			Analog power for TX/RX pairs. V_{DDS} & V_{DDA} may be tied to a common power plane. V_{DD} (core, digital supply) should have its own supply and plane.

Table 39 Pin Summary (Alphabetical)

Note:

1. REF_CLK, RX and TX (differential input/output) are all CML based.

21 Package Specifications

Package Physical & Thermal Specifications

Package: Super FlipChip FCBGA (BR676)

Dimensions: 27 X 27 mm

Ball Count: 676

Ball Diameter: 0.6mm

Ball Pitch: 1.0 mm

Theta J_A = {16.1 C/W @ 0m/s, 10.7 C/W @ 1m/s, 9.1 C/W @ 2m/s}

Theta J_C = 0.2 C/W

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22 Package Drawings

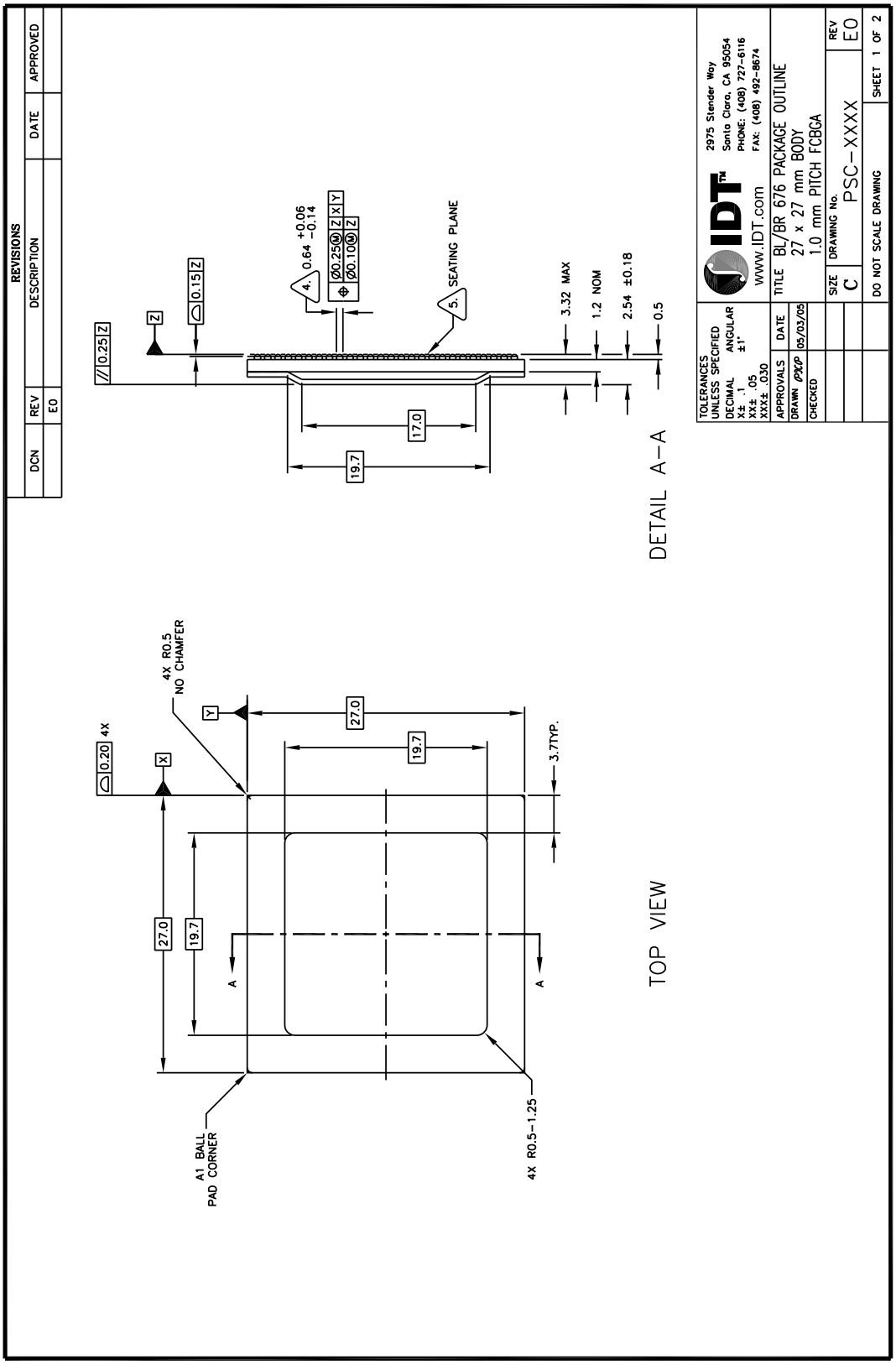

Figure 30 Package Drawings 1 of 2

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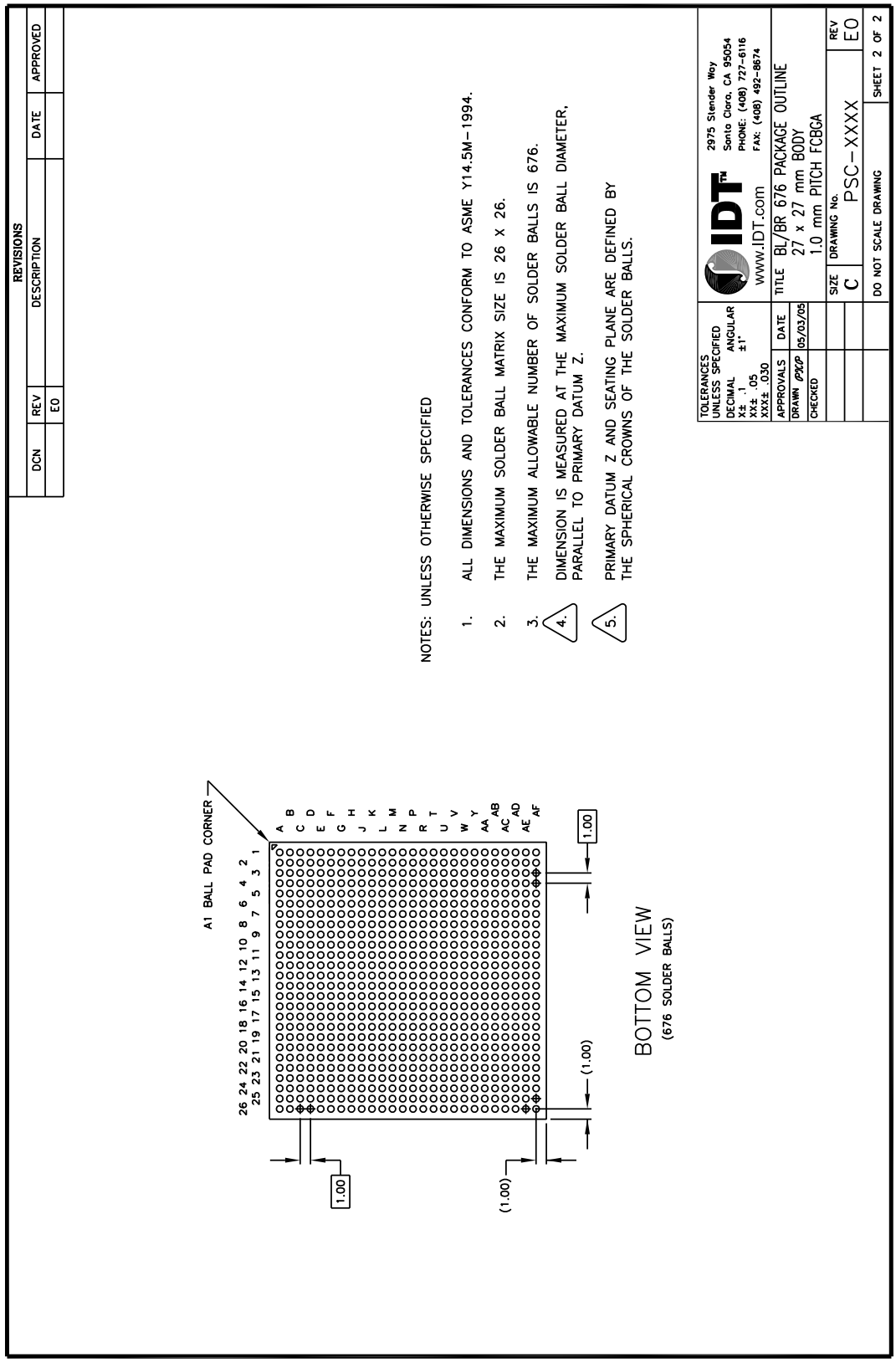

Figure 31 Package Drawing 2 of 2

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23 References & Standards

[1] "The I^2C-BUS Specification", version 2.1, January 2000, Philips

[2] RapidIO Interconnect Specification, Part I: Input/Output Logical Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[3] RapidIO Interconnect Specification, Part II: Message Passing Logical Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[4] RapidIO Interconnect Specification, Part III: Common Transport Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[5] RapidIO Interconnect Specification, Part VI: Physical Layer 1x/4x LP-Serial Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[6] RapidIO Interconnect Specification, Part VII: System and Device Inter-operability Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[7] RapidIO Interconnect Specification, Part VIII: Error Management Extensions Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[8] RapidIO Interconnect Specification, Part IX: Logic Layer Flow Control Extensions Specification, Rev. 1.0, 06/2005, RapidIO Trade Association

[9] RapidIO Interconnect Specification, Annex I: Software/System Bring Up Specification, Rev. 1.3, 06/2005, RapidIO Trade Association

[10] IEEE Std 1149.1-2001 IEEE Standard Test Access Port and Boundary-Scan Architecture

[11] IEEE Std 1149.6-2003 IEEE Standard for Boundary-Scan Testing of Final Digital Networks

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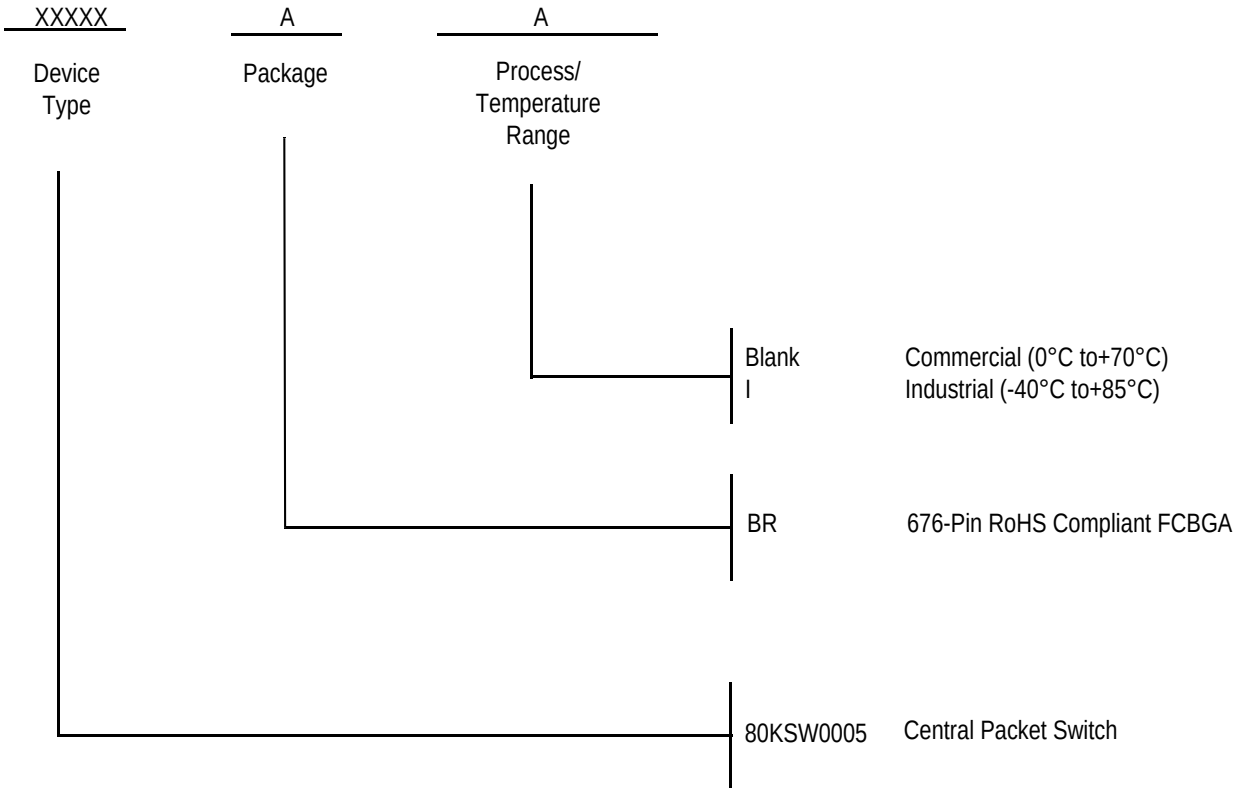
24 Ordering Information



25 Revision History

11/25/2008: Revision 0. Initial release

1/18/2011: Revision 1. Fixed a number of minor errors and inconsistencies.

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