

SN74LVC1G139 2-to-4 Line Decoder

1 Features

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Maximum t_{pd} of 4.9 ns at 3.3 V and 15 pF
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Solid State Drives (SSDs): Client and Enterprise
- TVs: LCD/Digital and High-Definition (HDTVs)
- Tablets: Enterprise
- Video Analytics: Server

3 Description

This 2-to-4 line decoder is designed for 1.65-V to 5.5-V V_{CC} operation.

The LVC1G139 2-line to 4-line decoder is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When used with high-speed memories using a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

NanoStar and NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---------------------|-----------|-------------------|
| SN74LVC1G139DC T | SM8 (8) | 2.95 mm x 2.80 mm |
| SN74LVC1G139DC U | VSSOP (8) | 2.30 mm x 2.00 mm |
| SN74LVC1G139YZ P | DSBGA (8) | 1.91 mm x 0.91 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

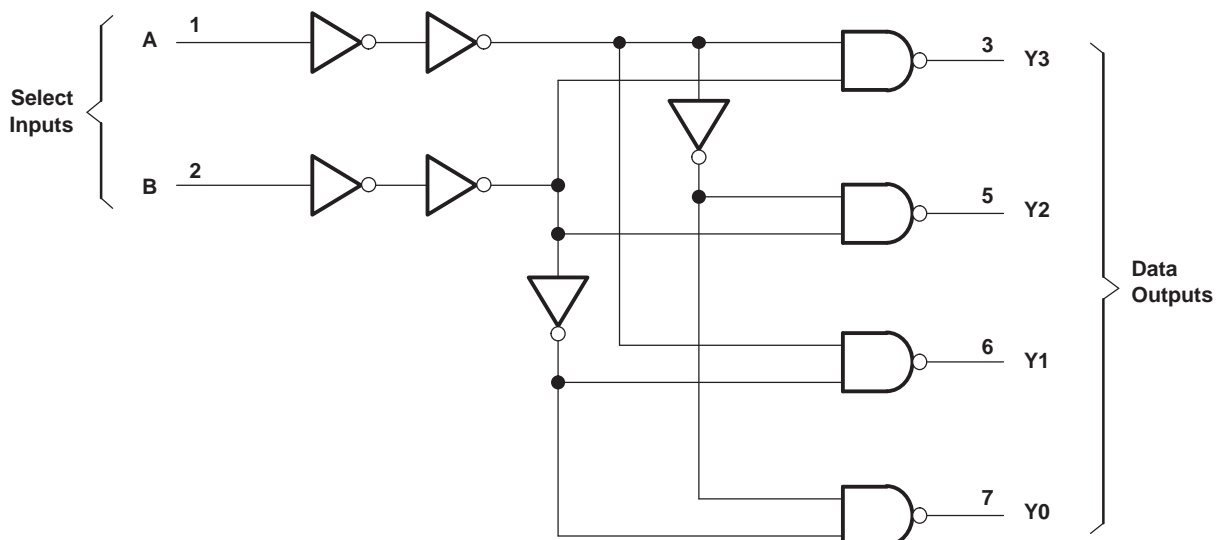


Table of Contents

| | |
|---|--|
| 1 Features 1 2 Applications 1 3 Description 1 4 Revision History 2 5 Pin Configuration and Functions 3 6 Specification 3 6.1 Absolute Maximum Ratings 3 6.2 ESD Ratings 4 6.3 Recommended Operating Conditions 4 6.4 Thermal Information 5 6.5 Electrical Characteristics 5 6.6 Switching Characteristics 5 6.7 Operating Characteristics 5 6.8 Typical Characteristics 6 7 Parameter Measurement Information 7 8 Detailed Description 9 8.1 Overview 9 | 8.2 Functional Block Diagram 9 8.3 Feature Description 9 8.4 Device Functional Modes 9 9 Application and Implementation 10 9.1 Application Information 10 9.2 Typical Application 10 10 Power Supply Recommendations 11 11 Layout 11 11.1 Layout Guidelines 11 11.2 Layout Example 11 12 Device and Documentation Support 12 12.1 Documentation Support 12 12.2 Community Resources 12 12.3 Trademarks 12 12.4 Electrostatic Discharge Caution 12 12.5 Glossary 12 13 Mechanical, Packaging, and Orderable Information 12 |
|---|--|

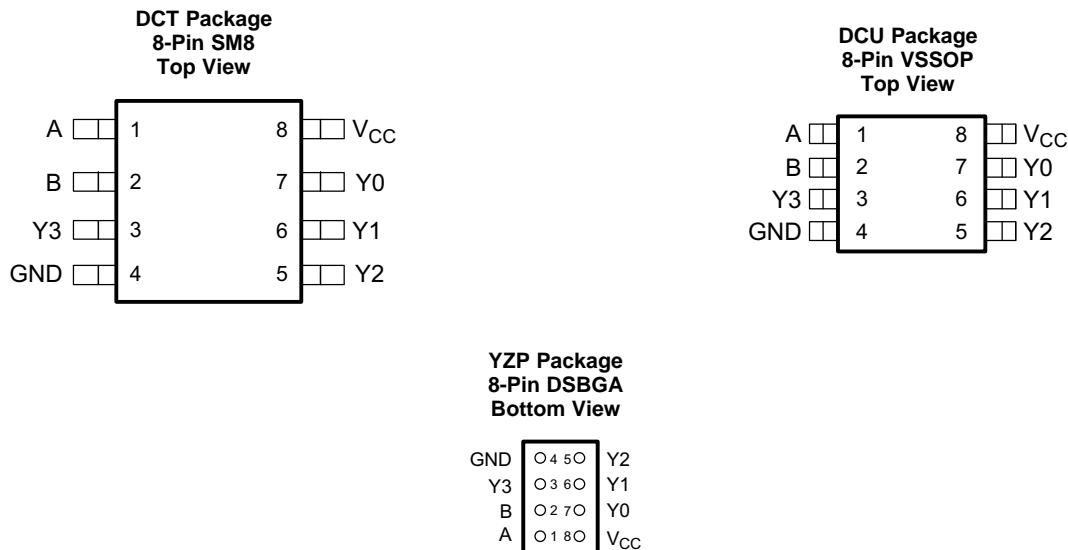
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (December 2005) to Revision D | Page |
|---|------|
| <ul style="list-style-type: none"> • Added <i>Applications</i> section, <i>Device Information</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section 1 | 1 |

| Changes from Revision B (December 2005) to Revision C | Page |
|--|------|
| <ul style="list-style-type: none"> • Updated document to new TI data sheet format 1 • Updated <i>Features</i> 1 • Removed <i>Ordering Information</i> table 1 | 1 |

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|-----|-----|--|
| NAME | NO. | | |
| A | 1 | I | Address input, bit 0 |
| B | 2 | I | Address input, bit 1 |
| Y ₃ | 3 | O | Output 3, low when B is high and A is high |
| GND | 4 | — | Ground |
| Y ₂ | 5 | O | Output 2, low when B is high and A is low |
| Y ₁ | 6 | O | Output 1, low when B is low and A is high |
| Y ₀ | 7 | O | Output 0, low when B is low and A is low |
| V _{CC} | 8 | — | Power pin |

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|--------------------|-----------------------|------|----|
| V _{CC} | Supply voltage | -0.5 | 6.5 | V | |
| V _I | Input voltage | -0.5 | 6.5 | V | |
| V _O | Voltage applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V | |
| V _O | Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾ | -0.5 | V _{CC} + 0.5 | V | |
| I _{IK} | Input clamp current | V _I < 0 | | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | -50 | mA |
| I _O | Continuous output current | | | ±50 | mA |
| I _{CC} | Continuous current through V _{CC} or GND | | | ±100 | mA |
| T _J | Junction temperature | | | 150 | °C |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

| | | VALUE | UNIT |
|-------------------------------------|--|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |
| | Machine model | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|--|----------------------|----------------------|------|
| V_{CC} Supply voltage | Operating | 1.65 | 5.5 | V |
| | Data retention only | 1.5 | | |
| V_{IH} High-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | | |
| | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 2 | | |
| | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $0.7 \times V_{CC}$ | | |
| V_{IL} Low-level input voltage | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | | $0.35 \times V_{CC}$ | V |
| | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | | 0.7 | |
| | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | | 0.8 | |
| | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | | $0.3 \times V_{CC}$ | |
| V_I Input voltage | | 0 | 5.5 | V |
| V_O Output voltage | | 0 | V_{CC} | V |
| I_{OH} High-level output current | $V_{CC} = 1.65\text{ V}$ | | –4 | mA |
| | $V_{CC} = 2.3\text{ V}$ | | –8 | |
| | $V_{CC} = 3\text{ V}$ | | –16 | |
| | $V_{CC} = 4.5\text{ V}$ | | –24 | |
| I_{OL} Low-level output current | $V_{CC} = 1.65\text{ V}$ | | 4 | mA |
| | $V_{CC} = 2.3\text{ V}$ | | 8 | |
| | $V_{CC} = 3\text{ V}$ | | 16 | |
| | $V_{CC} = 4.5\text{ V}$ | | 24 | |
| $\Delta t/\Delta v$ Input transition rise or fall rate | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$ | | 20 | ns/V |
| | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | 15 | |
| | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | | 10 | |
| T_A Operating free-air temperature | | –40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LVC1G139 | | | UNIT |
|-------------------------------|--|--------------|-------------|-------------|------|
| | | DCT (SM8) | DCU (VSSOP) | YZP (DSBGA) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 194 | 195 | 106 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 124 | 74 | 1.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 106 | 74 | 11 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 48 | 6.7 | 3.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 105 | 73 | 11 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | — | — | — | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = -100 μA | 1.65 V to 5.5 V | V _{CC} - 0.1 | | | V |
| | I _{OH} = -4 mA | 1.65 V | 1.2 | | | |
| | I _{OH} = -8 mA | 2.3 V | 1.9 | | | |
| | I _{OH} = -16 mA | 3 V | 2.4 | | | |
| | I _{OH} = -24 mA | | 2.3 | | | |
| | I _{OH} = -32 mA | 4.5 V | 3.8 | | | |
| V _{OL} | I _{OL} = 100 μA | 1.65 V to 5.5 V | | | 0.1 | V |
| | I _{OL} = 4 mA | 1.65 V | | | 0.45 | |
| | I _{OL} = 8 mA | 2.3 V | | | 0.3 | |
| | I _{OL} = 16 mA | 3 V | | | 0.4 | |
| | I _{OL} = 24 mA | | | | 0.55 | |
| | I _{OL} = 32 mA | 4.5 V | | | 0.55 | |
| I _I | A or B inputs V _I = 5.5 V or GND | 0 to 5.5 V | | | ±1 | μA |
| I _{off} | V _I or V _O = 5.5 V | 0 | | | ±5 | μA |
| I _{CC} | V _I = 5.5 V or GND, I _O = 0 | 1.65 V to 5.5 V | | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | 3 V to 5.5 V | | | 500 | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | 4 | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

6.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 5 V ± 0.5 V | | UNIT |
|-----------------|--------------|-------------|------------------------------|----------------------------------|------|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | See Figure 2 | 2.7 | 15.3 | 1.5 | 7.5 | 0.9 | 4.9 | 0.8 | 3.6 | ns |
| | | | See Figure 3 | 3 | 16.7 | 1.6 | 8.2 | 1.2 | 5.9 | 1.1 | 4.2 | |

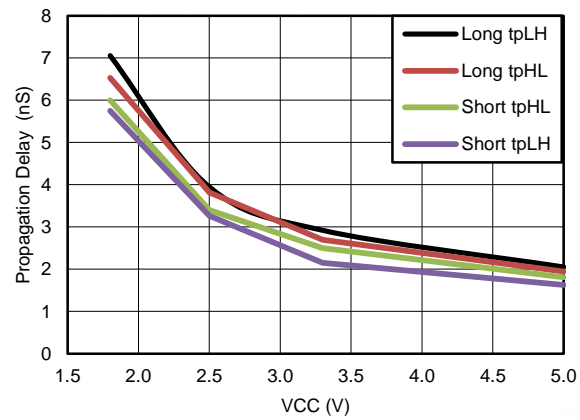
6.7 Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | V _{CC} = 5 V | UNIT |
|--------------------------------|-----------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C _{pd} ⁽¹⁾ | f = 10 MHz | 31 | 34 | 36 | 39 | pF |

(1) Two outputs switching.

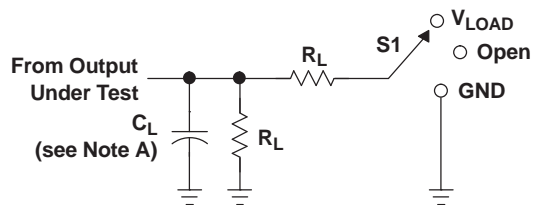
6.8 Typical Characteristics



Short is 2 inverter path; Long is 3 inverter path.

Figure 1. Propagation Delay vs. VCC

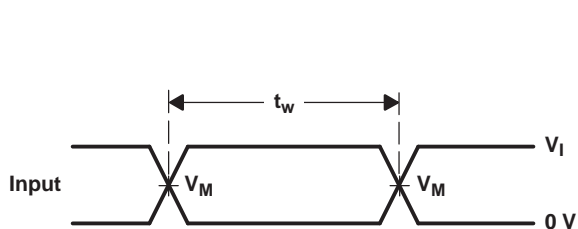
7 Parameter Measurement Information



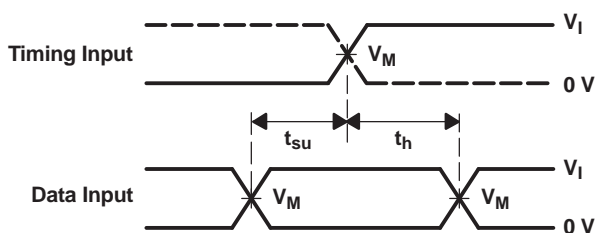
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

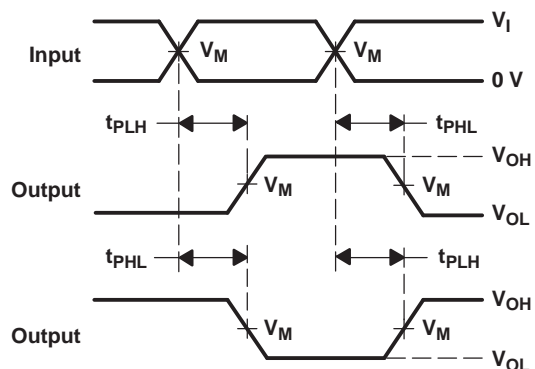
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



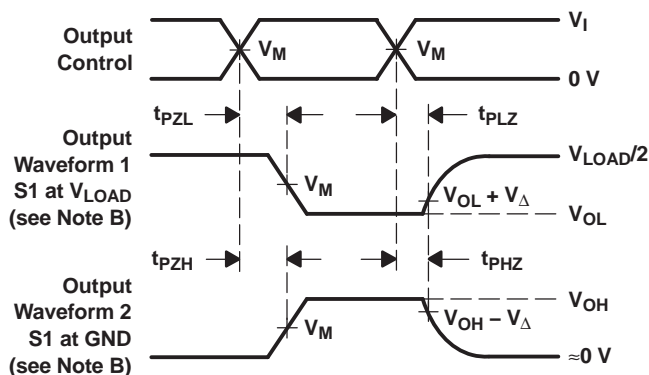
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

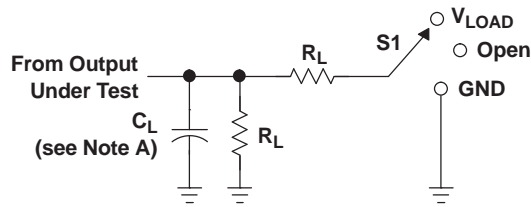


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

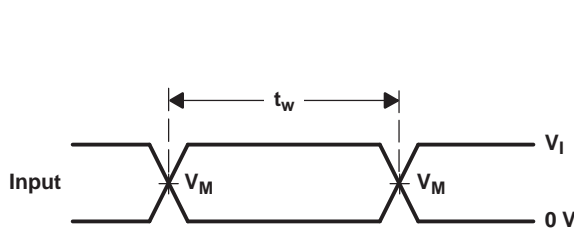
Parameter Measurement Information (continued)



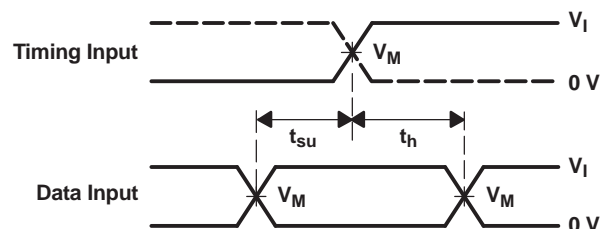
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

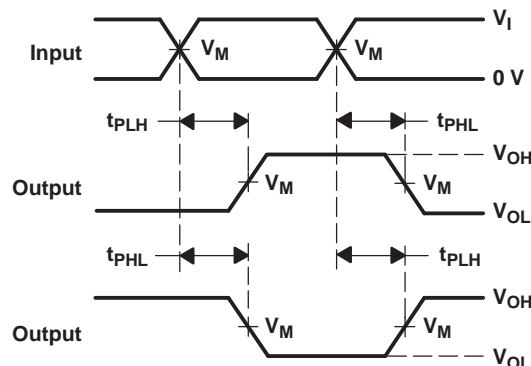
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



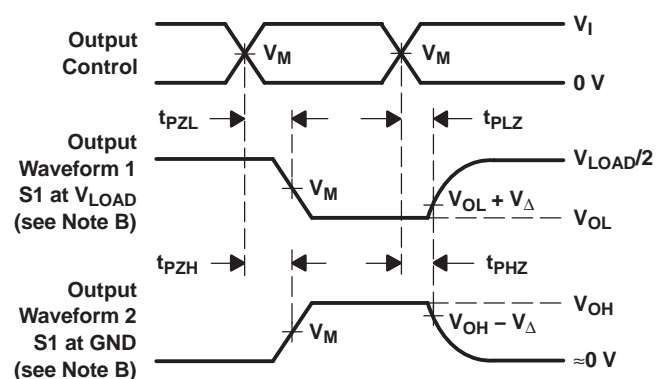
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

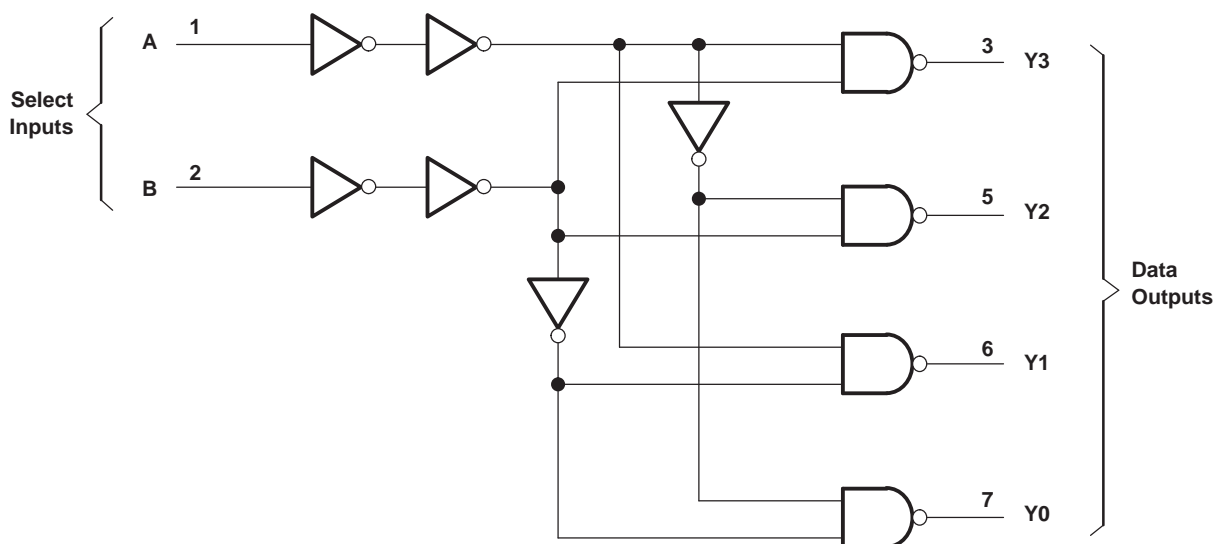
Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The LVC1G139 decodes the 2-bit input to one of the four outputs. The B input is the most significant bit and the Y outputs are active low. The propagation delays are very short and well matched (see Figure 1). Supply voltage from 1.65-V to 5.5-V is supported.

8.2 Functional Block Diagram



8.3 Feature Description

NanoStar and NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1G139.

Table 1. Function Table

| INPUTS | | OUTPUTS | | | |
|--------|---|----------------|----------------|----------------|----------------|
| B | A | Y ₀ | Y ₁ | Y ₂ | Y ₃ |
| L | L | L | H | H | H |
| L | H | H | L | H | H |
| H | L | H | H | L | H |
| H | H | H | H | H | L |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC1G139 device is a 2-of-4 decoder and demultiplexer. This device decodes the 2-bit address on inputs A (bit 0) and B (bit 1) then provides a logic low on the matching address output. It can produce 24 mA of drive current at 3.3 V, making it ideal for driving multiple outputs.

9.2 Typical Application

This is an address line decoder using a 16-bit bus example; address bus lines 14 and 15 are decoded and drive four active low chip selects. Each output covers 16k address space mapped by the address bus lines 0 through 13.

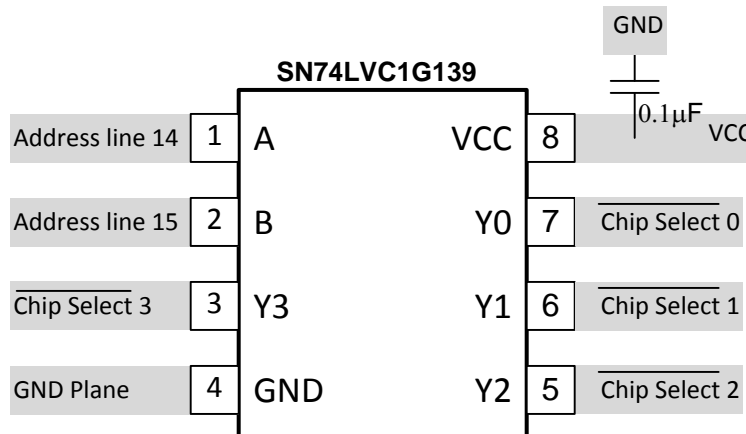


Figure 4. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see ($\Delta t/\Delta V$) in [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see (V_{IH} and V_{IL}) in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions:
 - Load currents should not exceed 50 mA per output and 100 mA total for the part.
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

Typical Application (continued)

9.2.3 Application Curve

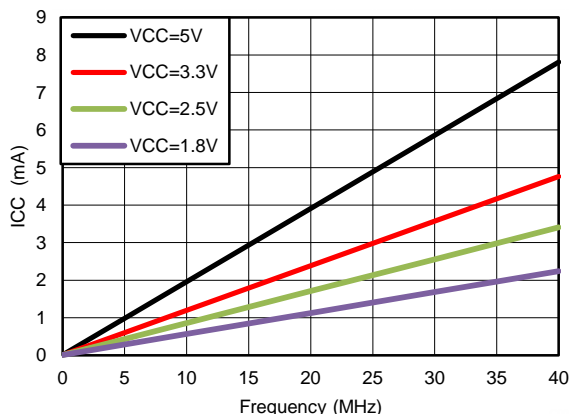


Figure 5. I_{CC} vs Frequency
Load is 15 pF

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

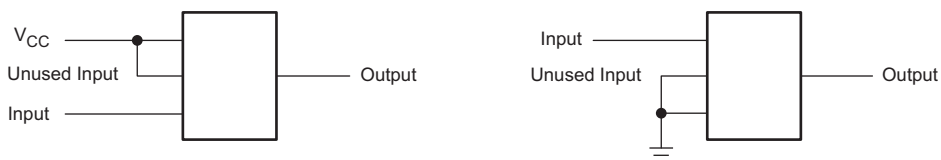


Figure 6. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

Implications of Slow or Floating CMOS Inputs, [SCBA004](#)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

NanoStar, NanoFree, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| 74LVC1G139DCTRE4 | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C39 Z | Samples |
| 74LVC1G139DCTTE4 | ACTIVE | SM8 | DCT | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C39 Z | Samples |
| 74LVC1G139DCURE4 | ACTIVE | VSSOP | DCU | 8 | | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| 74LVC1G139DCUTG4 | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C39R | Samples |
| SN74LVC1G139DCTR | ACTIVE | SM8 | DCT | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C39 Z | Samples |
| SN74LVC1G139DCTT | ACTIVE | SM8 | DCT | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | C39 Z | Samples |
| SN74LVC1G139DCUR | ACTIVE | VSSOP | DCU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C39Q ~ C39R) | Samples |
| SN74LVC1G139DCUT | ACTIVE | VSSOP | DCU | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 85 | (C39Q ~ C39R) | Samples |
| SN74LVC1G139YZPR | ACTIVE | DSBGA | YZP | 8 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | DFN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| 74LVC1G139DCUTG4 | VSSOP | DCU | 8 | 250 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC1G139DCTR | SM8 | DCT | 8 | 3000 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC1G139DCTT | SM8 | DCT | 8 | 250 | 180.0 | 13.0 | 3.35 | 4.5 | 1.55 | 4.0 | 12.0 | Q3 |
| SN74LVC1G139DCUR | VSSOP | DCU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC1G139DCUR | VSSOP | DCU | 8 | 3000 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC1G139DCUT | VSSOP | DCU | 8 | 250 | 178.0 | 9.5 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| SN74LVC1G139YZPR | DSBGA | YZP | 8 | 3000 | 178.0 | 9.2 | 1.02 | 2.02 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| 74LVC1G139DCUTG4 | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G139DCTR | SM8 | DCT | 8 | 3000 | 182.0 | 182.0 | 20.0 |
| SN74LVC1G139DCTT | SM8 | DCT | 8 | 250 | 182.0 | 182.0 | 20.0 |
| SN74LVC1G139DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G139DCUR | VSSOP | DCU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G139DCUT | VSSOP | DCU | 8 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G139YZPR | DSBGA | YZP | 8 | 3000 | 220.0 | 220.0 | 35.0 |

DCT (R-PDSO-G8)

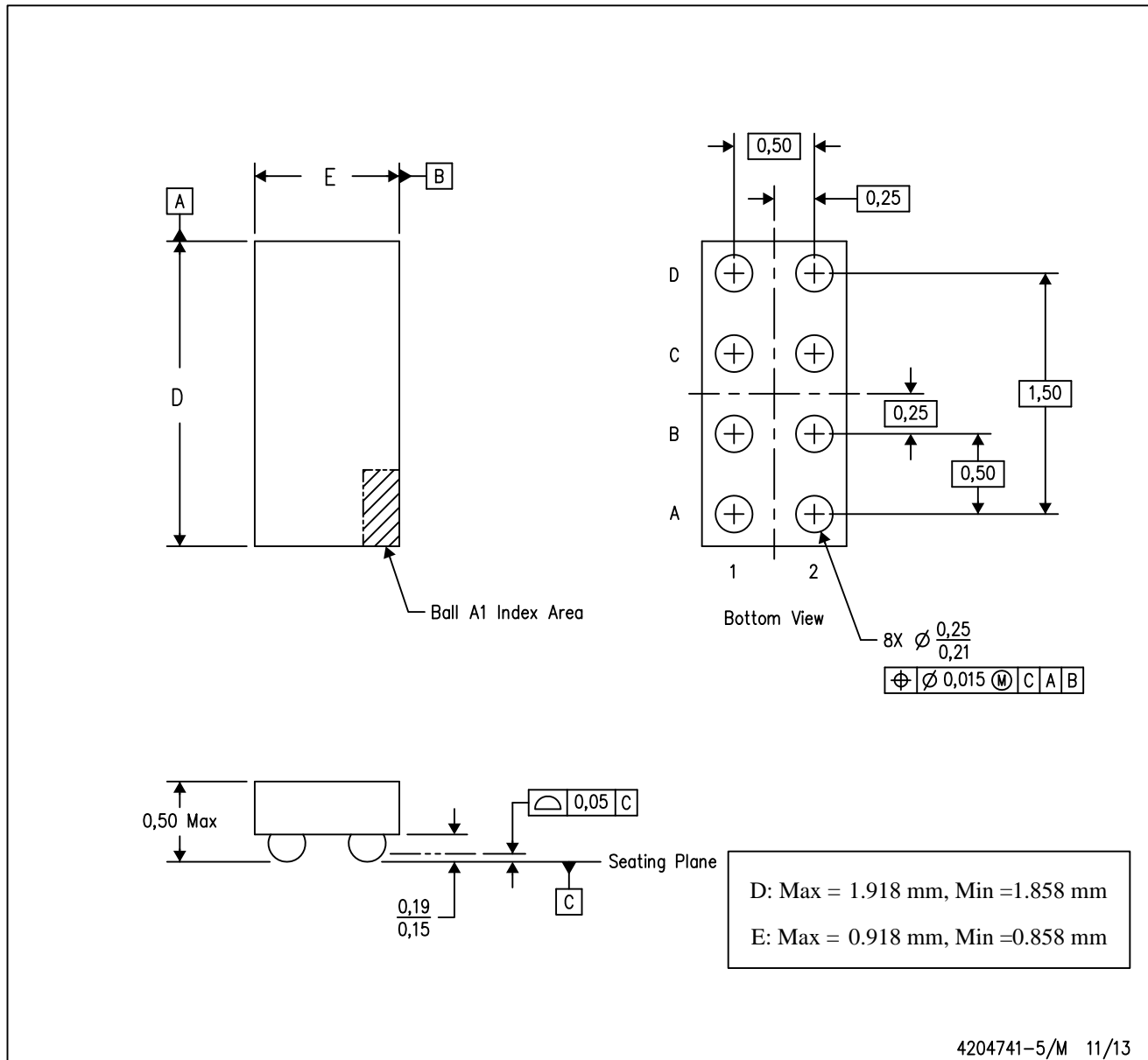
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated