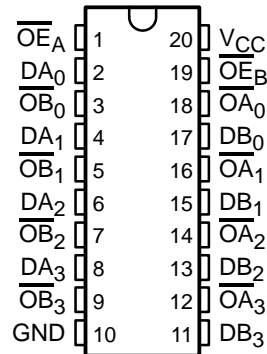


# CY74FCT2240T 8-BIT BUFFER/LINE DRIVER WITH 3-STATE OUTPUTS

SCCS036A – SEPTEMBER 1994 – REVISED OCTOBER 2001

- Function and Pinout Compatible With FCT and F Logic
- 25-Ω Output Series Resistors Reduce Transmission-Line Reflection Noise
- TTL-Output-Level Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Fully Compatible With TTL Input and Output Logic Levels
- 12-mA Output Sink Current  
15-mA Output Source Current
- 3-State Outputs

Q OR SO PACKAGE  
(TOP VIEW)



## description

The CY74FCT2240T is an octal buffer and line driver that includes on-chip 25-Ω terminating resistors at each of the outputs to minimize noise resulting from reflections or standing waves in high-performance applications. The on-chip resistors reduce overall board space and component count. Designed to be employed as a memory address driver, clock driver, and bus-oriented transmitter/receiver, this device provides speed and drive capabilities commensurate with its fastest bipolar logic counterparts, while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices, without the need for external components.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	4.1	CY74FCT2240CTQCT	FCT2240C
	SOIC – SO	Tube	4.1	CY74FCT2240CTSOC	FCT2240C
		Tape and reel	4.1	CY74FCT2240CTSOCT	
	QSOP – Q	Tape and reel	4.8	CY74FCT2240ATQCT	FCT2240A
	SOIC – SO	Tube	8	CY74FCT2240TSOC	FCT2240
		Tape and reel	8	CY74FCT2240TSOCT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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**CY74FCT2240T**  
**8-BIT BUFFER/LINE DRIVER**  
**WITH 3-STATE OUTPUTS**

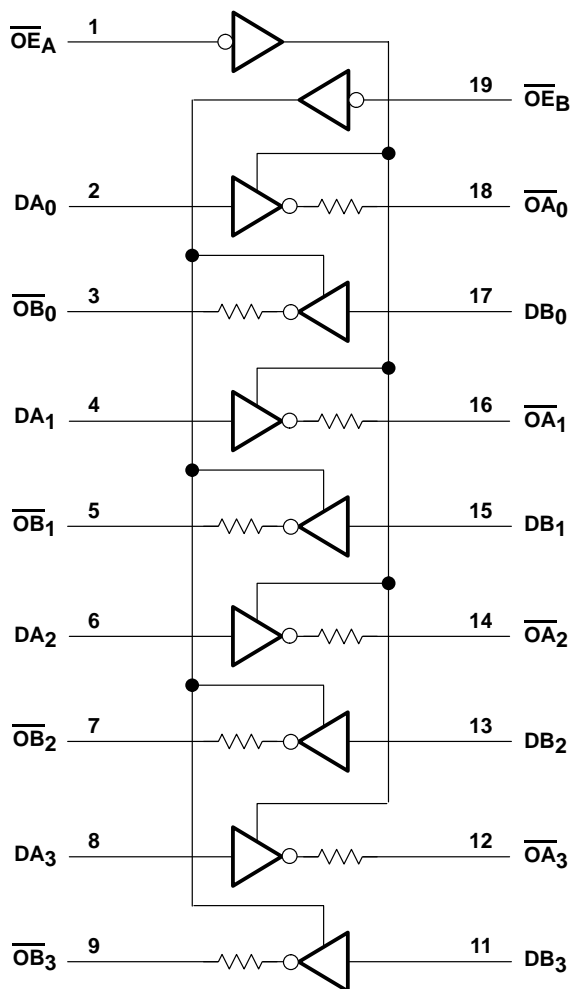
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**FUNCTION TABLE**

INPUTS			OUTPUT
$\overline{OE}_A$	$\overline{OE}_B$	D	$\overline{O}$
L	L	L	H
L	L	H	L
H	H	X	Z

H = High logic level, L = Low logic level,  
 X = Don't care, Z = High-impedance (off)  
 state

**logic diagram**



**CY74FCT2240T**  
**8-BIT BUFFER/LINE DRIVER**  
**WITH 3-STATE OUTPUTS**

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential .....	–0.5 V to 7 V
DC input voltage range .....	–0.5 V to 7 V
DC output voltage range .....	–0.5 V to 7 V
DC output current (maximum sink current/pin) .....	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package .....	68°C/W
SO package .....	58°C/W
Ambient temperature range with power applied, $T_A$ .....	–65°C to +135°C
Storage temperature range, $T_{stg}$ .....	–65°C to +150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 2)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			–15	mA
$I_{OL}$ Low-level output current			12	mA
$T_A$ Operating free-air temperature	–40		85	°C

NOTE 2: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



# CY74FCT2240T

## 8-BIT BUFFER/LINE DRIVER

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -15\text{ mA}$	2.4	3.3		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 12\text{ mA}$		0.3	0.55	V
$R_{OUT}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 12\text{ mA}$	20	25	40	$\Omega$
$V_{hys}$	All inputs			0.2		V
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = V_{CC}$			5	$\mu\text{A}$
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 2.7\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 2.7\text{ V}$			10	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0.5\text{ V}$			-10	$\mu\text{A}$
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA
$I_{off}$	$V_{CC} = 0\text{ V}$ ,	$V_{OUT} = 4.5\text{ V}$			$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.1	0.2	mA
$\Delta I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open			0.5	2	mA
$I_{CCD}^\parallel$	$V_{CC} = 5.25\text{ V}$ , One input switching at 50% duty cycle, Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz
$I_C^\#$	$V_{CC} = 5.25\text{ V}$ , Outputs open, $\overline{OE}_A = \overline{OE}_B = \text{GND}$	One bit switching at $f_1 = 10\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	0.7	1.4	mA
			$V_{IN} = 3.4\text{ V}$ or GND	1	2.4	
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$	1.3	2.6	
			$V_{IN} = 3.4\text{ V}$ or GND	3.3	10.6	
$C_i$				5	10	pF
$C_o$				9	12	pF

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_C$  formula.



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**switching characteristics over operating free-air temperature range (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT2240T		CY74FCT2240AT		CY74FCT2240CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	D	$\bar{O}$	1.5	8	1.5	4.8	1.5	4.1	ns
t <sub>PHL</sub>			1.5	8	1.5	4.8	1.5	4.1	
t <sub>PZH</sub>	$\bar{OE}$	$\bar{O}$	1.5	10	1.5	6.5	1.5	5.8	ns
t <sub>PZL</sub>			1.5	10	1.5	6.5	1.5	5.8	
t <sub>PHZ</sub>	$\bar{OE}$	$\bar{O}$	1.5	9.5	1.5	5.9	1.5	5.2	ns
t <sub>PLZ</sub>			1.5	9.5	1.5	5.9	1.5	5.2	



**CY74FCT2240T**  
**8-BIT BUFFER/LINE DRIVER**  
**WITH 3-STATE OUTPUTS**

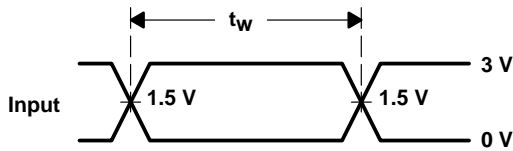
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**PARAMETER MEASUREMENT INFORMATION**



**LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS**

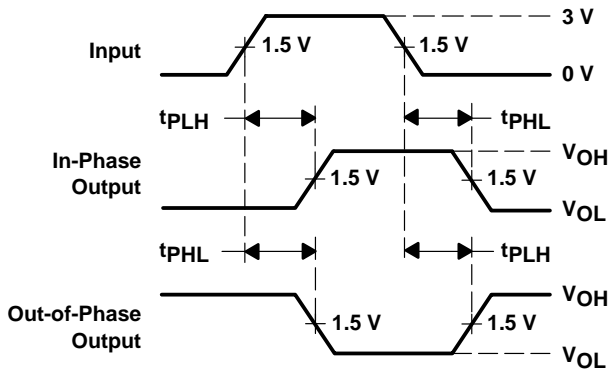
**LOAD CIRCUIT FOR 3-STATE OUTPUTS**



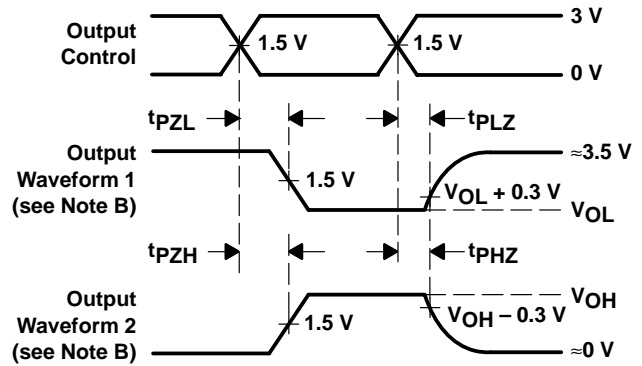
**VOLTAGE WAVEFORMS PULSE DURATION**



**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74FCT2240CTSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2240CTSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2244ATSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2244ATSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
74FCT2244CTSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT2244CTSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2240ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	20		TBD	Call TI	Call TI
CY74FCT2240ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	20		TBD	Call TI	Call TI
CY74FCT2240CTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2240CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2240CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2240CTSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2240CTSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2240TSOCE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2240TSOCG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2240TSOCTE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2240TSOCTG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
CY74FCT2244ATQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244ATQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244ATQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244ATSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244ATSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244ATSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244CTQCT	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244CTQCTE4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244CTQCTG4	ACTIVE	SSOP/QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244CTSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244CTSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244CTSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CY74FCT2244CTSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TQCT	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244TQCTE4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244TQCTG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
CY74FCT2244TSOC	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TSOCE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TSOCG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TSOCT	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TSOCTE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT2244TSOCTG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT2240CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2244ATQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2244CTQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2244CTSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CY74FCT2244TQCT	SSOP/QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CY74FCT2244TSOCT	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

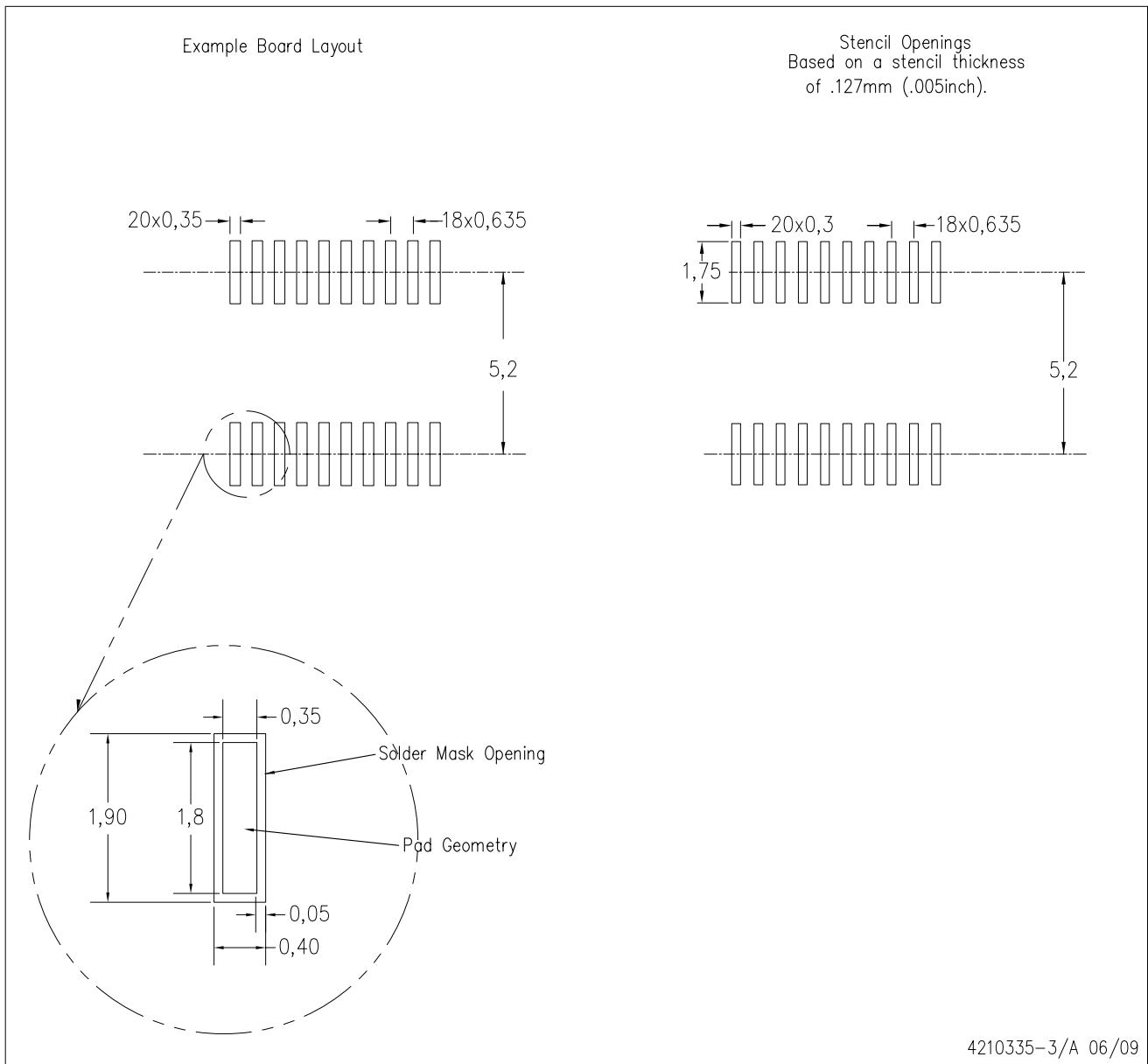
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT2240CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2244ATQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2244CTQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2244CTSOCT	SOIC	DW	20	2000	346.0	346.0	41.0
CY74FCT2244TQCT	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
CY74FCT2244TSOCT	SOIC	DW	20	2000	346.0	346.0	41.0



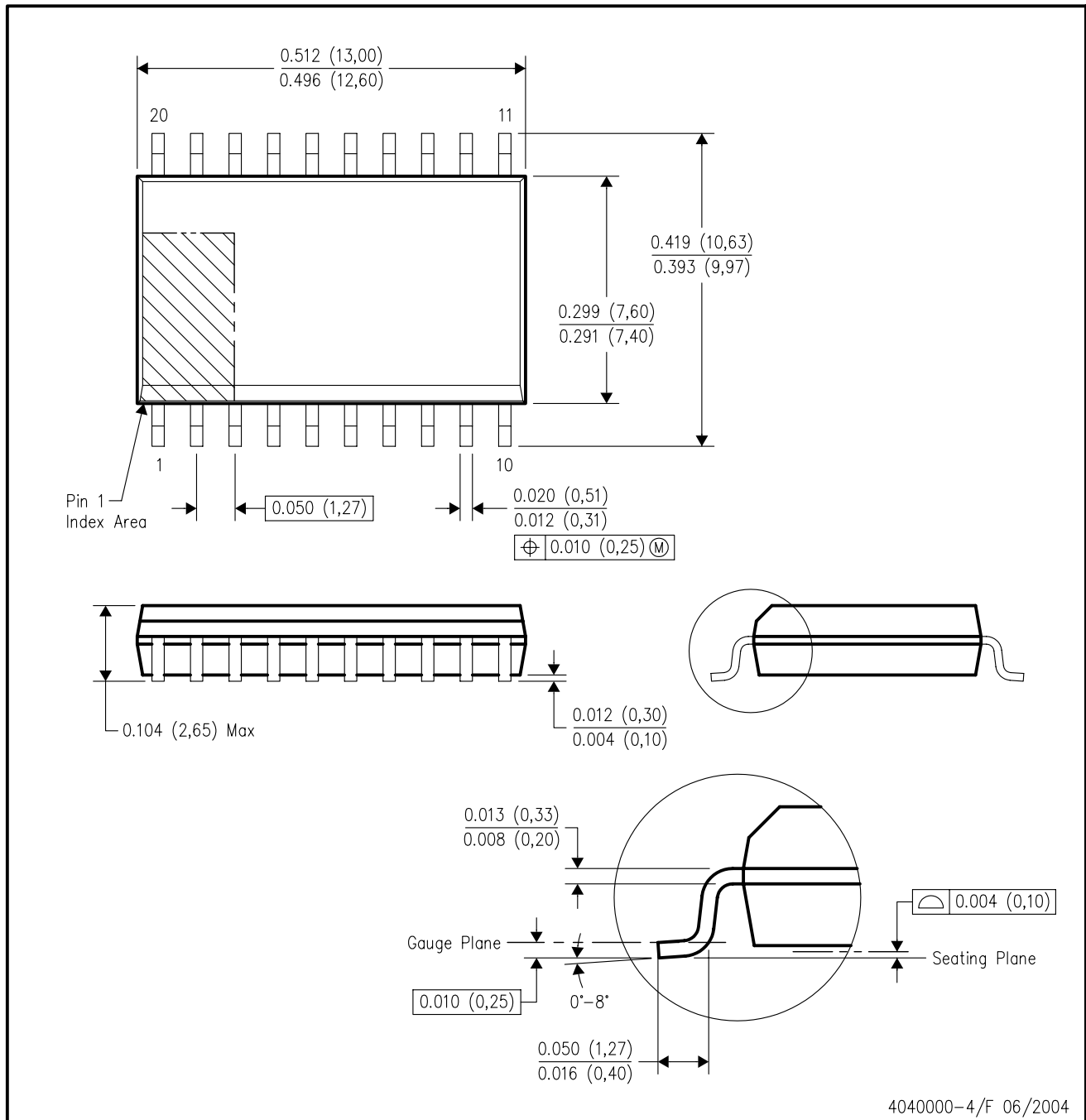
DBQ (R-PDSO-G20)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

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