73S8024C
Smart Card Interface

Simplifying System Integration™

DATA SHEET

ISO/IEC 7816-3

April 2009

DESCRIPTION

The Teridian 73S8024C is a single smart card interface IC. It provides full electrical compliance with ISO-7816-3, EMV 4.0 and NDS specifications[1].

Interfacing with the system controller is done through the control bus, composed of digital inputs to control the interface, and one interrupt output to inform the system controller of the card presence and faults. Data exchange with the card is managed from the system controller using the I/O line (and eventually the auxiliary I/O lines). Hardware support for auxiliary I/O lines, C4 / C8 contacts, is provided.

The card clock signal can be generated by an on-chip oscillator using an external crystal or by connection to a clock signal coming from the system controller.

The Teridian 73S8024C device incorporates an ISO-7816-3 activation/deactivation sequencer that controls the card signals. Level shifters drive the card signals with the selected card voltage (3 V or 5 V), coming from an internal DC-DC converter.

With its high-efficiency DC-DC converter, the Teridian 73S8024C is a cost-effective solution for any smart card reader application to be powered from a single 2.7 V to 3.6 V power supply.

Emergency card deactivation is initiated upon card extraction or upon any fault generated by the protection circuitry. The fault can be a V_{DD} (digital power supply) or a V_{CC} (card power supply) failure, a card over-current, or an over-heating fault.

ADVANTAGES

- The only smart card interface IC firmware compatible with the TDA8004 operating with a single 2.7 V to 3.6 V power supply (allows removal of 5 V from the system)
- The inductor-based DC-DC converter provides higher current and efficiency than the usual charge-pump capacitor-based converters
  - → Ideal for battery-powered applications
  - → Suitable for high current cards and SAMs: (100 mA max)
- Power down mode: 2 µA typical

FEATURES

- **Card Interface:**
  - Complies with ISO-7816-3, EMV 4.0 and NDS[1]
  - A DC-DC Converter provides 3V / 5V to the card from an external power supply input
  - High-efficiency converter: > 80% @ V_{DD}=3.3 V, V_{CC}=5 V and I_{CC} = 65 mA
  - Up to 100 mA supplied to the card
  - ISO-7816-3 Activation / Deactivation sequencer with emergency automated deactivation on card removal or fault detected by the protection circuitry
  - Protection includes 2 voltage supervisors which detect voltage drops on card V_{CC} and on V_{DD} power supplies
  - The V_{DD} voltage supervisor threshold value can be externally adjusted
  - True over-current detection (150 mA max.)
  - 2 card detection inputs, 1 for each possible user polarity
  - Auxiliary I/O lines, for C4/C8 contact signals
  - Card clock up to 20 MHz
- **System Controller Interface:**
  - 3 Digital inputs control the card activation / deactivation, card reset and card voltage
  - 4 Digital inputs control the card clock (division rate and card clock stop modes)
  - 1 Digital output, interrupt to the system controller, allows the system controller to monitor the card presence and faults.
  - Crystal oscillator or host clock, up to 27 MHz
- **Power Supply: V_{DD} 2.7 V to 3.6 V**
- **Power Down mode**
- **6 kV ESD Protection on the card interface**
- **Package: SO28**

APPLICATIONS

- Set-Top-Boxes , DVD / HDD Recorders
- Point of Sales and Transaction Terminals
- Control Access and Identification

[1] Pending NDS approval.

FUNCTIONAL DIAGRAM

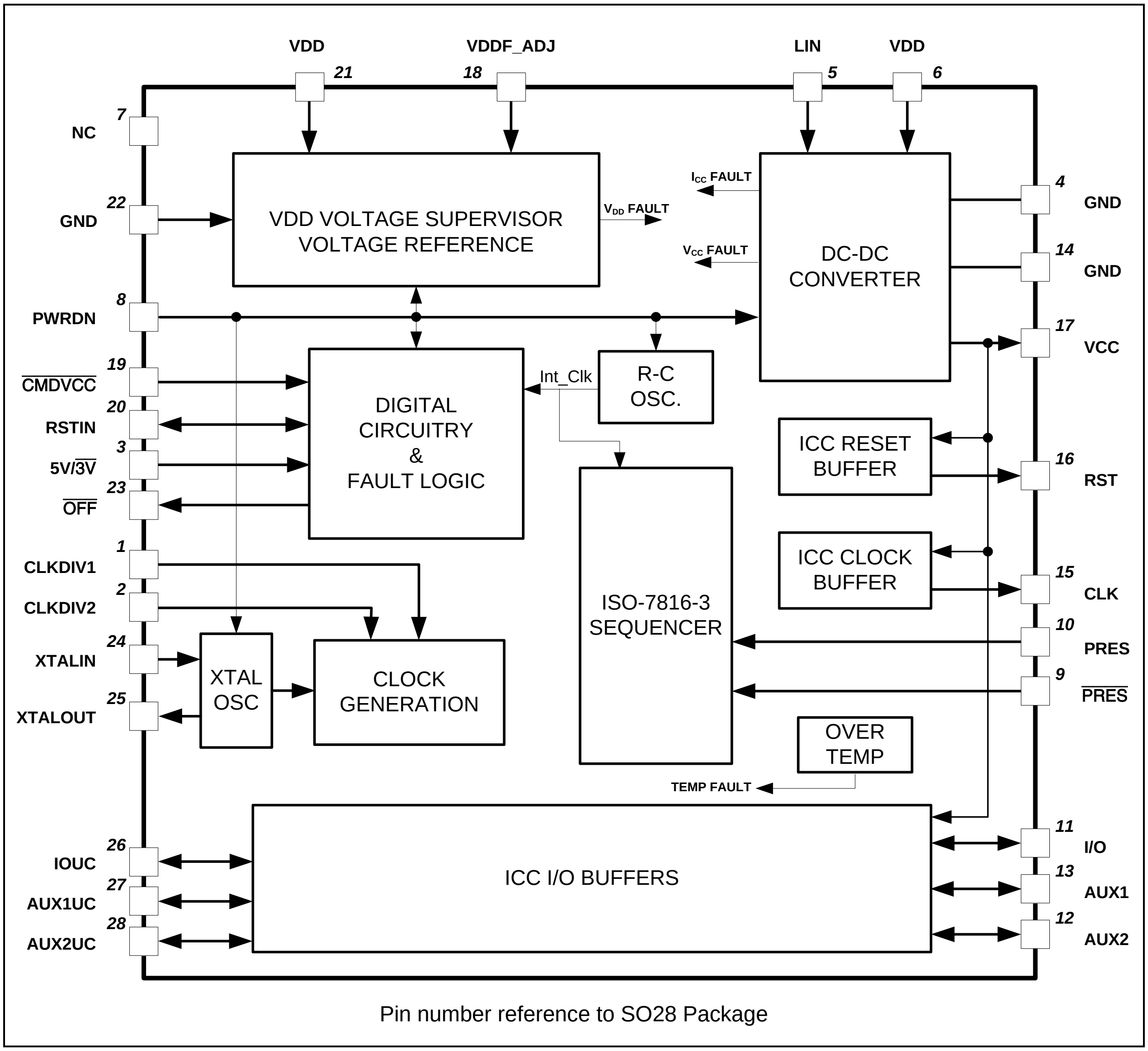


Figure 1: 73S8024C Block Diagram

Table of Contents

Figures

Table

1 Pin Description

1.1 Card Interface

Name	Pin (SO)	Description
IO	11	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX1	13	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX2	12	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
RST	16	Card reset: provides reset (RST) signal to card.
CLK	15	Card clock: provides clock (CLK) signal to card. The rate of this clock is determined by crystal oscillator frequency and CLKDIV selections.
PRES	10	Card Presence switch: active high indicates card is present. Includes a pull-down current source.
$\overline{\text{PRES}}$	9	Card Presence switch: active low indicates card is present. Includes a pull-up current source.
VCC	17	Card power supply: logically controlled by the sequencer, output of DC-DC converter. Requires an external filter capacitor to the card GND.
GND	14	Card ground.

1.2 Miscellaneous Inputs and Outputs

Name	Pin (SO)	Description
XTALIN	24	Crystal oscillator input: can either be connected to crystal or driven as a source for the card clock.
XTALOUT	25	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as an external clock input.
VDDF_ADJ	18	V_{DD} fault threshold adjustment input: this pin can be used to adjust the V_{DDF} value (that controls deactivation of the card). Must be left open if unused.
NC	7	Non-connected pin.

1.3 Power supply and ground

Name	Pin (SO)	Description
VDD	6, 21	System controller interface supply voltage, supply voltage for internal power supply and DC-DC converter power supply source.
GND	4	DC-DC converter ground.
GND	22	Digital ground.
LIN	5	External inductor. Connect external inductor from pin 5 to V_{DD}. Keep the inductor close to pin 5.

1.4 Microcontroller Interface

Name	Pin (SO)	Description
CMDVCC	19	Command V_{CC} (negative assertion): Logic low on this pin causes the DC-DC converter to ramp the V_{CC} supply to the card and initiates a card activation sequence.
5V/$\overline{3V}$	3	5 volt / 3 volt card selection: Logic one selects 5 volts for V_{CC} and card interface, logic low selects 3 volt operation. When the part is to be used with a single card voltage, this pin should be tied to either GND or V_{DD}. However, it includes a high impedance pull-up resistor to default this pin high (selection of 5 V card) when unconnected.
PWRDN	8	Power Down control input (active high): When Power Down (PD) mode is activated; all internal analog functions are disabled to place the 73S8024C in its lowest power consumption mode. The PD mode is allowed only out of a card session (= PWRDN high is not taken into account when CMDVCC = 0). Must be tied to ground when the power down function is not used.
CLKDIV1 CLKDIV2	1 2	Sets the divide ratio from the XTALIN oscillator (or external clock input) to the card clock. These pins include pull-down resistors. CLKDIV1 / CLKDIV2 / Clock Rate: 0 / 0 / XTALIN/8 0 / 1 / XTALIN/4 1 / 1 / XTALIN/2 1 / 0 / XTALIN
OFF	23	Interrupt signal to the processor (active low): Multi-function indicating fault conditions and card presence. Open drain output configuration; it includes an internal 20 kΩ pull-up to $V_{DD.}$
RSTIN	20	Reset Input: This signal is the reset command to the card.
I/OUC	26	System controller data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$
AUX1UC	27	System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$
AUX2UC	28	System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to $V_{DD.}$

Clock rate selection (CLKDIV1, CLKDIV2):

CLKDIV1	CLKDIV2	Clock Rate
0	0	XTALIN/8
0	1	XTALIN/4
1	1	XTALIN/2
1	0	XTALIN

2 System Controller Interface

- 2 digital inputs allow direct control of the card interface from the host as follows:
  - Pin CMDVCC: When low, starts an activation sequence if a card is present.
  - Pin 5V/3V: Defines the card voltage.
- The card I/O and Reset signals have their corresponding controller I/Os to be connected directly to the host:
  - Pin RSTIN: controls the card reset signal (when enabled by the sequencer).
  - Pin I/OUC: data transfer to card I/O contact.
  - Pins AUX1UC and AUX2UC (auxiliary I/O lines associated to the auxiliary I/O lines to be connected to the C4 and C8 card connector contacts).
- 2 digital inputs control the card clock frequency division rate: CLKDIV1 and CLKDIV2 define the card clock frequency, from the input clock frequency (crystal or external clock). The division rate is defined as follows:

CLKDIV2	CLKDIV1	CLK
0	0	⅛ XTAL
0	1	XTAL
1	0	¼ XTAL
1	1	½ XTAL

When the division rate is equal to 1 (CLKDIV2 =0 and CLKDIV1 = 1), the duty-cycle of the card clock depends on the duty-cycle and waveform of the signal applied on the pin XTALIN. When other division rates are used, the 73S8024C circuitry guarantees a duty-cycle in the range 45% to 55%, conforming to ISO-7816-3, EMV 4.0 and NDS specifications.

- Interrupt output to the host: As long as the card is not activated, the OFF pin informs the host about the card presence only (low = no card in the reader). When CMDVCC is set low (Card activation sequence requested from the host), a low level on OFF means a fault has been detected (e.g. card removed during a card session, or voltage fault, or thermal / over-current fault) that automatically initiates a deactivation sequence.
- Power Down: The PWRDN pin is a digital input that allows the host controller to put the 73S8024C in its Power Down state. This pin can only be activated out of a card session.

3 Oscillator

The 73S8024C device has an on-chip oscillator that can generate the smart card clock using an external crystal (connected between the pins XTALIN and XTALOUT) to set the oscillator frequency. When the card clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected.

4 DC-DC Converter – Card Power Supply

An internal DC-DC converter provides the card power supply. This converter is able to provide either 3 V or 5 V card voltage from the power supply applied on the V_{DD} pin. The digital ISO-7816-3 sequencer controls the converter. Card voltage selection is carried out by the digital input 5V/$\overline{\text{3V}}$.

The circuit is an inductive step-up converter/regulator. The external components required are 2 filter capacitors on the power-supply input V_{DD} (next to the LIN pin, 100 nF + 10 µF), an inductor, and an output filter capacitor on the card power supply V_{CC}. The circuit performs regulation by activating the step-up operation when V_{CC} is below a set point of 5.0 or 3.0 volts minus a comparator hysteresis voltage and the input supply V_{DD} is less than the set point for V_{CC}. When V_{DD} is greater than the set point for V_{CC} (V_{DD} = 3.6 V, V_{CC} =3 V) the circuit operates as a linear regulator.

Depending on the inductor values, the voltage converter can provide current on V_{CC} as high as 100 mA. The circuit provides over-current protection and limits I_{CC} to 150 mA. When an over-current condition is sensed, the circuit initiates a deactivation sequence from the control logic and reports back to the host controller a fault on the interrupt output $\overline{\text{OFF}}$.

Choice of the inductor

The nominal inductor value is 10 µH, rated for 400 mA. The inductor is connected between LIN (pin 5 in the SO package, pin 2 in the QFN package) and the V_{DD} voltage. The inductor value can be optimized to meet a particular configuration (I_{CC_MAX}). The inductor should be located on the PCB as close as possible to the LIN pin of the IC.

Choice of the V_{CC} capacitor

Depending on the applications, the requirements in terms of both the V_{CC} minimum voltage and the transient currents that the interface must provide to the card are different. Table 1 shows the recommended capacitors for each V_{CC} power supply configuration and applicable specification.

Table 1: Choice of VCC Pin Capacitor

<table>
<tr><th colspan="3">Specification Requirement</th><th colspan="2">Application</th></tr>
<tr><th>Specification</th><th>Min V_{CC} Voltage Allowed During Transient Current</th><th>Max Transient Current Charge</th><th>Capacitor Type</th><th>Capacitor Value</th></tr>
<tr><td>EMV 4.0</td><td>4.6 V</td><td>30 nAs</td><td rowspan="2">X5R/X7R w/ ESR < 100 mΩ</td><td>3.3 µF</td></tr>
<tr><td>ISO-7816-3</td><td>4.5 V</td><td>20 nAs</td><td>1 µF</td></tr>
</table>

Table 1: Choice of VCC Pin Capacitor

5 Over-temperature Monitor

A built-in detector monitors die temperature. When an over-temperature condition occurs, a card deactivation sequence is initiated, and an error or fault condition is reported to the system controller.

6 Voltage Supervision

Two voltage supervisors constantly check the level of the voltages V_{DD} and V_{CC}. A card deactivation sequence is triggered upon a fault of any of these voltage supervisors.

The digital circuitry is powered by the power supply applied on the VDD pin. V_{DD} also defines the voltage range for the interface with the system controller. The V_{DD} Voltage supervisor is also used to initialize the ISO-7816-3 sequencer at power-on, and also to deactivate the card at power-off or upon a fault. The voltage threshold of the V_{DD} voltage supervisor is internally set by default to 2.3 V nominal. However, it may be desirable, in some applications, to modify this threshold value. The pin VDDF_ADJ (pin 18 in the SO package, pin 17 in the QFN package) is used to connect an external resistor R_{EXT} to ground to raise the V_{DD} fault voltage to another value, V_{DDF}. The resistor value is defined as follows:

$$R_{EXT} = 180\ k\Omega / (V_{DDF} - 2.33)$$

An alternative (more accurate) method of adjusting the V_{DD} fault voltage is to use a resistive network of R3 from the pin to supply and R1 from the pin to ground (see Figure 9). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as R1/(R1+R3) and is calculated as:

$Kx = (2.649 / V_{TH}) - 0.6042$ where V_{TH} is the desired new threshold voltage.

To determine the values of R1 and R3, use the following formulas:

$$R3 = 72000 / Kx \qquad R1 = R3*(Kx / (1 – Kx))$$

Taking the example above, where a V_{DD} fault threshold voltage of 2.7 V is desired, solving for Kx gives:

$\rightarrow$ Kx = (2.649 / 2.7) - 0.6042 = 0.377.

Solving for R3 gives: $\rightarrow$ R3 = 72000 / 0.377 = 191 kΩ.
Solving for R1 gives: $\rightarrow$ R1 = 191000 *(0.377 / (1 – 0.377)) = 115.6 kΩ.

Using standard 1% resistor values gives R3 = 191 kΩ and R1 = 115 kΩ. These values give an equivalent resistance of Kx = 0.376, a 0.3% error.

If the 2.3 V default threshold is used, this pin must be left unconnected.

7 Power Down

A power down function is provided via the PWRDN pin (active high). When activated, the Power Down (PD) mode disables all the internal analog functions, including the card analog interface, the oscillators and the DC-DC converter, to put the 73S8024C in its lowest power consumption mode. PD mode is only allowed in the deactivated condition (out of a card session, when the $\overline{\text{CMDVCC}}$ signal is driven high from the host controller).

The host controller invokes the power down state when it is desirable to save power. The signals PRES and $\overline{\text{PRES}}$ remain functional in PD mode such that a card insertion sets $\overline{\text{OFF}}$ high. The micro-controller must then set PWRDN low and wait for the internal stabilization time prior to starting any card session (prior to turning $\overline{\text{CMDVCC}}$ low).

Resumption of the normal mode occurs at approximately 10 ms (stabilization of the internal oscillators and reset of the circuitry) after PWRDN is set low. No card activation should be invoked during this 10 ms time period. If a card is present, $\overline{\text{OFF}}$ can be used as an indication that the circuit has completed its recovery from the power down state. $\overline{\text{OFF}}$ will go high at the end of the stabilization period. Should $\overline{\text{CMDVCC}}$ go low during PWRDN = 1, or within the 10 ms internal stabilization / reset time, it will not be taken into account and the card interface will remain inactive. Since $\overline{\text{CMDVCC}}$ is taken into account on its edges, it should be toggled high and low again after the 10 ms to activate a card.

Figure 2 illustrates the sequencing of the PD and Normal modes. PWRDN must be connected to GND if the power down function is not used.

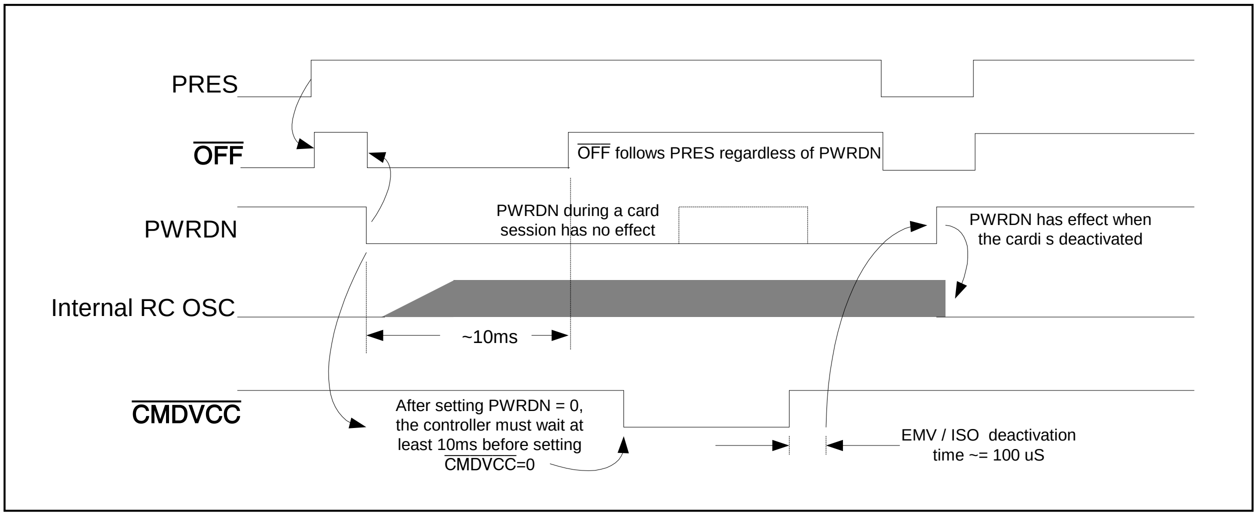


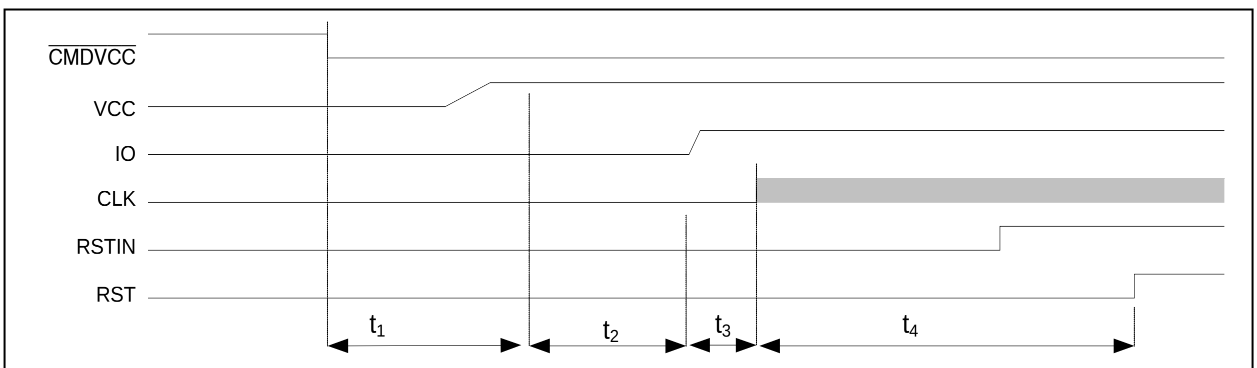
Figure 2: Power Down Mode Operation

8 Activation Sequence

The 73S8024C smart card interface IC has an internal 10 ms delay at power-on reset or upon application of $V_{DD} > V_{DDF}$ or upon exit of Power-Down mode. The card interface may only be activated when $\overline{\text{OFF}}$ is high which indicates a card is present. No activation is allowed at this time. $\overline{\text{CMDVCC}}$ (edge triggered) must then be set low to activate the card.

The following steps and Figure 3 show the activation sequence and the timing of the card control signals when the system controller sets $\overline{\text{CMDVCC}}$ low while the RSTIN is low:

1. $\overline{\text{CMDVCC}}$ is set low.
2. Next, the internal V_{CC} control circuit checks the presence of V_{CC} at the end of t_1. In normal operation, the voltage V_{CC} to the card becomes valid during t_1. If V_{CC} does not become valid, then $\overline{\text{OFF}}$ goes low to report a fault to the system controller, and the power V_{CC} to the card is shut down.
3. Turn I/O (AUX1, AUX2) to reception mode at the end of t_2.
4. Due to the fall of RSTIN, CLK is applied to the card at the end of t_3.
5. RST is a copy of RSTIN after t_4. RSTIN may be set high before t_4, however the sequencer won't set RST high until 42000 clock cycles after the start of CLK.

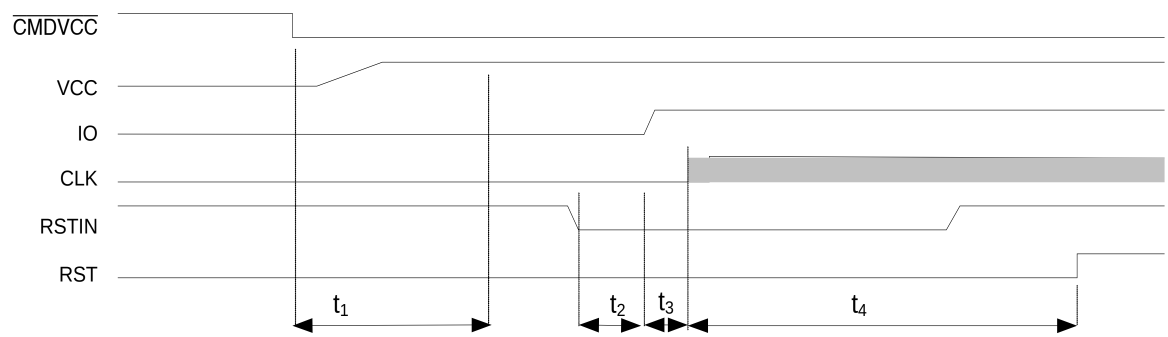


t_1 = 0.510 ms (timing by 1.5 MHz internal Oscillator)
t_2 = 1.5 µs, I/O goes to reception state t_3 = >0.5 µs, CLK starts
$t_4 \geq$ 42000 card clock cycles (time for RST to become the copy of RSTIN)

Figure 3: Activation Sequence – RSTIN low when $\overline{\text{CMDVCC}}$ goes low

The following steps and Figure 4 show the activation sequence and the timing of the card control signals when the system controller pulls $\overline{\text{CMDVCC}}$ low while RSTIN is high:

1. $\overline{\text{CMDVCC}}$ is set low.
2. Next, the internal V_{CC} control circuit checks the presence of V_{CC} at the end of t_1. In normal operation, the voltage V_{CC} to the card becomes valid during this time. If not, $\overline{\text{OFF}}$ goes low to report a fault to the system controller and the V_{CC} power to the card is shut down.
3. After the fall of RSTIN at t_2, turn I/O (AUX1, AUX2) to reception mode.
4. CLK is applied to the card at the end of t_3 after I/O is in reception mode.
5. RST is a copy of RSTIN after t_4. RSTIN may be set high before t_4, however the sequencer will not set RST high until 42,000 clock cycles after the start of CLK.



t_1 = 0.510 ms (timing by 1.5MHz internal Oscillator)
t_2 = 1.5 µs, I/O goes to reception state $t_3 \geq 0.5$ µs, CLK active
$t_4 \geq$ 42000 card clock cycles (time for RST to become the copy of RSTIN).

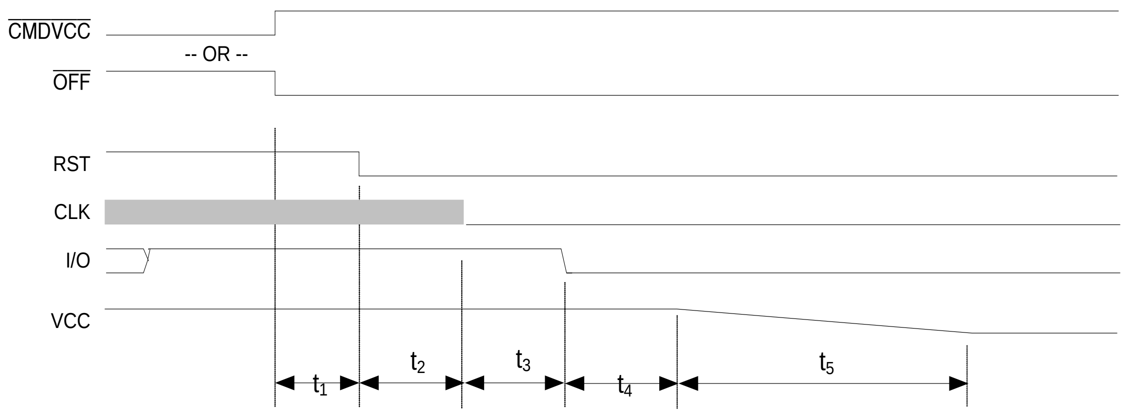
Figure 4: Activation Sequence – RSTIN high when $\overline{\text{CMDVCC}}$ goes low

9 Deactivation Sequence

Deactivation is initiated either by the system controller by setting the $\overline{\text{CMDVCC}}$ high, or automatically in the event of hardware faults. Hardware faults are over-current, overheating, V_{DD} fault, V_{CC} fault, and card extraction during the session.

The following steps and Figure 5 show the deactivation sequence and the timing of the card control signals when the system controller sets the $\overline{\text{CMDVCC}}$ high or $\overline{\text{OFF}}$ goes low due to a fault or card removal:

1. RST goes low at the end of time t_1.
2. CLK is set low at the end of time t_2.
3. I/O goes low at the end of time t_3. Out of reception mode.
4. V_{CC} is turned off at the end of time t_4. After a delay t_5 (discharge of the V_{CC} capacitor), V_{CC} is low.



$t_1 \geq 0.5\ \mu s$, timing by 1.5 MHz internal Oscillator
$t_2 \geq 7.5\ \mu s$ $t_3 \geq 0.5\ \mu s$ $t_4 \geq 0.5\ \mu s$
t_5 = depends on V_{CC} filter capacitor
For NDS application, $C_F = 1\ \mu F$ making $t_1 + t_2 + t_3 + t_4 + t_5 < 100\ \mu s$

Figure 5: Deactivation Sequence

10 $\overline{\text{OFF}}$ and Fault Detection

There are two cases for which the system controller can monitor the $\overline{\text{OFF}}$ signal: to query regarding the card presence outside card sessions, or for fault detection during card sessions.

Monitoring Outside a Card Session

In this condition, $\overline{\text{CMDVCC}}$ is always high, $\overline{\text{OFF}}$ is low if the card is not present, and high if the card is present. Because it is outside a card session, any fault detection will not act upon the $\overline{\text{OFF}}$ signal. No deactivation is required during this time.

Monitoring During a Card Session

$\overline{\text{CMDVCC}}$ is always low, and $\overline{\text{OFF}}$ falls low if the card is extracted or if any fault is detected. At the same time that $\overline{\text{OFF}}$ is set low, the sequencer starts the deactivation process.

Figure 6 shows the timing diagram for the $\overline{\text{CMDVCC}}$, PRES, and $\overline{\text{OFF}}$ signals during a card session and outside the card session.

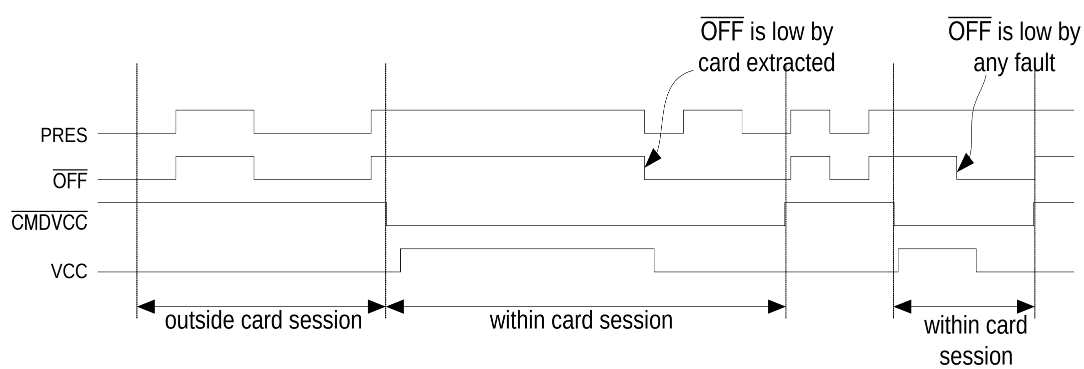


Figure 6: Timing Diagram – Management of the Interrupt Line $\overline{\text{OFF}}$

11 I/O Circuitry and Timing

The I/O, AUX1, and AUX2 pins are in the low state after power on reset and they are in the high state when the activation sequencer turns on the I/O reception state. See Section 8 Activation Sequence for more details on when the I/O reception is on.

The state of the I/OUC, AUX1UC, and AUX2UC is high after power on reset. Within a card session and when the I/O reception state is on, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected, both I/O lines return to their neutral state.

Figure 7 shows the state diagram of how the I/O and I/OUC lines are managed to become input or output. The delay between the I/O signals is shown in Figure 8.

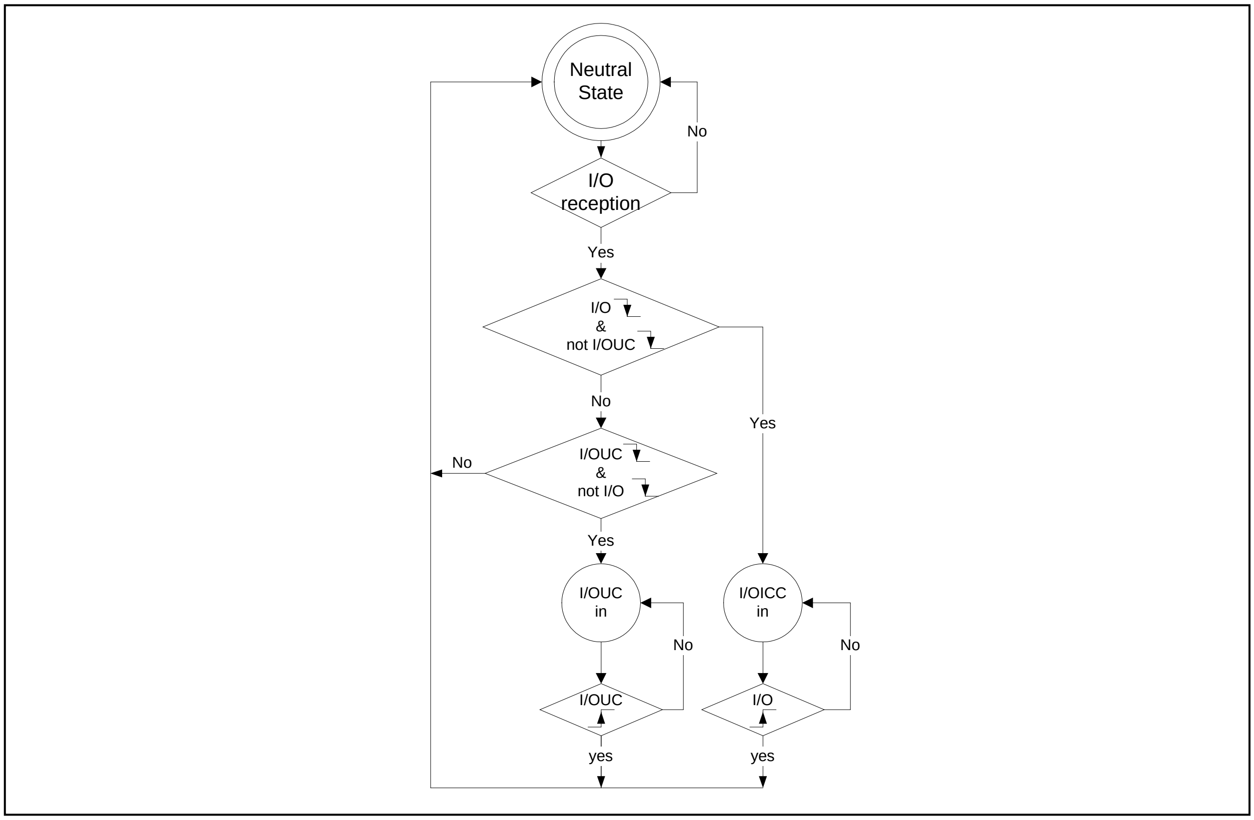


Figure 7: I/O and I/OUC State Diagram

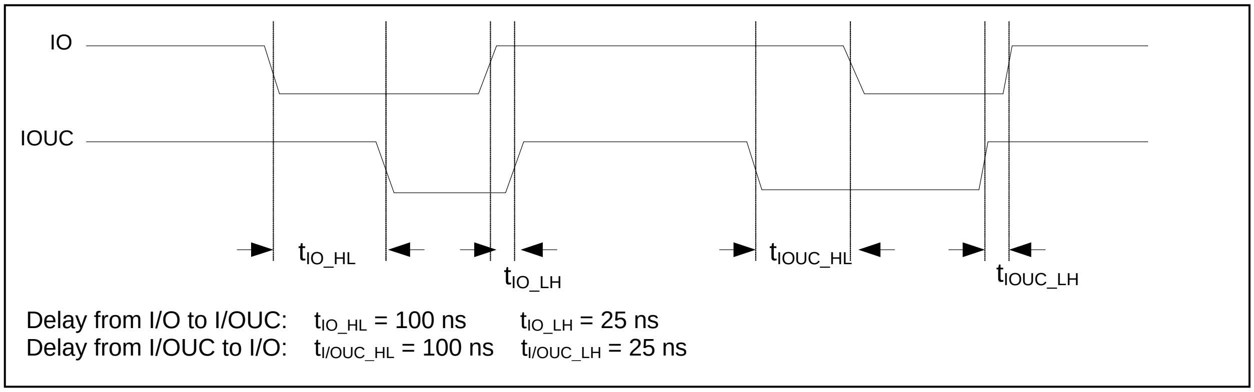


Figure 8: I/O – I/OUC Delays: Timing Diagram

12 Typical Application Schematic

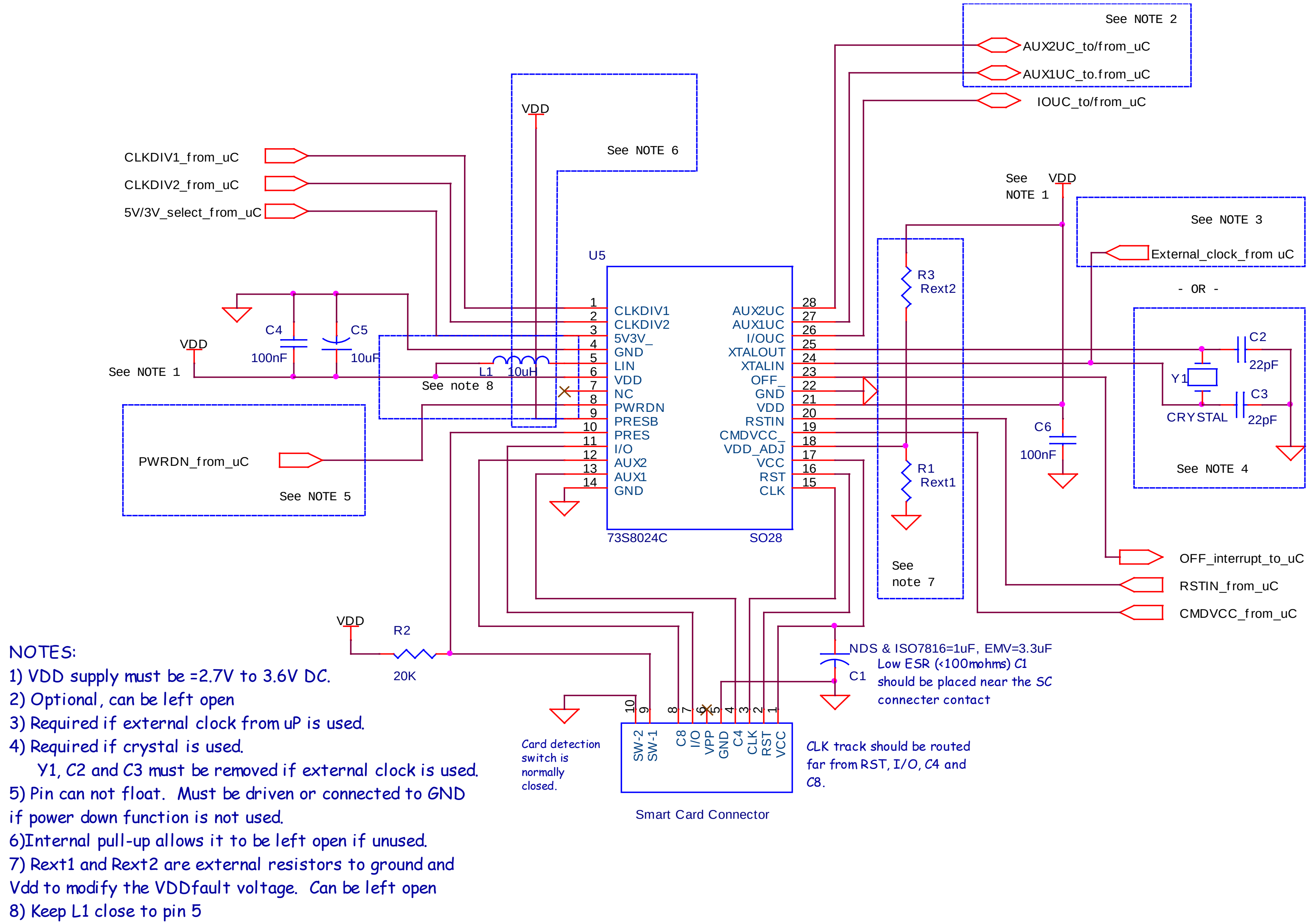


Figure 9: 73S8024C Typical Application Schematic

13 Electrical Specification

13.1 Absolute Maximum Ratings

Operation outside these rating limits may cause permanent damage to the device.

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 °C to 150 °C
Pin Voltage (except LIN and card interface)	-0.3 to (V_{DD} +0.5) VDC
Pin Voltage (LIN)	-0.3 to 6.0 VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD Tolerance – Card interface pins	+/- 6 kV
ESD Tolerance – Other pins	+/- 2 kV

ESD testing on Card pins uses the HBM condition, 3 pulses, each polarity referenced to ground.

13.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 3.6 VDC
Ambient Operating Temperature	-40 °C to +85 °C
Input Voltage for Digital Inputs	0 V to V_{DD} + 0.3 V

13.3 Card Interface Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Card Power Supply (V_{CC}) DC-DC Converter General conditions, -40 °C < T < 85 °C, 2.7 V < V_{DD} < 3.6 V						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode I_{CC} =1 mA	-0.1		0.4	V
		Active mode I_{CC} < 65 mA; 5 V	4.75		5.25	V
		Active mode I_{CC} < 65 mA; 3 V	2.8		3.2	V
		Active mode single pulse of 100 mA for 2 µs; 5 V, fixed load = 25 mA	4.6		5.25	V
		Active mode single pulse of 100 mA for 2 µs; 3 V, fixed load = 25 mA	2.76		3.2	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 5 V	4.6		5.25	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 3 V	2.76		3.2	V
I_{CCmax}	Maximum supply current to the card	Static load current, V_{CC} > 4.6 or 2.7 volts as selected, L=10 µH	100			mA
I_{CCF}	I_{CC} fault current		100	125	180	mA
V_{SR}	V_{CC} slew rate – Rise rate on activate	C_F on V_{CC} = 1 µF	0.05	0.15	0.25	V/µs
V_{SF}	V_{CC} slew rate – Fall rate on deactivate	C_F on V_{CC} = 1 µF	0.1	0.3	0.5	V/µs
C_F	External filter capacitor (V_{CC} to GND)		0.47	1	3.3	µF
L	Inductor (LIN to V_{DD})			10		µH
Limax	Imax in inductor	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 2.7 V			400	mA
η	Efficiency	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 3.3 V		80		%

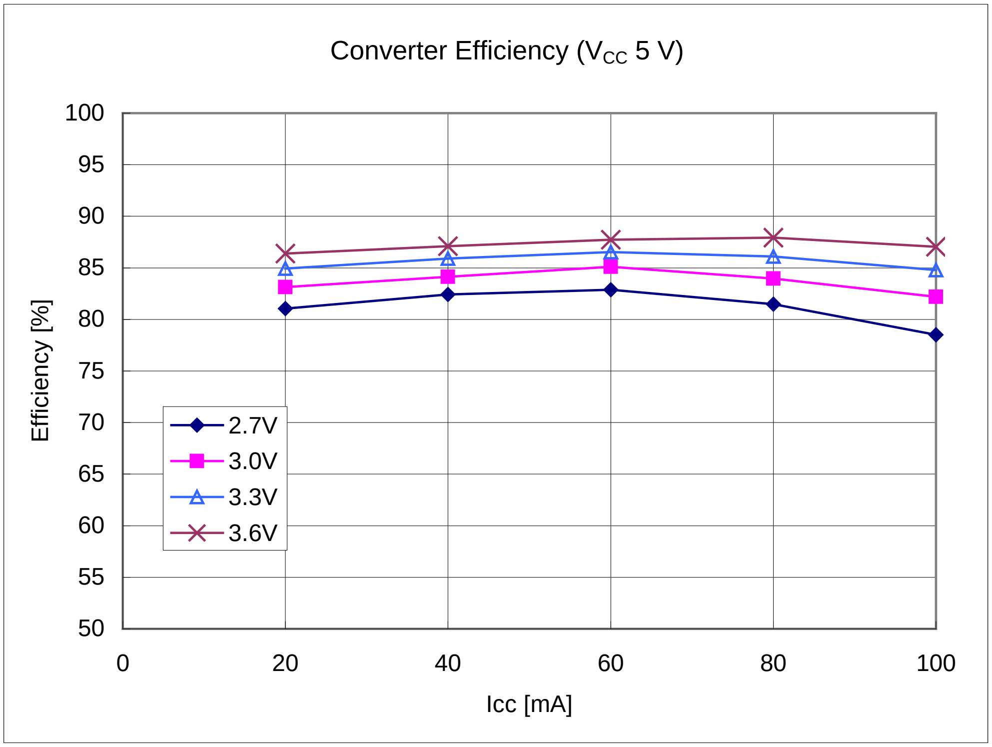


Figure 10: DC – DC Converter efficiency (V_{CC} = 5 V)

Output current on V_{CC} at 5 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

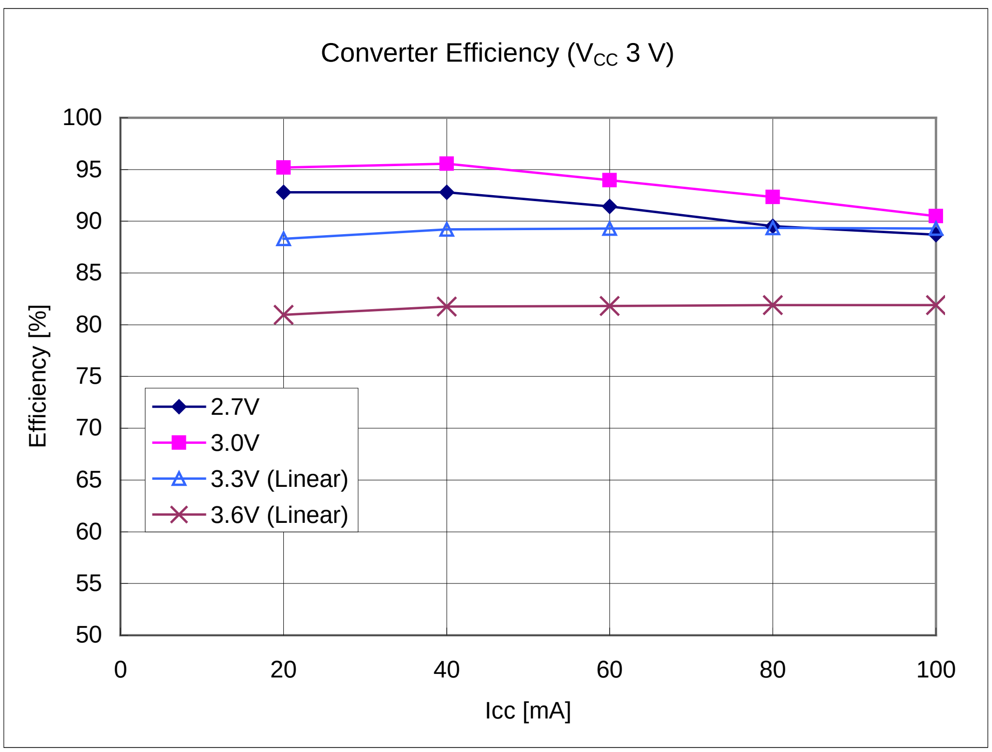


Figure 11: DC – DC Converter Efficiency (V_{CC} = 3 V)

Output current on V_{CC} at 3 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I//OUC, AUX1UC, and AUX2UC. I_{IL} requirements only pertain to I//OUC, AUX1UC, and AUX2UC.						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} = 0	0.9 V_{CC}		V_{CC}+ 0.1	V
		I_{OH} = -40 μA	0.75 V_{CC}		V_{CC} + 0.1	V
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} = 0	0.9 V_{DD}		V_{DD} + 0.1	V
		I_{OH} = -40 μA	0.75 V_{DD}		V_{DD} + 0.1	V
V_{OL}	Output level, low	I_{OL} = 1 mA			0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		1.8		V_{CC} + 0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)		1.8		V_{DD} + 0.30	V
V_{IL}	Input level, low		-0.3		0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	μA
I_{IL}	Input current, low	V_{IL} = 0, CS = 1			0.65	mA
		V_{IL} = 0, CS = 0			5	μA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω			15	mA
t_R, t_F	Output rise time, fall times	C_L = 80 pF, 10% to 90%. For I/OUC, AUX1UC, AUX2UC, CL = 50 pF			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	μs
R_{PU}	Internal pull-up resistor	Output stable for > 200ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
T_{FDIO}	Delay, I/O to I/OUC, I/OUC to I/O (falling edge to falling edge)			100		ns
C_{IN}	Input capacitance				10	pF
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} = -200 μA	0.9 V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL} = 200 μA	0		0.3	V
V_{INACT}	Output voltage when outside of a session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	mA
I_{CLK_LIM}	Output current limit, CLK				70	mA
t_R, t_F	Output rise time, fall time	C_L = 35 pF for CLK, 10% to 90%			8	ns
		C_L = 200 pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK, except for f = f_{XTAL}	C_L =35 pF, F_{CLK} ≤ 20 MHz	45		55	%

13.4 Digital Signals

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Digital I/O except for OSC I/O						
VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		1.8		VDD + 0.3	V
VOL	Output Low Voltage	IOL = 2 mA			0.45	V
VOH	Output High Voltage	IOH = -1 mA	VDD - 0.45			V
ROUT	Pull-up resistor, OFF			20		kΩ
|IIL1|	Input Leakage Current	GND < VIN < VDD	-5		5	µA
Oscillator (XTALIN) I/O Parameters						
V_{ILXTAL}	Input Low Voltage - XTALIN		-0.3		0.3 V_{DD}	V
V_{IHXTAL}	Input High Voltage - XTALIN		0.7 V_{DD}		V_{DD} + 0.3	V
I_{ILXTAL}	Input Current - XTALIN	GND < V_{IN} < V_{DD}	-30		30	µA
f_{MAX}	Max freq. Osc or external clock				27	MHz
δin	External input duty cycle limit	$t_{R/F}$ < 10% f_{IN}, 45% < δ_{CLK} < 55%	48		52	%

13.5 DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{PC}	Supply Current on V_{DD}	Linear mode, ICC = 0 I/O, AUX1, AUX2 = high		4.9		mA
		Step up mode, ICC = 0 I/O, AUX1, AUX2 = high		4.7		mA
I_{DD_PD}	Supply Current on V_{DD} in Power Down mode	PWRDN=1, Start/stop bit = 0 All digital inputs driven with a true logical 0 or 1		0.11	2.5	µA

13.6 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDF}	V_{DD} fault (V_{DD} Voltage supervisor threshold)	No external resistor on VDDF_ADJ	2.15		2.4	V
V_{CCF}	V_{CC} fault (V_{CC} Voltage supervisor threshold)	V_{CC} = 5 V	4.20		4.6	V
		V_{CC}= 3 V	2.5		2.7	V
T_F	Die over temperature fault		115		145	°C
I_{CCF}	Card over current fault		90		150	mA

14 Mechanical Drawings (28-SO)

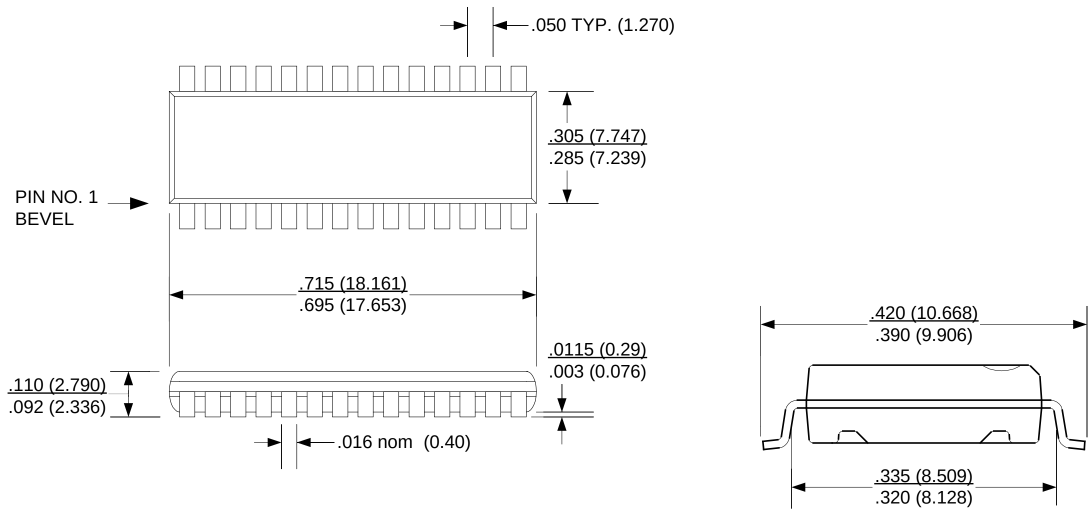
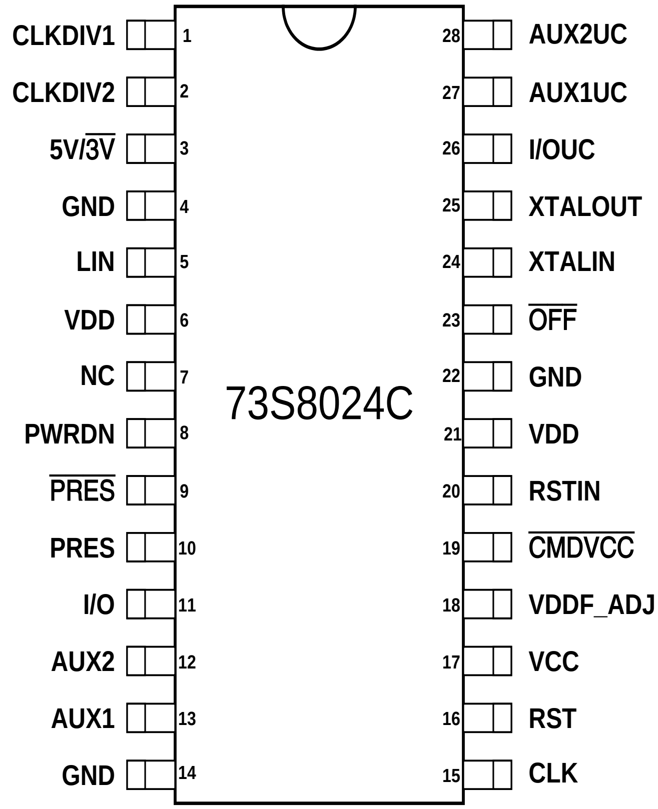


Figure 12: **28 Lead SO**

15 Package Pin Designation (28-SO)

Use handling procedures necessary for a static sensitive component.



(Top View)

Figure 11: 73S8024C 28-SO Pin Out

16 Ordering Information

Part Description	Order Number	Packaging Mark
73S8024C-SO 28-pin Lead-Free SO	73S8024C-IL/F	73S8024C-IL
73S8024C-SO 28-pin Lead-Free SO Tape / Reel	73S8024C-ILR/F	73S8024C-IL

17 Related Documentation

The following 73S8024C documents are available from Teridian Semiconductor Corporation:

73S8024C Data Sheet (this document)
73S8024C Demo Board User's Guide

18 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73S8024C, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: scr.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

Revision History

Revision	Date	Description
1.0	6/21/2005	First publication.
1.1	7/15/2005	Removed QFN package information.
1.2	12/5/2007	Add ISO and EMV logos, remove leaded package option, update 28SO package dimension.
1.3	4/3/2009	Remove all references to VPC as VPC must be tied to VDD.

Teridian Semiconductor Corp., 6440 Oak Canyon Rd., Suite 100, Irvine, CA 92618
TEL (714) 508-8800, FAX (714) 508-8877, http://www.Teridian.com